Performance Analysis of CMOS Full adders using 180nm Technology

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Abstract *— this paper presents the comparative analysis of power, delay and power delay product (PDP) of different Full adder circuit designs. Addition is the fundamental building block for processor architectures and for any VLSI application specific designs. Here group of different full adder structures are considered. Performance parameters in terms of power and delay are analyzed for special full adders like complementary and level restoring carry logic (CLRCL), static energy recovery full adder (SERF), GDI_XOR full adder also. All adder designs are simulated in Mentor Graphics tool with 180nm technology. Among the simulated full adders 8Transistor full adder is the high performed adder cell, which is the option for an efficient VLSI design.*

Keywords — *CLRCL, GDI_XOR, PDP, SERF*

I. INTRODUCTION

Adders are the basic building blocks for the design of VLSI application specific systems. In this paper power dissipation, power consumption of the circuit and time delay are analyzed. A bunch of different full adders like SERF, GDI_XOR full adder, GDI_XNOR full adder, Full adder 9TA, Full adder 9TB, CLRCL, 8T full adder, 9T Full adder, 6T full adder Type I, 6T full adder Type II are analyzed using Mentor Graphics tool.

II. PREVIOUS WORK

A full adder adds three one-bit binary numbers often represented as A, B, and Cin. Cin is the carry input to the full adder from the previous addition. The output of the full adder is two one-bit binary numbers often represented as Sum and Cout. The function of 1-bit full adder is described to calculate the Sum and the Cout as,

$$Sum = \bar{A}\,\bar{B}Cin + \bar{A}B\,\bar{C}in + A\,\bar{B}\,\bar{C}in + ABCin$$
$$= A \oplus B \oplus Cin \quad \ldots\ldots\ldots (1)$$

$$Cout = AB + BCin + ACin$$
$$= AB + Cin\,(A \oplus B) \quad \ldots\ldots\ldots\ldots (2)$$

Rewriting above equations

$$Sum = (A \odot B) \odot Cin \quad \ldots\ldots\ldots (3)$$

$$Cout = (A \odot B)\,Cin + (A \odot B)\,A \quad \ldots\ldots\ldots (4)$$

$$P = I * V \quad \ldots\ldots\ldots\ldots\ldots\ldots (5)$$

Equations (3) and (4) say that full adder can also be designed from XNOR logic which is used in GDI_XNOR full adder.

III. HIGH PERFORMANCE FULL ADDER

After analyzing the performance parameters of mentioned ten full adders, we can say that 8T full adder consumes less power and high speed compared to other adders. By exclusive ORing/cascading of A,B and Cin, the Sum output is obtained. The W/L ratio of all the transistors is 180nm. The delay is obtained by adding Sum and Cout delay and also voltage drop is because of threshold drop in transistor M3 and M6. This can be reduced when a=b=0, then nMOS pass transistor M8 will turn ON hence obtain the output |VT, p| - VT, n. By increasing the W/L ratio of transistors M7 and M8, their threshold drop can be reduced.

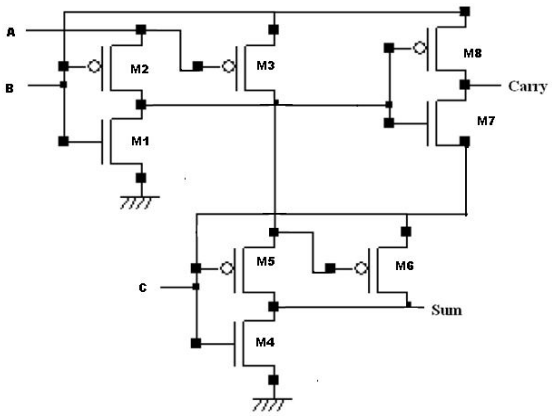

Fig. 1. Schematic model of 8T-full adder

IV. SIMULATION RESULTS AND COMPARISON

A group of different full adder designs were analyzed for their performance with the number of

transistor count, power dissipation, power consumption and delay in the circuits for driving the output. Group of full adders like SERF, GDI_XOR full adder, GDI_XNOR full adder, Full adder 9TA, Full adder 9TB, CLRCL, 8T full adder, 9T Full adder, 6T full adder Type I, 6T full adder Type II are analyzed based on the literatures. All the full adders are simulated based on 180nm technology with 1.8V supply voltage by applying all 8 combinations of inputs (000-111) and simulated using Mentor Graphics tool. Delay is calculated by adding Sum delay and Cout delay, power dissipation is extracted from netlist, power consumption is calculated from current, voltage [eq.(5)] of each circuit. The power consumption and power dissipation of 6T full adder Type I is less compared to 8T full adder. But delay and PDP of 8T full adder is better than 6T full adder Type I. Table 1 gives the comparison of delay, power dissipation, PDP and power consumption for different full adder designs.

V. FIGURES AND TABLES

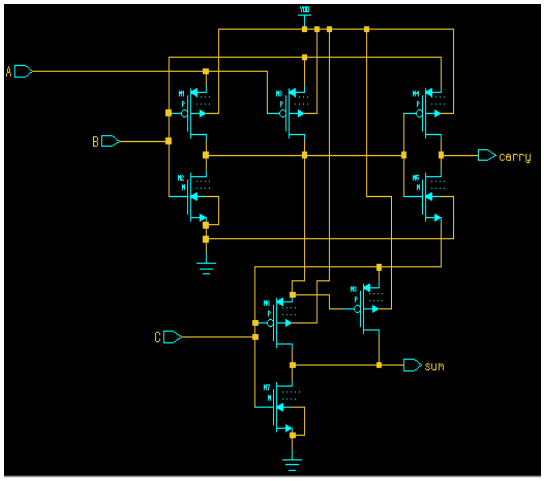

Fig. 2. Schematic of 8T-full adder

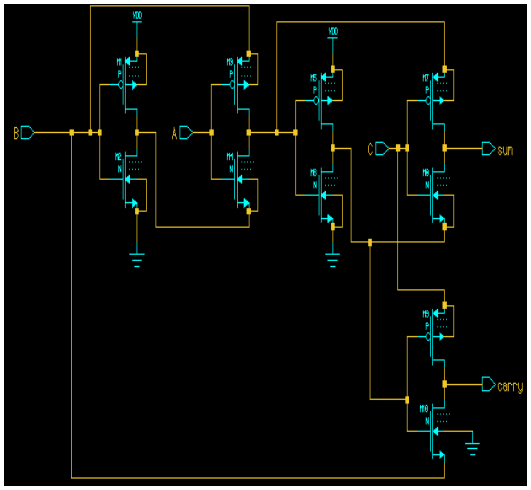

Fig. 3. Schematic of GDI_XOR Full adder

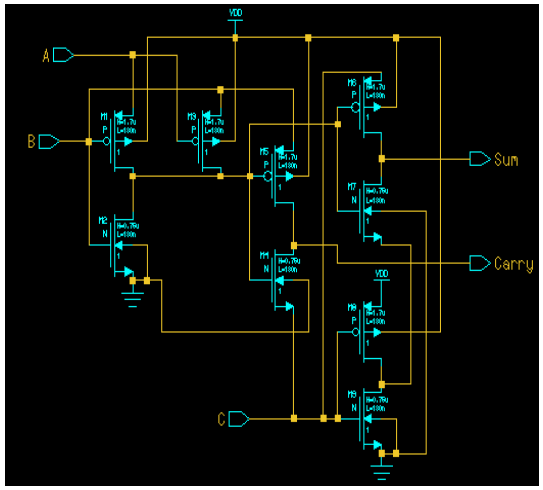

Fig. 4. Schematic of 9T Full adder

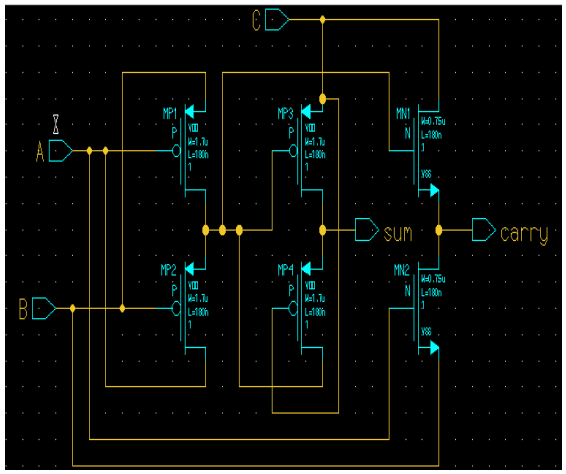

Fig.5. Schematic of 6T Full adder Type I

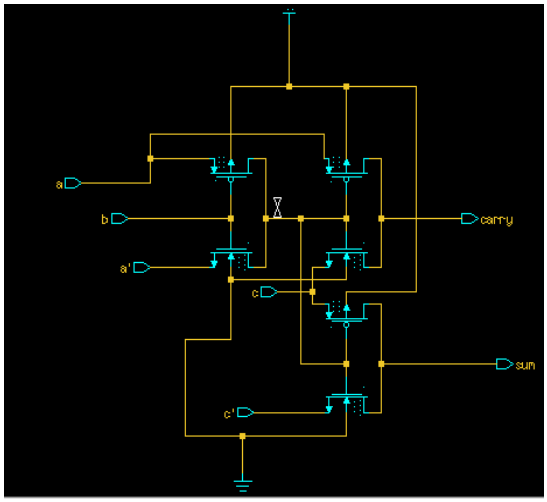

Fig. 6. Schematic of 6T Full adder Type II

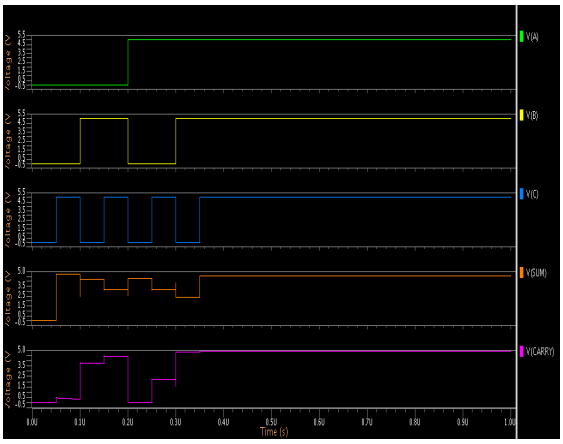

Fig. 7. Output waveform of 8T Full adder

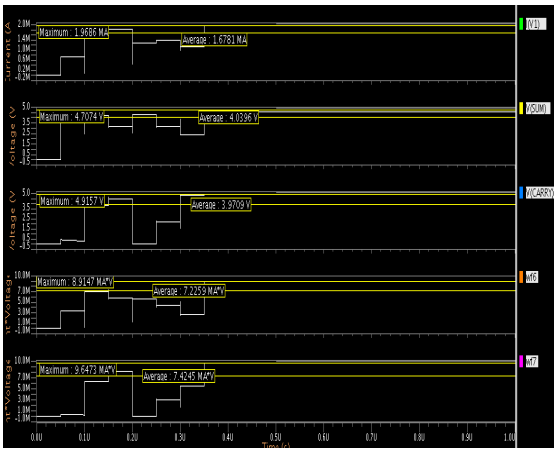

Fig. 8. Average power of 8T Full adder

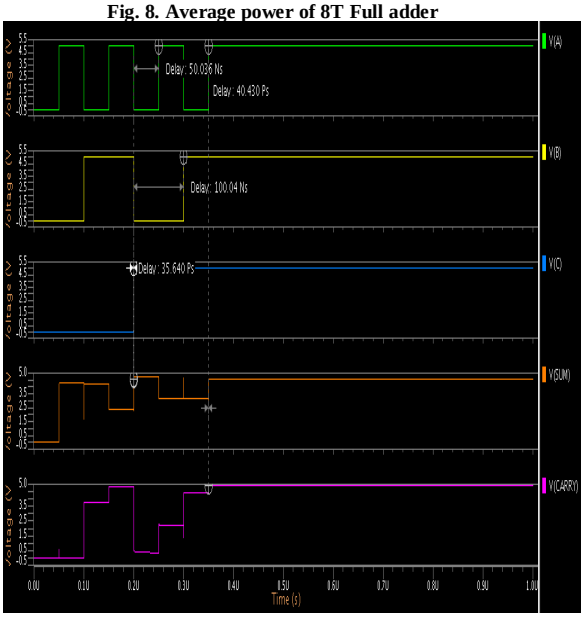

Fig. 9. Delay of 8T Full adder

TABLE 1
PARAMETERS OBSERVATION FOR 1.8V

Types of full adder	Delay (ns)	Power dissipation (nW)	PDP (W-sec) (10-15)	Power Consumption(mW)
8Transistors	150.1527	0.0325798	0.0048919	14.6504
GDI_XOR	347.29	294232.9	102184	38.5163
9T A	298.494	90747.6	27087.6	3.8159
9T B	298.517019	88855.9	26525	3.8003
SERF	297.75375	88855.9	26457	3.8051
GDI_XNOR	248.208	90747.6	22524	3.7561
9T	220.57968	0.0333791	0.0073628	16.843
CLRCL	299.66322	88856	26627	6.09307
6T Type I	251.63314	0.0260638	0.0065585	8.8676
6T Type II	200.055779	0.0755058	0.015105	9.5348

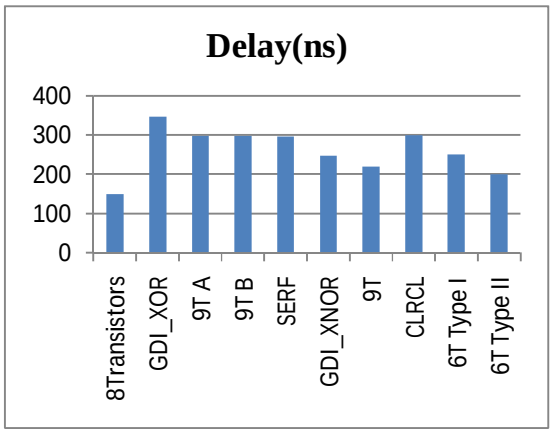

Fig:10 Comparative chart of delay in Full adders

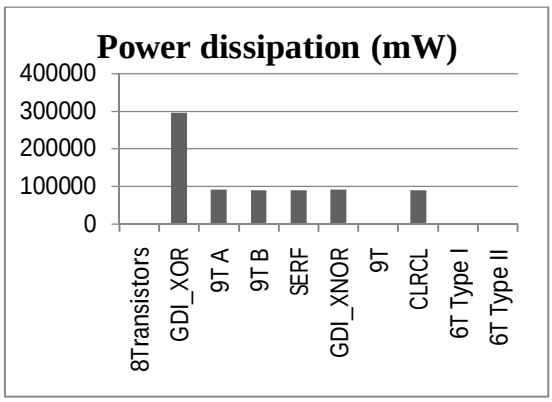

Fig:11 Comparative chart of power dissipation in Full adders

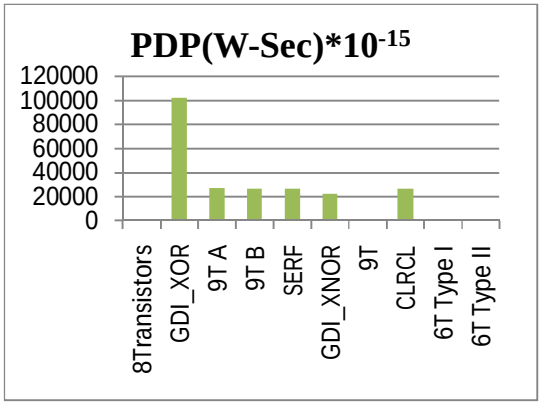

Fig:12 Comparative chart of PDP in Full adders

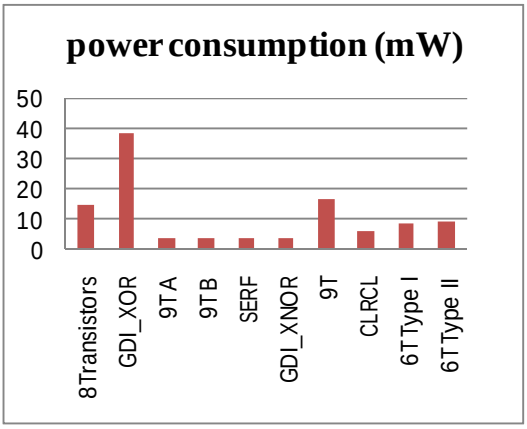

Fig:13 Comparative chart of power consumption in Full adders

VI. CONCLUSION

Among the ten different types of full adders, 8T full adder exhibits less delay, less PDP and high speed. So the high speed 8T full adder is a good candidate to design larger circuits such as multipliers, digital filters with respect to the delay and PDP.

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