Modified Interleaved Buck Converter with Reduced Input Current and Number of Switches

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Abstract *- There are many applications which needs low voltage DC supply in controlled manner. It includes various microcontrollers, several electronic ICs, laptops, traction signalling, electric vehicles etc. This DC-DC converter with interleaved technique can step down a high DC voltage to very low DC voltage with lesser voltage ripple and low value of inductor and capacitor. Since inductor and capacitor is having low value, the system will be of reduced size. With conventional buck chopper for converting high voltage to low voltage, very small duty cycle is required which further adds several limitations on different components and triggering circuitry. It requires relatively high values of inductor and capacitor. So the size of the system will be large. Comparatively the current ripple and voltage ripple will be more. The proposed converter reduces the complexity of the circuit and the input current also reduced. Here Simulations have been performed using MATLAB / SIMULINK. All results clearly show that very low voltage can be obtained using this topology. Moreover, the desired values of the output voltages can be numerically calculated which absolutely match with simulation results. Analysis is carried out by plotting the variation of voltage ripple with different frequencies.*

Keyword — *interleaved buck converter, DC-DC converter, Interleaved switches*

I. INTRODUCTION

The electronic equipment is consisting of the analog, digital and mixed-signal systems. They are becoming more complex to meet the challenges of increased demand for different features and due to continuous pressure on size reduction. The trend in minimizing the cost and power consumption of portable electronic devices are forcing to implement different system in a single IC. But these systems need very low input voltage and independent low power supplies. DC-DC converter can work as power supply unit for different system with isolation from each other. Beside this the design of converter is dependent on application.

Modern electronic systems usually have a number of different regulated DC supply voltages providing power to various functional blocks. The general trend for these supply voltages is to become lower moving into 0.6 V to 3.3 V range. In such applications synchronous buck converters have become preferable solution generating low voltages from relatively high voltage dc input [4]. But the ripple content may be very high. For obtaining DC with reduced ripple content we go for interleaved converter. In Applications where non isolation, step-down conversion ratio, and high output current with low ripple are required, an interleaved buck converter (IBC) has received a lot of attention due to its simple structure and low control complexity. Interleaved Buck Converter Have Low Switching Losses and Improved Step-Down Conversion Ratio. Compared with traditional converter, interleaved converter provides lower peak-to-peak ripple amplitude, smaller size of device, lower stress on components, easy maintenance, reliability and higher fault tolerance [10]. The size of the passive components used in the buck converter can be reduced by increasing the switching frequency, but may lead to increased switching losses. Therefore, in order to reduce the size of the passive components used, the converter can be interleaved. Interleaved topologies also provide the advantage of lower ripple in the output current [11].

Nowadays the demand of electrical power is growing at a rapid rate. To meet this demand, more efficient systems are needed. For fulfilling this faster and more efficient device such as data processors, microcontrollers etc are needed. These devices work under very low voltage. This interleaved dc-dc converter gives low voltage and high current at its output. Since interleaving methodology is used here the voltage ripple at the output terminals is minimized. With the advancement of the ICs, the size of the devices is getting reduced day by day. Here for obtaining low voltage at the output the required duty ratio is large (nearly 50%). So the value of inductor and capacitor is reduced. The size also gets reduced. In conventional buck converter, extremely low duty cycle is required for obtaining low output voltage which increases the value of inductor and capacitor used [1].

The proposed converter reduces the complexity and the input current also reduced. In-stead of 4 switches there are only 2 switches. Thus the control circuitry is reduced. Finally, the variation of output voltage ripple with different frequencies are analysed.

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II. SYSTEM DESCRIPTION

The block diagram of the system is shown in Fig 1. It is basically two buck converters connected in parallel. The duty cycle of both the converters can be same or different. For simplicity, the duty cycle of both buck converters is kept same here. By varying the duty cycle of both converter or any one converter, the desired output voltage can be obtained. Here the duty cycle is comparatively high. It gives very low voltage at the output.

In conventional DC-DC buck converter 6.25% duty cycle is required to get 1.5V with 24V of input voltage but here both the choppers are being operated at duty cycle close to 50% in order to get same 1.5V of output voltage with 24V of input. The advantage of increasing the duty cycle is that value of inductor and capacitor requires for continuous conduction gets reduced but both voltage ripple and current ripple gets increased.

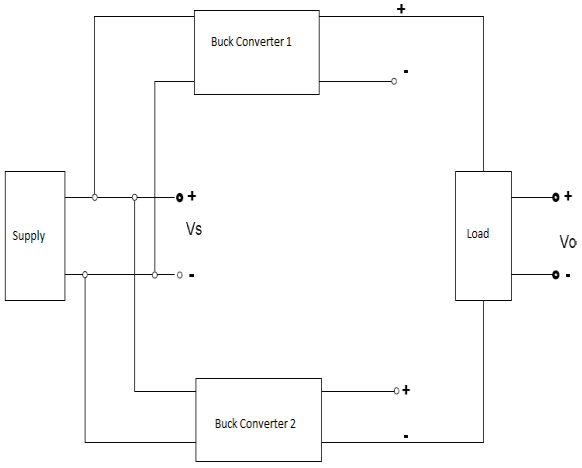

Fig 1: Block diagram of the system

A. Circuit Diagram

The circuit diagram of the system is shown in Fig 2. Two buck converters are cascaded here. In this topology, there are two techniques involved. First one is interleaved and second one is synchronous buck technique. The rest one implies that both buck chopper are interleaved from one another by 180 degree as triggering pulse in S1, S3 are having the time lag corresponding to 180 degree. So S3 is on after some time i.e. t=1/(2*fc) when S1 is ON.

Second technique is synchronous buck converter technique. There will be a main switch and a complementary switch. S2 which in turn is complementary with S1 and similarly S4 is complementary with S3. The advantage of using the synchronous buck topology is that it reduces power loss taking place in diode during conduction period which is equal to the product of the forward voltage drop and the current owing during conduction period.

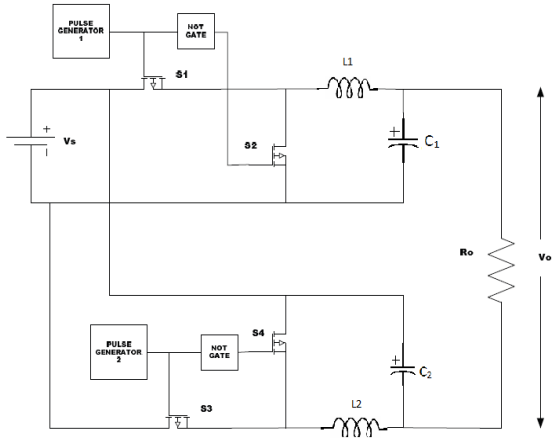

Fig 2: Circuit Diagram of the System

But in the above interleaved DC to DC buck converter the amount of input current is very large. So it's practical implementation is difficult. Also since there are 4 switches the control circuitry is complex. So this interleaved DC to DC buck converter is modified.

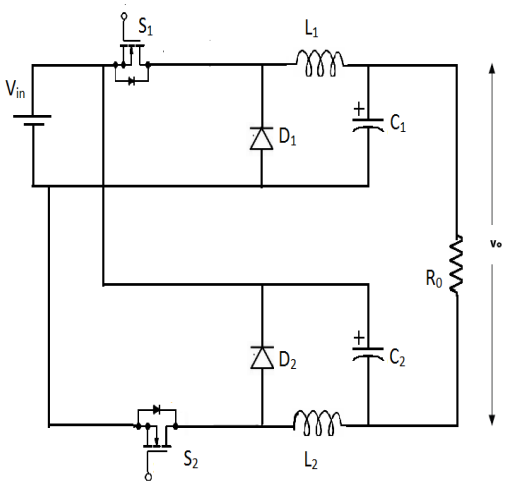

Fig 3: Modified circuit diagram of the system

B. Modes of Operation

Modes of operation can be explained in two modes.

1) Mode 1

In mode 1 switch S1 is on. Switch S2 is ON. Diode D2 conducts. Here are two tank circuit. Since L and C values of both the tank circuit is same the frequency is also same. The voltages of the tank circuit are equal in magnitude but opposite in sign. So this will cancel each other. The output voltage will be DC.

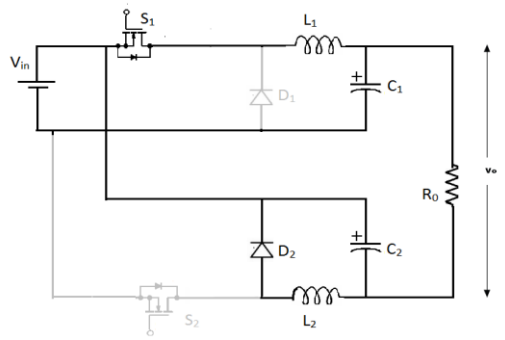

Fig 4: Mode 1 Operation

2) Mode 2

In mode 2 switch S2 is on. Switch S1 is off. Diode D1 conducts. Here also two tank circuits are present. Operation is similar to mode 1.

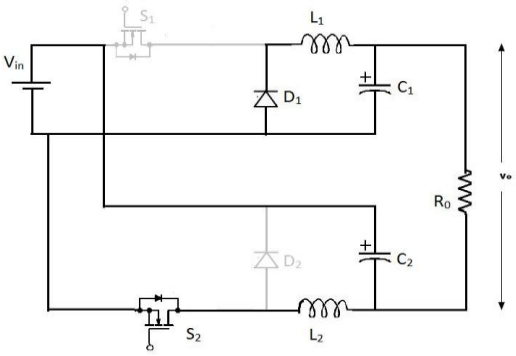

Fig 5: Mode 2 Operation

III. MATHEMATICAL ANALYSIS

Now in this section it can be observed that how this dc-dc converter topology can obtain low output voltage at higher duty cycle which has its obvious advantages over conventional buck converter that operates at low duty cycle about less than 10% in order to obtain same output voltage. For DC-DC buck converter the relation is:

$$Vo = DVs \quad (1)$$

$$Vo = V\,s - V1 - V2 \quad (2)$$

$$V1 = D1 * Vs - Vdr \quad (3)$$

$$V2 = D2 * Vs - Vdr \quad (4)$$

$$Vo = Vs - D1*Vs - D2*Vs - 2Vdr \quad (5)$$

Assuming that both converter operates at same duty cycle then,

$$D1 = D2 = D \quad (6)$$

$$V_O = V_s - 2*D*V_s - 2V_dr \quad (7)$$

$$V_O = V_s - 2*D*(V_s + V_dr) \quad (8)$$

Assume D =35%, Vs =24V, Vdr =0 We get V_0 =7.2V Practically voltage drop cannot be zero. So Vo will be less than 7.2V.

IV. SIMULATION MODELS AND RESULTS

A. *Simulation Model of Modified Interleaved Buck Converter*

The detailed MATLAB/Simulink model of interleaved buck converter is made. The simulation parameters are given by the table 1.

Table 1: Simulation parameters

Parameters	specifications
Supply voltage	24V
L	3mH
C	1uF
Voltage ripple	0.05
Current ripple	0.009

The simulation model is plotted on the basis of the parameters given in table 1. The simulink model is given in fig 6. Here we will obtain low voltage at the output. The output power is also low. It shows that it can be used for low power application. Voltage and current ripple is reduced. We are obtaining low voltage at comparatively higher duty ratio nearly equal to 50%. Output current is large. Here the inductors and capacitors are given with very low value. Both the inductors and both the capacitors are taken as the same.

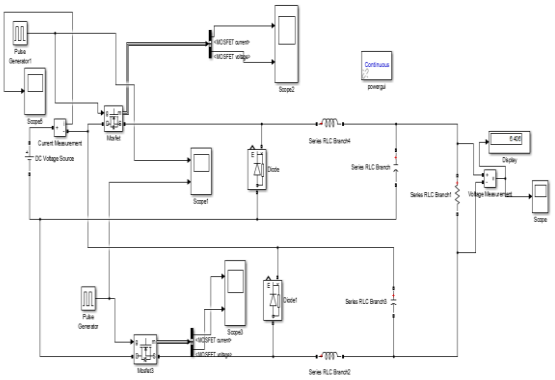

Fig 6: Simulink Model of Interleaved Buck Converter

Here voltage pulse is given to switch S1 and this pulse is shifted by 180 degree and given to switch S2. Switching pulse for switch S1 is given in fig 7 and for switch S2 is given in fig 8.

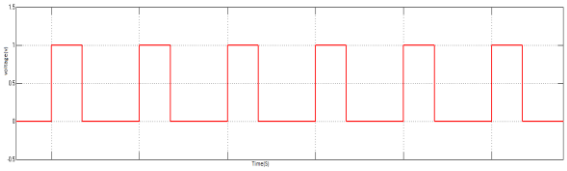

Fig 7: Switching pulses for switch S1

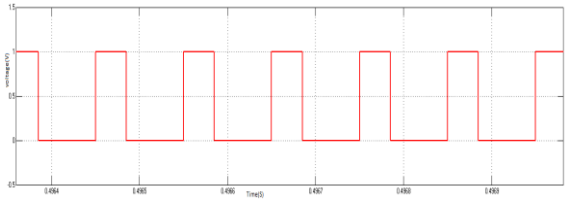

Fig 8: Switching pulses for switch S2

The output voltage obtained is very low that is nearly 5V. the output current is obtained in the range of 13A. The output voltage and current waveform is given by,

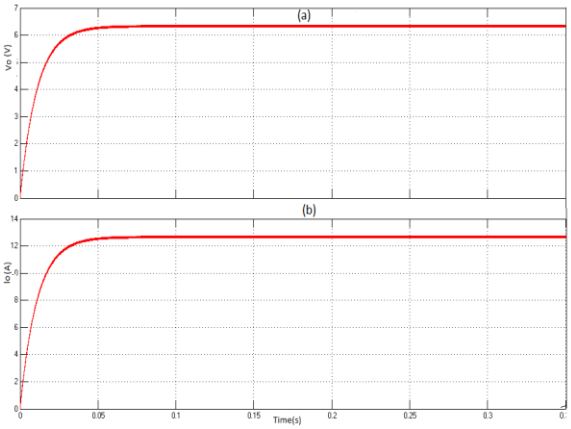

Fig 9: (a) Output voltage waveform (b) output current waveform

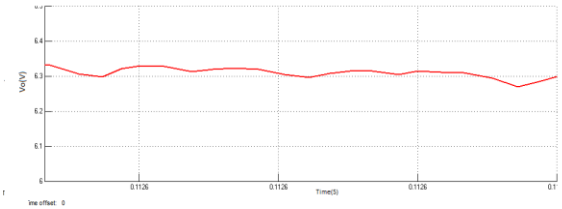

Fig 10: Output voltage ripple

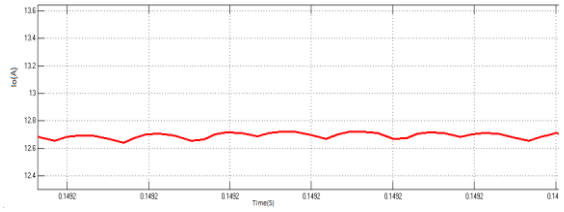

Fig 11: current ripple

From Fig 10 and Fig 11 it is clear that output voltage ripple and current ripple is very low. The voltage ripple is in the range of 0.03 and current ripple is 0.009.

The inductor current and capacitor voltage is given by Fig 12 and fig 13 respectively. The current through the inductor is same as that of the output current. The capacitor voltage is 20V.

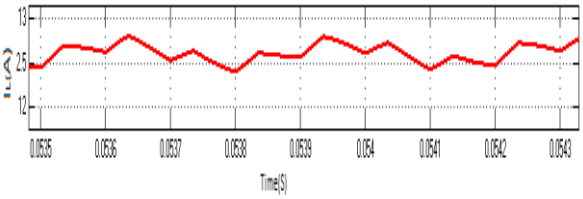

Fig 12: Current through the inductor

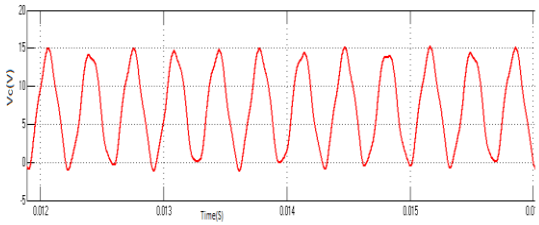

Fig 13: voltage across the capacitor

Voltage stress across the switch S1 is given in Fig 14 and across S2 is given in Fig 15. Across switch S1 the voltage stress is 24V. Across switch S2 it is in the order of 23.9.

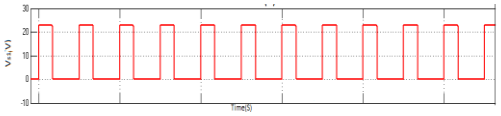

Fig 14: Voltage stress on switch S1

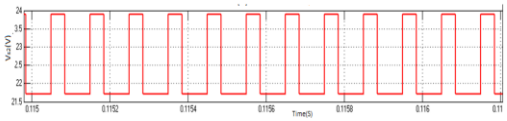

Fig 15: Voltage stress on switch S2

B. ***Simulation Model of Conventional Buck Converter***

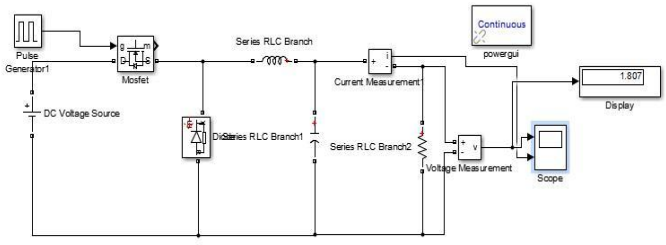

Fig 16: simulation model of conventional buck converter

Output voltage and output current wave form is given in Fig 17.

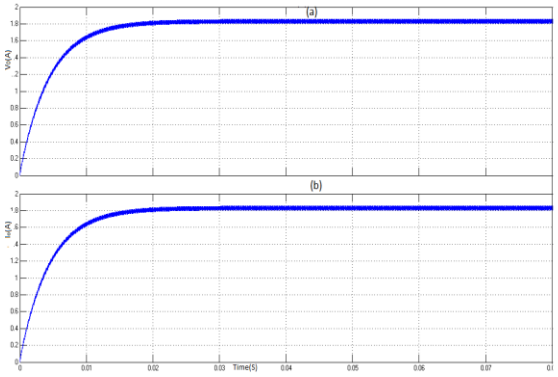

Fig 17: (a) output voltage waveform of conventional buck converter (b)output current waveform of conventional buck converter.

C. *Comparative Study*

Table 2: Comparative study

Parameters	Conventional buck	Proposed topology
Supply voltage	24V	24V
Output voltage	6V	6V
L	58mH	3mH
C	100µF	1µF
Voltage ripple	0.2	0.05
Duty	35%	35%

A comparative study is made between the proposed converter and the conventional buck converter by keeping input voltage, output voltage and duty ratio as constant. From the comparative study it is observed that the value of inductor and capacitor is reduced thereby size of the device is also reduced. The voltage ripple is very low in proposed converter when compared with conventional buck converter.

V. ANALYSIS OF PROPOSED CONVERTER

The proposed circuit is analysed by plotting the variation of voltage ripple with different values of frequencies. The voltage ripple varies when frequency changes. At high frequencies the ripple content in the output voltage is low. That is when frequency increases the output ripple decreases. Hence we can say that the proposed converter is more effective at higher frequencies.

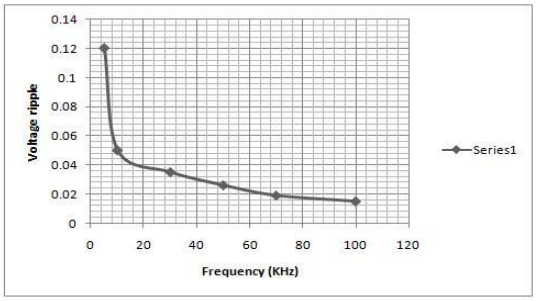

Fig 18: Frequency Vs Voltage ripple graph

VI. EXPERIMENTAL SETUP AND RESULT

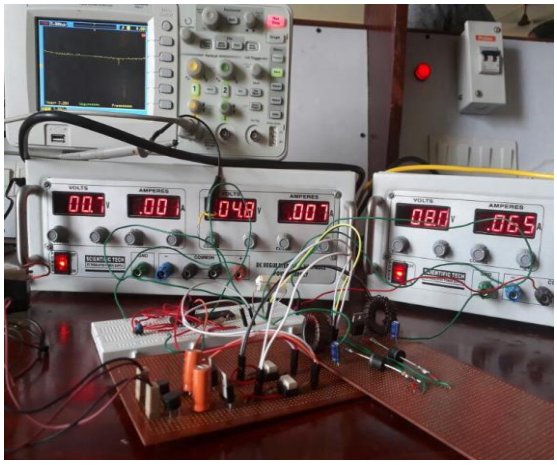

Fig 19: Experimental setup

A. *Components Used*

Table3: Components used

COMPONENTS USED	SPECIFICATION
CONTROLLER	PIC16F877A
MOSFET	IRF540
DRIVER IC	TLP50
INDUCTANCE	3mH
CAPACITANCE	1µF
POWER DIODE	INF5822

VII. EXPERIMENTAL OUTPUT

A. *Switching Pulses*

Switching pulses of switch S1 and S2 is experimentally obtained. Both these switches possess 180-degree phase shift.

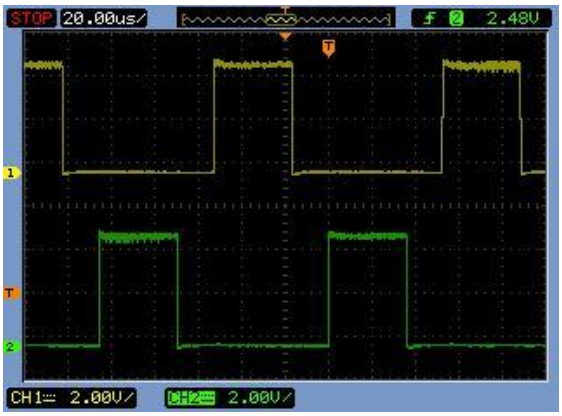

Fig 20: Switching pulses for S1 & S2

B. ***Output Voltage***

Output voltage obtained is shown in Fig 21. 3.2V is obtained at the output.

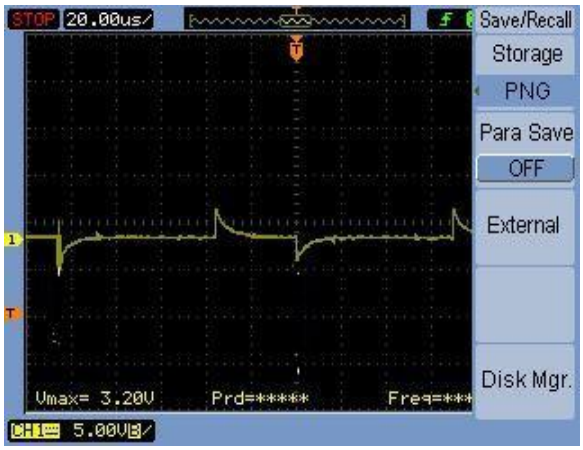

Fig 21: Output voltage

VIII. CONCLUSIONS

In this proposed interleaved DC to DC Buck Converter we obtain reduced voltage ripple at the output. The control circuitry is much simple since only two switches are there. Hence it is economical. Required capacitor and required inductor value is also low. Hence the device size is reduced. In the modern system the continuous sandwiching the large number of devices on single chip may increase the size. So the size become
a major concern. By the use of this system we can develop the system with reduced size. Interleaving methodology is used to minimize the voltage ripple. Here the system is compared with conventional buck converter. On comparing, conventional buck converter with our system it has been found that the voltage ripples decrease from 0.2V to 0.03V. That is Voltage ripple obtained is 0.5% of the output voltage. Current ripple also gets reduced. current ripple is in the range of 0.009A. The power output obtained is low. Hence the proposed converter is highly significant in low power application.

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