A Single Switched Capacitor Cell Multilevel Inverter using APOD PWM Technique for Power Grid Application

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Abstract — Multilevel inverter is a power electronic device that is used for high voltage and high power application because of its characteristics of synthesizing a sinusoidal voltage on several DC levels. They give good quality output resulting with lower harmonic distortion in the output. This topology is designed based on Switched Capacitor technique and the number of output levels is determined by the number of Switched Capacitor (SC) cells. Only one DC voltage source is needed and the problem of capacitor voltage balancing is avoided as well. A small input voltage can be used to produce a boosted output voltage, by switching the capacitors in series and in parallel. Number of switching devices used in the circuit is reduced as compared to the conventional cascaded multilevel inverter of same configuration. This work also presents the simulation study of Performance factors such as % THD, voltage stress, ripple voltage etc. using the Alternative Phase Opposition Disposition (APOD) modulation technique. The simulations are done with MATLAB/ SIMULINK software. The control strategy is the key part for the circuit and switching signals are generated with the help of PIC16F877A microcontroller.

Keywords — *Multilevel Inverter, charge Pump, Switched Capacitor, Grid Application.*

I. INTRODUCTION

In recent years, multilevel inverters are attracting lot of attentions due to the increasing higher power quality requirements. It possesses the several features such as reduced harmonic distortion, near sinusoidal output voltage waveform and reduces *dv/dt* stress. As a result, multilevel inverters are used in industrial applications to meet the requirements. Inverter performs DC to AC conversion for distributed electrical energy systems and electrical vehicles.

Multilevel inverters have several advantages over the conventional inverters. One of the significant advantages of multilevel inverter configuration is the harmonic reduction in the output waveform without increasing the switching frequency or decreasing the inverter power output. Conventionally, multilevel inverters are classified in to two categories: Type 1 and Type 2. Type 2 inverter uses multiple DC voltage capacitors; neutral point clamped [1] and flying capacitors. Type 1 inverter uses multiple DC voltage sources; cascaded H-bridge inverter [2]. Type 1 inverters are again divided in to two: symmetrical and asymmetrical inverters. In cascaded symmetrical inverters all the DC voltage sources are equal where as asymmetrical inverter uses unequal voltage sources. However, their drawbacks are also apparent such as Cascaded H –bridge inverter requires multiple separate dc sources. Problem of voltage balancing among DC link and clamping capacitors exists in both neutral point clamped and flying capacitor inverters [2]. Diode clamped or neutral clamed has the difficulty of increase in the number of clamping diodes as the level increases. Similarly, in flying capacitor the number of capacitors increases and system becomes bulkier. Among these inverter topologies cascaded inverter achieves greater reliability and simplicity because it does not requires any power electronic devices other than switches and capacitor voltage balancing technique.

From normal inverter, magnitude of the inverter output is same as that of input voltage when the modulation index is equal to one. To offer output voltage greater than input we have to use a DC-DC boost converter. Other method is to use inductors or transformers but at higher power, transformer should withstand heavy magnetic core so that it can sustain higher power level [3]. As a solution charge pump [20] technique is used with switched capacitors, which does not requires any inductors. Charge pump technique generates larger output voltage from a small DC voltage with a switched capacitor [3]-[5].

Multilevel inverters are mainly controlled by Multicarrier Pulse Width Modulation method and the harmonic contents can be reduced by using PWM techniques [6]. There are two PWM methods mainly used in multilevel inverter control strategy [7]. One is fundamental switching frequency and another one is high switching frequency.

Photovoltaic (PV) systems are nowadays recognized for their contribution to clean power generation. A Photovoltaic (PV) system directly converts sunlight into electricity. The basic device of a PV system is the PV cell [22]-[27]. Cells may be

grouped to form panels or arrays. The classic configuration of a grid connected renewable energy system consists basically of two parts. The first stage is the energy supply, by a photovoltaic array. Additionally, a power conditioner is necessary to boost the voltage generated by the photovoltaic panel. In the second stage, an inverter is used to convert and adapt the energy accumulated in an intermediate storage element to be consistent with the voltage and power quality requirements of the utility grid.

In this paper, the performance analysis of switched capacitor seven level inverter is evaluated using APOD technique. For the grid application eleven level inverter is developed.

II. CIRCUIT TOPOLOGY OF SEVEN LEVEL INVERTER

A boost switched-capacitor (SC) multilevel inverter is formed by cascading two structures, a switched capacitor network and a two level (full bridge) inverter explained in [10]. The basic switched capacitor cell shown in figure 1, decides the number of output levels. Each switched capacitor cells are connected across the input DC source through a common switch S_b shown in figure 2 [10]. By cascading N-number of switched capacitor cells generates (2N+3) levels in the output and the maximum output voltage is $(N+1)V_{dc}$. Only one DC voltage source is needed and the problem of capacitor voltage balancing is avoided. One basic switched capacitor cell is formed by one capacitor, one switching devices with two diodes. Each of these cells is connected in parallel with each other to increase the number of levels required in the multilevel output. Each cell is made to operate as a parallel-series converter. The proper switching of these devices is required for obtaining the desired output [6]-[10].

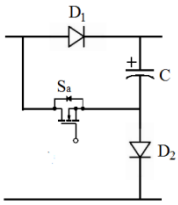

Fig 1: Switched Capacitor Cell

Figure 3 shows the structure of seven level inverter. A Switched Capacitor (SC) circuit is used in order to obtain a boost multilevel DC voltage waveform, which is inserted between the source and the full bridge inverter [8]. The multilevel AC output voltage of the switched capacitor circuit is the input voltage of the classical full bridge inverter, resulting in a staircase output voltage waveform.

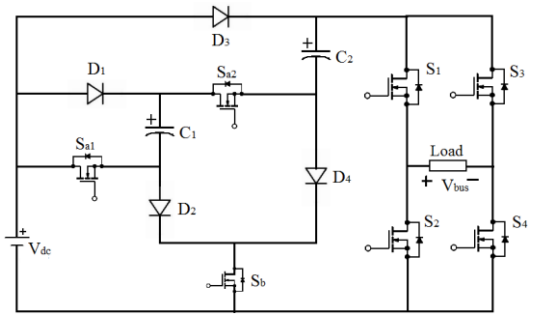

Fig 2: Circuit diagram of Seven Level Inverter

The multilevel output voltage is larger voltage than the input voltage by connecting the capacitors in series and in parallel to the input.

III. OPERATING PRINCIPLE OF INVERTER

A switched capacitor multilevel inverter which is capable of giving a maximum of seven level is analyzed here, the number of capacitor cells to be used in the circuit are N=2. When the capacitor and the input voltage source are connected in parallel, the capacitors are charged. When the capacitor and input voltage source are connected in series, the capacitors are discharged.

A. Mode 1 (V_{bus} = 0 V)

All capacitors are made in parallel with the input source voltage by turning ON the switch S_b, thus each capacitor maintains an input voltage across it. Switches in same upper/lower limb conduct either S_2 and S_4 or S_1 and S_3 are turned ON to produce the zero voltage at the output shown in figure 3.

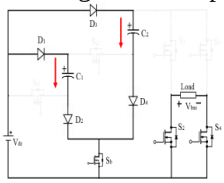

Fig 3: Mode 1

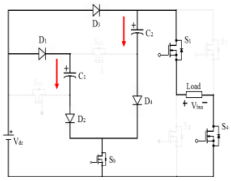

Fig 4: Mode 2

B. Mode 2 ($V_{bus} = V_{dc} - V_f$)

In this mode switches S_1 and S_4 of full bridge inverter are turned ON to generate the first level, which is equal to (V_{dc} - V_f) shown in figure 4. Where V_f is the forward voltage drop of diode D_3. Switch S_b is also ON to make the capacitor to get charged.

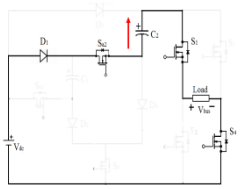

Fig 5: Mode 3

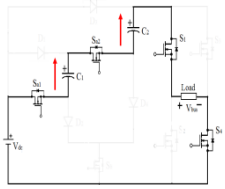

Fig 6: Mode 4

C. Mode 3 ($V_{bus} = V_{dc} + V_{C2} - V_f$)

This is the mode when one capacitor is connected in series. The capacitor C_2 is connected in series with

the source by simultaneous turning ON of switch S_{a2} shown in figure 5. The switches S_1 and S_4 of full bridge inverter are conducting in this period. So the output voltage is (V_{dc} + V_{C2} - V_f). Where V_f is the forward voltage drop of diode D_1 and V_{C2} is the voltage of capacitor C_2.

D. Mode 4 ($V_{bus} = V_{dc} + V_{C1} + V_{C2}$)

In this mode all the two capacitors are connected in series. The capacitor C_1 and C_2 are connected in series with the source voltage by making switches S_{a1} and S_{a2} conducting shown in figure 6. The switches S_1 and S_4 of full bridge inverter are conducting in this period. So the last voltage level is (V_{dc} + V_{C1} +V_{C2}). Where V_{C1} is the voltage of capacitor C_1 and V_{C2} is the voltage of capacitor C_2.

Similarly the negative half cycle can be obtained by turning ON S_2 and S_3 instead of S_1 and S_4, thus seven level output can be obtained. The maximum voltage stress across each of the switches of switched capacitor network is the input voltage.

IV. SYSTEM ANALYSIS

A. Number of Levels and Maximum output value

A Switched Capacitor (SC) circuit is used in order to obtain a boost multilevel AC voltage waveform. The maximum output voltage level is determined by the number of switched capacitor connected to the network.

No. of output levels, m = 2N+3 (1)

Maximum output voltage = (N+1)V_{dc} (2)

B. Voltage stress across the Switches

The maximum voltage dropped is the output voltage which is across the full bridge switches (S_1, S_2, S_3 & S_4) and minimum voltage dropped is across the switches in the switched capacitor cell. If N is the number of SC cells;

Voltage stress across the full bridge switches (S_1, S_2,S_3 & S_4)

$$V_{fullbridge} = (N+1)\,V_{dc} \quad (3)$$

Voltage across the switch S_b ,

$$V_{sb} = V_{sa1} \quad ; \text{Switch } S_{a2} \text{ is ON} \quad (4)$$

$$= (V_{sa1} + V_{sa2}) \quad ; \text{both } S_{a1} \text{ \& } S_{a2} \text{ ON} \quad (5)$$

Voltage across the switches in SC network,

Voltage across switch S_{a1} , $V_{sa1} = V_{dc} - V_f$ (6)

Voltage across Switch S_{a2}, $V_{sa2} = V_{dc} - 2V_f$ (7)

Where, V_{dc} is the input DC voltage

V_f is the forward voltage drop of diodes

C. Voltage across the Diodes

Proposed inverter uses double number of diodes compared to the existing topology [3][4]-[9]. In which diodes in the upper limb of the SC cell undergoes high frequency switching and diodes in the lower limb of SC cell undergoes normal switching with different reverse biased voltages. All diodes are forward biased when common switch S_b is turned ON.

Diode D_1 in the upper limb of SC cell is reverse biased by the capacitor voltage when switch S_{a1} is turned ON and Diodes in the lower limb is reverse biased when the common switch S_b is turns off.

Diode D_1 in the upper limb, $V_{D1} = - V_{c1}$

Diode D_2 in the, $V_{D2} = -(V_{dc} - V_f)$ (8)

D. Voltage ripple of capacitor

For a switched capacitor cells, when the switch S_{ai} is turned OFF, capacitor C_i (i = 1, 2.....N) starts charging to (V_{dc} – 2 V_f) and when switch S_{ai} turned ON means the charging period of capacitor C_i ends shown in figure 2.

Voltage ripple of capacitor, $\Delta V_c = \frac{1}{C_i}\int_{t_0}^{t_1} i_0\, dt$ (9)

Where t_0 and t_1 are the start and end time of discharging period. For different PWM techniques t_0 and t_1 varies.

$$\Delta V_{Ci} = \frac{1}{2\pi f_s C_i}\int_{\theta_{1+i}}^{\pi-\theta_{1+i}} i_0\; d\omega t \quad (10)$$

$$= \frac{V_{in}}{2\pi f_s R C_i}[\pi - 2\theta_{1+i}] \quad (11)$$

$$= \frac{V_{in}}{2\pi f_s R C_i}\sum_{a=i}^{n}[\pi - 2\theta_{1+i}](a+1) \quad (12)$$

So for the two capacitors C_1 and C_2, the corresponding capacitor ripple voltages are;

E. Conduction Losses

The conduction losses of switched capacitor cells occurred during charging process of the capacitor. When switch S_{ai} is turned OFF, the capacitor C_i (i = 1, 2.....N) is charged to (V_{dc} – 2V_f) through two forward biased diodes shown in figure 2, where V_f is the forward voltage drop of a diode. For seven level inverter circuits two similar charging paths operated in parallel with a common switch of S_b. The conduction losses during charging of Capacitor C_i are given by the equation (13)

$$P_{con} = \frac{f_s}{2}\sum_{i=1}^{p} C_i\left(2V_f + \Delta V_{Ci}\right)\Delta V_{Ci} \quad (13)$$

Where, p is the number of capacitor charging parallel path, p, i = 1, 2.....N

During the discharging period, capacitors are connected in series with the input DC source. Then conduction loss during discharging period is given by the equation (14)

$$P_{con\_dis} = (ESR + r_{Sa} + 2r_s + r_D)\left(\frac{V_{in} + V_C - V_D}{R + ESR + r_{Sa} + 2r_s + r_D}\right)^2 \quad (14)$$

Where, C_{eq} is the equivalent capacitance

ESR is the equivalent series resistance

r_D is the resistance of diodes

r_{Sa} is the resistance of all SC switches

r_s is the resistance of the H-Bridge switches

From this relation (14), by selecting appropriate switches with low ON resistance, we can reduce the losses.

F. Switching Losses

Switching losses occur during turning ON and turning OFF time and they dominate for the fast switching operations. The switching loss P_{sw} of the

switch during one switching cycle is given by the equation (15)

$$P_{sw} = f_s C_{ds} V_s^2 \quad (15)$$

Where, C_{ds} is the parasitic capacitance of MOSFET
V_s is the voltage across the switch

V. PULSE WIDTH MODULATION SCHEMES

To control and to generate high quality output waveform, an appropriate modulation scheme is required. Among the various modulation schemes, multicarrier pulse width modulation stands out because it offers significant simplicity and easy to implement switching waveforms.

A. *Sinusoidal Alternative Phase Opposition Disposition PWM*

For an m-level inverter, (m-1) carriers with same carrier frequency f_c and same peak-to-peak amplitude A_c are continuously compared with the sinusoidal reference waveform having amplitude A_m and reference frequency f_m. Sinusoidal Alternative Phase Opposition Disposition alternate carriers are phase shifted by 180˚ from its neighbour [6] - [8] shown in figure 7.

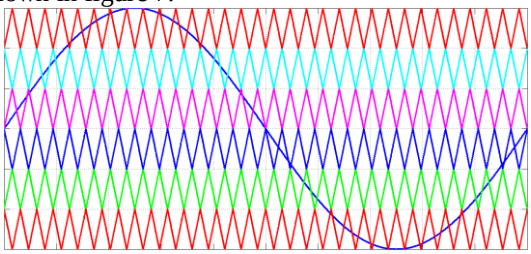

Fig 7: Sinusoidal Phase Disposition PWM

VI. Simulation and Results

For an input of 5V, switching frequency f_c as 1kHz and reference frequency f_m as 50Hz, the multilevel inverter was simulated in Matlab Ra2014a.

B. *Gate Pulse Generation*

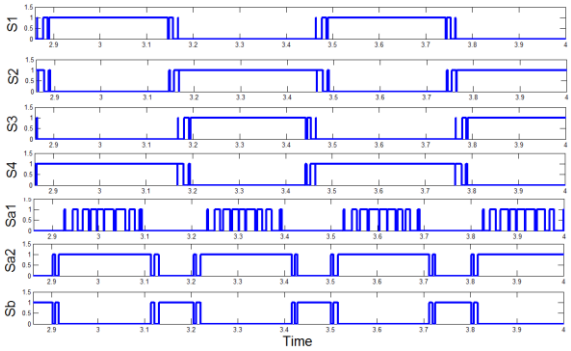

Fig 8: Switching Pulses using APOD techniques

Gate signals are obtained by comparing sinusoidal reference or modulating signal at fundamental frequency (50Hz) with triangular carrier signal which are at higher frequency. Here switching frequency is selected as 1kHz for better performance or a carrier to fundamental frequency ratio of 20. Figure 8 shows the seven switching pulses using APOD technique.

C. *Input current*

Figure 9 shows the input current drawn by the circuit. Input current which is a combination of two diode currents and one switch current during the capacitor discharging period. Diode current is used to charge the capacitors when the switch S_a is turned OFF. During the discharging period switch is operated in a higher switching frequency.

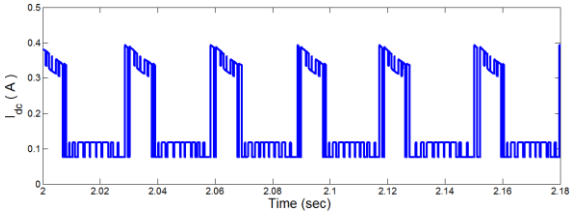

Fig 9: Input Current

D. *Diode current*

Figure 10 shows the current through the diodes. The maximum current is 0.16A during the charging period of capacitor, because capacitor is charged through input source, diodes D_1, D_2 and a common switch S_b. The maximum current through diode can be calculated using an expression (16)

$$I_{d\_max} = \frac{\Delta V_c}{r_d + r_s + ESR} \quad (16)$$

Where, ΔV_c is the ripple voltage across the capacitor
r_d is the diode internal resistance
r_s is the ON resistance of common switch
ESR is the equivalent resistance of capacitor.

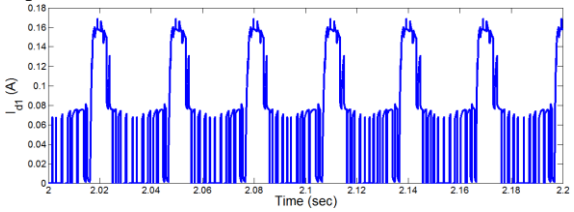

Fig 10: Current through Diode D_1

E. *Diode Voltage*

Figure 11 shows the voltage across the diode D_1. Diode D_1 experiences 0.8V forward drop and -3.4V reverse voltage with a high frequency switching due to the capacitor discharging periods.

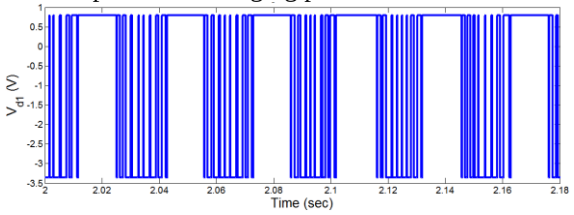

Fig 11: Voltage across Diode D_1

Figure 12 shows the voltage across the diode D_2. From the waveform forward diode drop is 0.8V and -2.6V reverse voltage and D_2 operates with ON – OFF states.

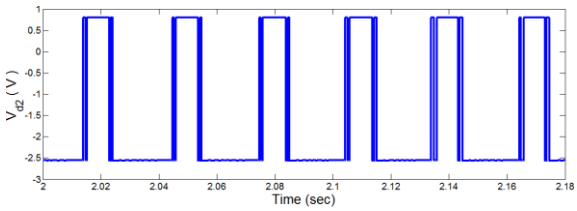

Fig 12: Voltage across Diode D_2

F. Voltage Stress across the Switches

Figure 13 shows the voltage stress across the seven switches using Alternative Phase Opposition Disposition PWM technique. From the simulation, voltage drop across the switches in the full bridge inverter is 11.8V. Voltage stress across switch $S_{a1}$is 4.2V and S_{a2} is 3.4V. For a common switch S_b is 7.6V.

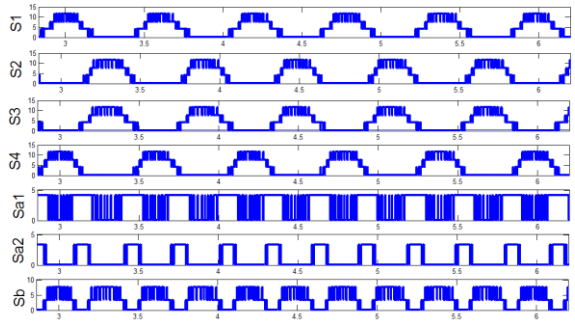

Fig 13: Voltage Stress of Switches

G. Capacitor Voltage

During S_{ai} turned ON, capacitor C_i (i = 1, 2....N) starts charging to a voltage equal to (V_{dc} - $2V_f$) through forward biased diodes. All the parallel connected capacitors are charged equally. In this work, V_{dc}= 5V and Forward diode drop, V_f = 0.8V means capacitor charged to 3.4V as shown in figure 14.

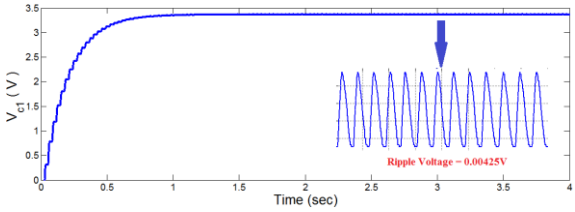

Fig 14: Voltage across Capacitor C_1

Capacitance ripple voltage from the simulation for C_1 is 0.00425V and from the calculation 0.00575V. The capacitor to be used should be such that it should retain the voltage specified (V_{dc} - $2V_f$).

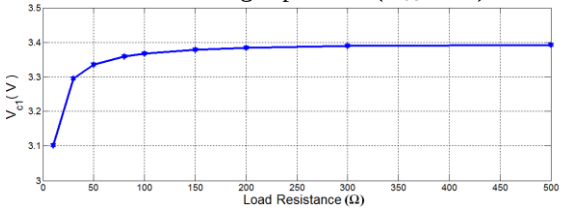

Fig 15: Voltage across Capacitor C_1Vs Load Resistance

Figure 15 shows the capacitor voltage with respect to load resistance. As the load resistance value increases capacitor charging accuracy increases for the same capacitance 100mF. So for the capacitor to charge up to the specified voltage, the resistive load must be greater than or equal to 100Ω shown in the figure 15.

H. Output Voltage and Output Current (R LOAD)

In seven level inverter output contains three steps. Figure 16 show the seven level output voltage using Alternative Phase Opposition Disposition PWM technique.

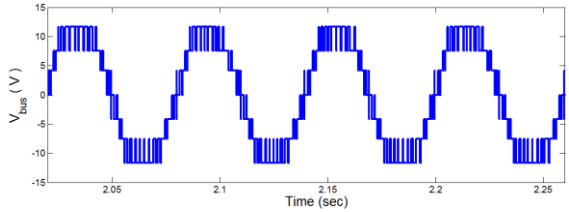

Fig 16: Output Voltage (R Load)

Figure 17 shows the Seven level output current of the inverter.

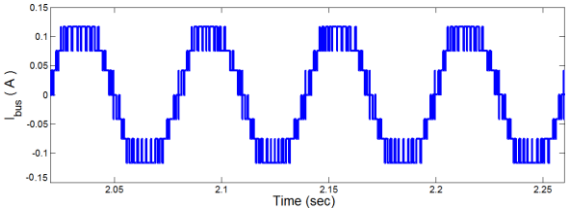

Fig 17: Output Current (R Load)

I. Resistive-Inductive load (RL LOAD)

Figure 18 and 19 shows the output voltage and current under R-L condition respectively. Resistive - Inductive Load (R-L) for 50 Hz output is 100 Ω and 138mH.

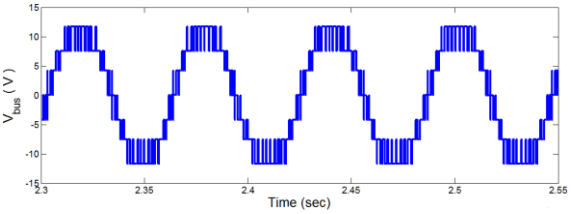

Fig 18: Output Voltage (RL Load)

So the minimum load must be 100Ω and 40mH by considering capacitor voltage and output current distortion. And also as the inductance in the load increases, load current reduces because total load impedance increases.

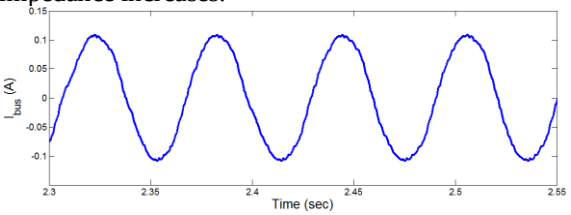

Fig 19: Output Current (RL Load)

J. Power Factor

It is cosine of the phase difference between output voltage and current. Also the fraction of total power (apparent power) which is utilized to do the useful

work called active power. For RL load current lags the voltage.

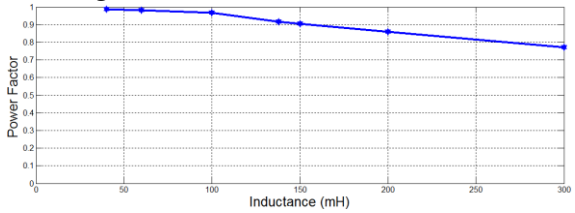

Fig 20: Power Factor Vs Load Inductance

For the minimum load inductance of 40mH power factor is 0.987 and for the simulated value of 138mH power factor is 0.917 shown in figure 20.

K. Filter Circuit

The capacitor-input filter, also called the π - filter due to its shape. A typical capacitor input filter consists of a filter or reservoir capacitor C_1, connected across the rectifier output, an inductor L, in series and another filter or smoothing capacitor, C_2, connected across the load, R. Assuming C_1=C_2=C,

$$\text{Capacitor, } C = \frac{1}{4\pi^2 L {f_c}^2} \quad (17)$$

Figure 21 shows the seven level inverter output voltage using the filter.

$$\text{Cut-off frequency, } f_c = \frac{1}{2\pi\sqrt{LC}} \quad (18)$$

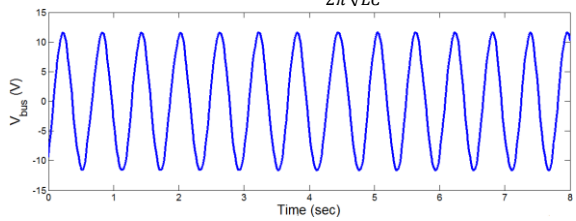

Fig 21: Filter Output Voltage

VII. GRID CONNECTED PHOTOVOLTAIC SYSTEM

In grid-connected photovoltaic system (GCPV), the grid inverter is crucial to convert the DC power which is generated from the photovoltaic (PV) arrays into the AC power to match with the grid voltage and frequency.

In practice, PV array is connected to a maximum power point tracker (MPPT) in order to allow the PV array to produce maximum power it is capable of. The produced DC power is then converted into AC power using inverter before delivered into the utility grid. But the major problem is in the DC-DC converter circuit. By using the conventional multilevel inverter the input must be large enough to produce the grid AC voltage. This is the main design criterion for the inductor and capacitor of the DC-DC converter. Proposed switched capacitor multilevel inverter is presented in this study acts as boosted DC-AC converter. So the input DC required to generate the grid voltage is less compared to other multilevel configuration and number of series connected module in the PV array can also be reduced. Thus size and capacity of PV array becomes minimized.

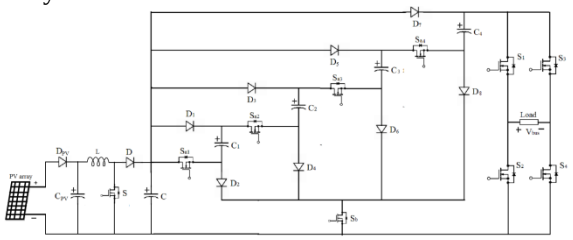

Fig 22: Eleven Level Switched Capacitor Inverter

Eleven level switched capacitor inverter is designed with four switched capacitor cells in parallel shown in figure 22. As the number of SC cell increases, the input required to produce particular output voltage is reduced. Thus the size of entire system minimized because boost converter design can be reduced. In order to generate 230V single phase supply, from the eleven level inverter 50V DC is required and using the seven level inverter 80V is required. Figure 23 shows the variation of different parameters such as number of SC cells, %THD and input voltage with the number of output levels for a constant 230V output voltage. Stress across the common switch S_b is the limiting factor for selecting the number of cells in the proposed inverter.

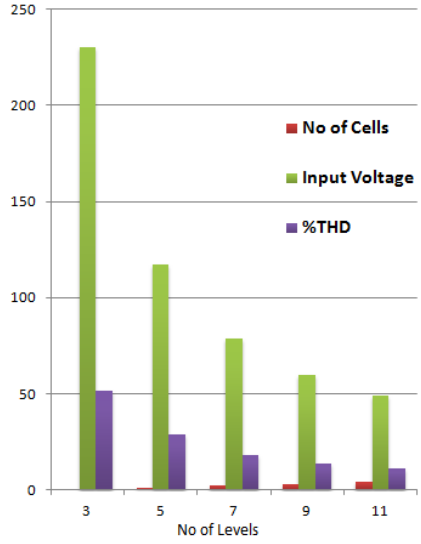

Fig 23: Parameters Vs Number of Output Levels

The three phase structure for a switched capacitor multilevel inverter can be implemented by combining three individual inverter blocks for each phase connected together. Three individual voltage sources of equal magnitude are required for each phase. Control for each phase is done individually depending on the modulation strategy used.

Number of switched capacitor cells increases the value of maximum output step and also reduces %THD. Using the eleven level inverter %THD is 10.93% without filter circuit shown in figure 24.

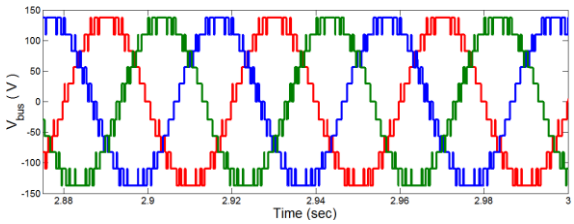

Fig 24: Three Phase Eleven Level Output Voltage

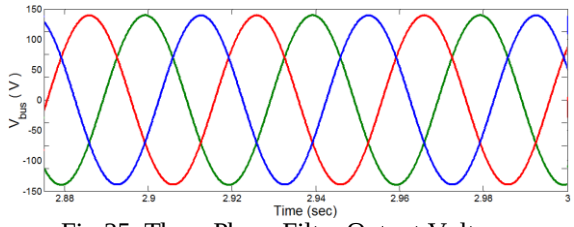

Fig 25: Three Phase Filter Output Voltage

VIII. EXPERIMENTAL SETUP AND RESULTS

Figure 26 shows the experimental setup of switched capacitors seven level inverter.

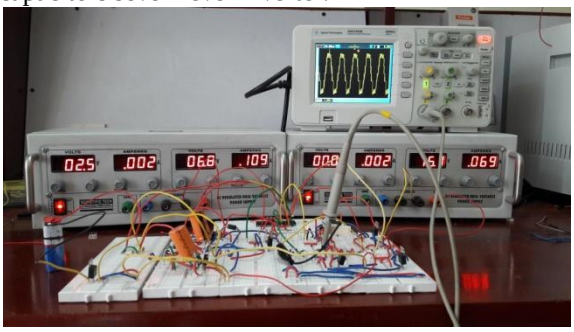
Fig 26: Experimental Setup of Seven Level Inverter

To control MOSFET (IRF540), pulses are created using PIC16F877A microcontroller based on Alternative Phase Opposition Disposition (APOD) modulation technique. These control pulses are amplified using an optocoupler TLP250 Driver/Optocoupler IC.

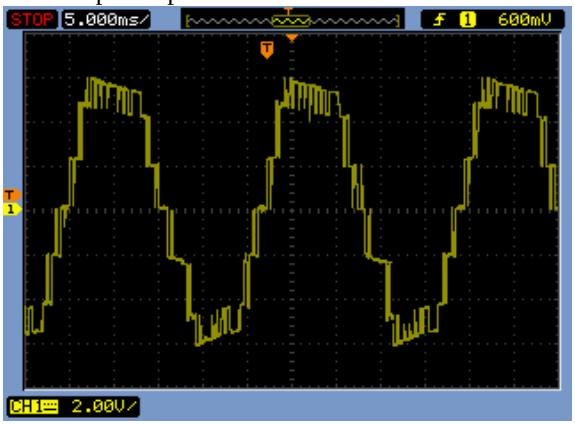

Fig 27: Experimental Result of Seven Level Inverter

Figure27 shows the seven level output voltage of the proposed inverter. For the hardware prototype, 1000µF capacitor and 100Ω, 5W load resistor is used. Since the capacitor charged to 2V, output is 50Hz staircase waveform having maximum output voltage of 6V with 5V DC input. With the same load, in order to increase the output voltage the value of capacitor must be increased.

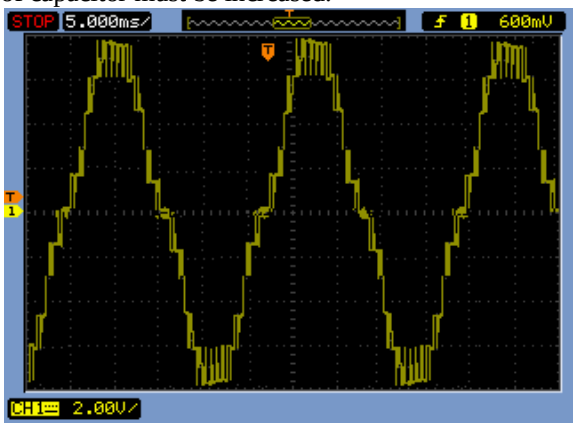

Fig 28: Experimental Result of Eleven Level Inverter

Figure 28 shows the eleven level inverter output voltage by cascading four SC cells.

IX. CONCLUSIONS

In this paper, step up switched capacitor multilevel inverter is studied, which is a combination of DC – DC converter and a full bridge inverter. This multilevel inverter uses very less number of switching devices compared to conventional inverters and existing switched capacitor multilevel inverters. Simplified method to generate simulation model for multicarrier PWM techniques based on various carrier signals and modulating signals are presented. Alternative Phase Opposition Disposition technique produces less THD among all the multicarrier PWM techniques. Operation and performance analysis of proposed inverter are studied with seven level inverter prototype. The efficiency of the inverter is studied based on the capacitor charged voltage. Eleven Level Inverter is designed and experimentally verified for Grid application.

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