Transformer Inrush Current Mitigation for Series Voltage Sag Compensator

Anil Kumar Pathak[1] Dr. A. K. Jhala[2] Pramod Kumar Rathore[3]
[1]M. Tech Department of Electrical & Electronics Engineering RKDF-CE, Bhopal (MP) India
[2]Associate Professor Department of Electrical & Electronics Engineering RKDF-CE, Bhopal (MP) India
[3]Assistant Professor Department of Electrical & Electronics Engineering RKDF-CE, Bhopal (MP) India

Abstract- *Manufacturing industries are located in industrial park. Survey results suggest that 90% of interruption at industrial facilities is related voltage sag. An inrush mitigation technique is proposed and implemented in a synchronous reference frame sag compensator controller. The voltage sag compensator is based on three phase voltage source inverter and a coupling transformer for serial connection. In various companies voltage sag may affect many manufactures and may reduce the efficiency of the system which results sufficient losses in the power system. It is the most cost effective solution against voltage sags. When voltage sag happen, the transformers, which are often installed in front of critical loads for electrical isolation, are exposed to the disfigured voltages and a DC offset will occur in its flux linkage. A transformer inrush may occur at the start of sag compensator. This over current may damage the inrush protection of the series connected inverter and the transformer output voltage is greatly reduced due the magnetic saturation. When the compensator restores the load voltage, the flux linkage will be driven to the level of magnetic saturation and severe inrush current occurs. The compensator is likely to be interrupted because of its own over current protection. This paper proposes an inrush current mitigation technique together with a state-feedback controller for the Voltage sag compensator.*

Keywords- SVPWM, Inrush current, Voltage sag compensator.

I. INTRODUCTION

To strengthen the power network stability by mitigating the power quality issues. The study shows how much work is done in the field of power quality and what can be done to increase reliability and stability.

The main objective of the dissertation can be grouped as follows-

- Balancing the active and reactive power in power system.
- To maintain voltage profile across power system by reducing the inrush current in the distribution system.
- Various methods and their effect on distribution system.
- To study the harmonic distortion due to various methods used for inrush current mitigation.

Problem Formulation: The Electrical Power System is a very large network in which number of power quality issues may occurs such as voltage sag/swell, harmonics, interruptions, transients, voltage fluctuation, noise, notching. In a power system different types of loads are connected across load side as well as source side of system. In survey it is found that most of the interruption at industrial facilities is voltage sag related. Voltage sag is a most infamous problem as it goes on affecting a large network.

As the power network, consist of large numbers of transformers which are affected by inrush current drawn due to sudden loading. Hence inrush current across the transformer also create the voltage sag which is not addressed in any voltage sag compensator. A system to mitigate the inrush current is required to minimize the voltage sag in the network. Hence proposed mitigation technique reduces the inrush current in distribution power system.

Work Methodology:

The dissertation will focus on the concept of mitigation technique of power quality issues (inrush current mitigation) and how they can be used to maintain the power distribution system reliability and stability.

- Simulation of inrush mitigation technique with series voltage sag compensator in MATLAB and its behavior when disturbances are applied on the system under critical load condition and also with different control technique PWM & SVPWM.
- Study of different control techniques used for mitigation.

- Simulation and implementation of mitigation technique with series voltage sag compensator in above simulation of test system.
- Analysis, performance and calculation of inrush mitigation technique with series voltage sag compensator for different as well as online and offline load conditions.

II. PROPOSED METHODOLOGY

When the grid is normal, the compensator is bypassed by the thyristors for high operating efficiency. When voltage sags occur, the voltage sag compensator injects the required compensation voltage through the coupling transformer to protect sensitive loads from being interrupted by sags. However, certain detection time (typically within 4ms) is required by the sag compensator controller to identify the sag event. And the load transformer is exposed to the. Deformed voltage from the sag occurrence to the moment when the compensator restores the load voltage. Also its short duration, the deformed voltage causes magnetic flux linkage deviation inside the load transformer, and magnetic saturation may easily occur when the compensator restores the load voltage, thus results in inrush current. The inrush current could trigger the over-current protection of the compensator and lead to compensation failure thus this paper proposes inrush mitigation technique by correcting the flux linkage offsets of the load transformer. This technique can be seamlessly integrated with the state feedback controller of the compensator.

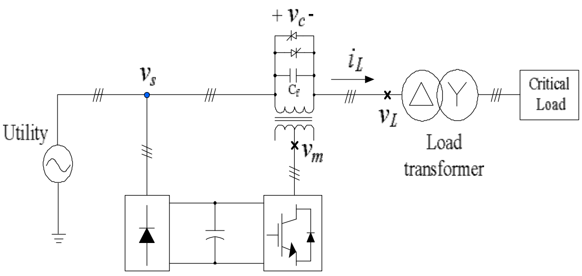

Fig. 1. Simplified One Line Diagram of the Off-Line Series Voltage Sag Compensator

- ***Generalization of the Proposed SVPWM Scheme for An `n' Level PWM Inverter:***

The SVPWM, proposed for a three-level inverter, can be easily extended to any n-level PWM generation. In the SPWM scheme for an n level inverter, the reference signals are compared with(n-1) level shifted carriers The triangular carriers and the reference signals, for an n-level PWM scheme, for n is odd, for n is even. The (n-1) triangular carriers are compared with reference phase voltages. A carrier index, I, is defined to designate the carrier regions in which the reference phase voltages lie during the sampling interval under consideration. When n is odd. The carrier index I for the top carrier is 1, and it increases in steps of 1 towards the bottom carriers. The carrier index I for the lowest carrier is equal to (n-1). During a sampling interval, the carrier indices, I_a, I_b and I_c (which can be from 1 to (n-1), for A, B and C phases, respectively, are determined depending on the carrier region in which the respective phase voltage lies. The determination of the time durations,$T_{a\ cross}$, $T_{b\ cross}$, and $T_{c\ cross}$.
When n is odd, can be generalized as

$$T_{a\_cross} = T_{as}^{*} + (I_a - \frac{n-1}{2}) * T_s \qquad (1)$$

$$T_{b\_cross} = T_{bs}^{*} + (I_b - \frac{n-1}{2}) * T_s \qquad (2)$$

$$T_{c\_cross} = T_{cs}^{*} + (I_c - \frac{n-1}{2}) * T_s \qquad (3)$$

When n is even, the triangular carrier & reference phase voltage, are as shown in this case, the reference phase voltage are centred on the middle triangular carrier. The determination of $T_{a\ cross}$, $T_{b\ cross}$, and $T_{c\ cross}$ can be generalized as

$$T_{a\_cross} = (\frac{T_s}{2}) + T_{as}^{*}(I_a - \frac{n-1}{2}) * T_s \qquad (4)$$

$$T_{b\_cross} = (\frac{T_s}{2}) + T_{bs}^{*}(I_b - \frac{n-1}{2}) * T_s \qquad (5)$$

$$T_{c\_cross} = (\frac{T_s}{2}) + T_{cs}^{*}(I_c - \frac{n-1}{2}) * T_s \qquad (6)$$

Space vector is employed as it is an advanced topology from the conventional PWM techniques. Space vector PWM technique is an advancement of sinusoidal PWM as the pulses produced by digital switching of the fundamental waveform. Considering six switch operation we divide the VSI into two parts as upper part and lower part. The upper part contain the switches S1 S3 & S5 leaving the lower part of the VSI with S2 S4 & S6.

TABLE 1. SWITCHING STATES

Switch	S_1	S_2	S_3
1st Mode	0	0	0
2nd Mode	0	0	1
3rd mode	0	1	0
4th Mode	0	1	1
5th Mode	1	0	0
6th Mode	1	0	1
7th Mode	1	1	0
8th Mode	1	1	1

The signal generation of space vector is compared to the triangular waveform to generate three PWM pulses to which NOT gates are given to get the other three pulses. The control signal of space vector PWM is given blow fig. 2

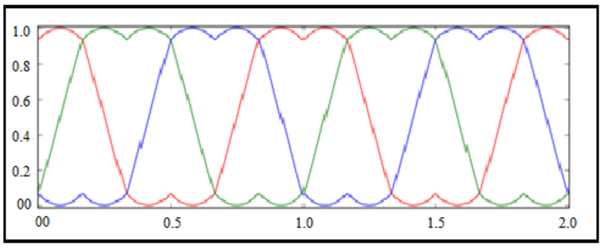

Fig. 2. Control signals of Space vector PWM

III. SYSTEM CONFIGURATION OF THE PROPOSED COMPENSATOR

The series compensator is consisted by a three phase voltage source inverter. The leakage inductor of coupling transformer L_f and capacitor C_f is recognized as the low-pass filter to suppress PWM ripples of inverter output voltage V_m. Fig. 3 shows the equivalent circuit of series voltage sag compensator and its dynamic equation can be expressed as,

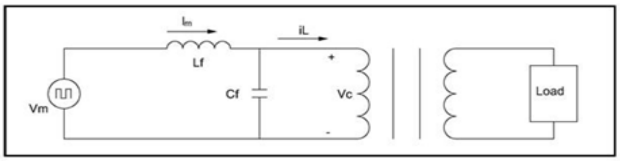

Fig. 3. Per phase equivalent circuit of the voltage sag compensator series

$$L_f \frac{d}{dt}\begin{bmatrix} i_{ma} \\ i_{mb} \\ i_{mc} \end{bmatrix} = \begin{bmatrix} v_{ma} \\ v_{mb} \\ v_{mc} \end{bmatrix} - \begin{bmatrix} v_{ca} \\ v_{cb} \\ v_{cc} \end{bmatrix} \quad (7)$$

$$C_f \frac{d}{dt}\begin{bmatrix} v_{ca} \\ v_{cb} \\ v_{cc} \end{bmatrix} = \begin{bmatrix} i_{ma} \\ i_{mb} \\ i_{mc} \end{bmatrix} - \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \quad (8)$$

Where $[v_{ma}\, v_{mb}\, v_{mc}]^T$ is the inverter output voltage, $[i_{ma}\, i_{mb}\, i_{mc}]^T$ is the filter inductor current, $[v_{ca}\, v_{cb}\, v_{cc}]^T$ is the compensation voltage, and $[i_{La}\, i_{Lb}\, i_{Lc}]^T$

$$\frac{d}{dt}\begin{bmatrix} i^e_{mq} \\ i^e_{md} \end{bmatrix} = \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix}\begin{bmatrix} i^e_{mq} \\ i^e_{md} \end{bmatrix} + \frac{1}{L_f}\begin{bmatrix} v^e_{mq} \\ v^e_{md} \end{bmatrix} - \frac{1}{L_f}\begin{bmatrix} v^e_{cq} \\ v^e_{cd} \end{bmatrix} \quad (9)$$

$$\frac{d}{dt}\begin{bmatrix} v^e_{cq} \\ v^e_{cd} \end{bmatrix} = \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix}\begin{bmatrix} v^e_{cq} \\ v^e_{cd} \end{bmatrix} + \frac{1}{C_f}\begin{bmatrix} i^e_{mq} \\ i^e_{md} \end{bmatrix} - \frac{1}{C_f}\begin{bmatrix} i^e_{Lq} \\ i^e_{Ld} \end{bmatrix} \quad (10)$$

IV. SIMULATION AND RESULTS ANALYSIS

- ***Simulation with proposed mitigation technique (PWM):***

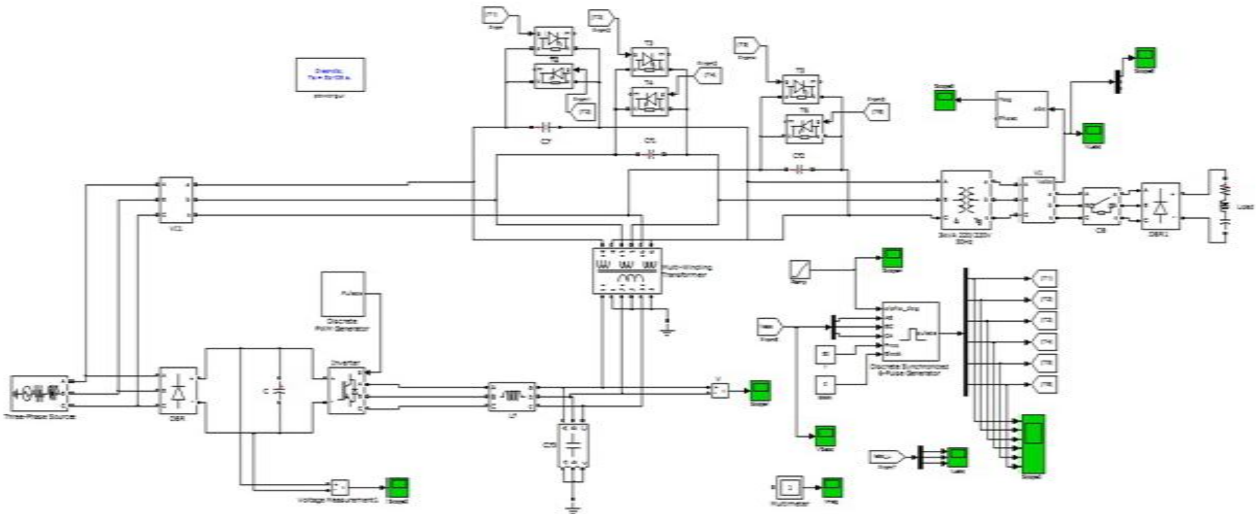

Fig. 4. Simulation model with mitigation technique (PWM)

- Output waveforms:

a) Source voltage

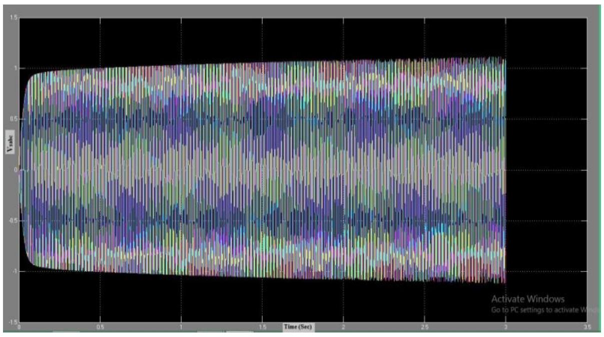

Fig. 5. Source voltage Waveform

b) Load Voltage

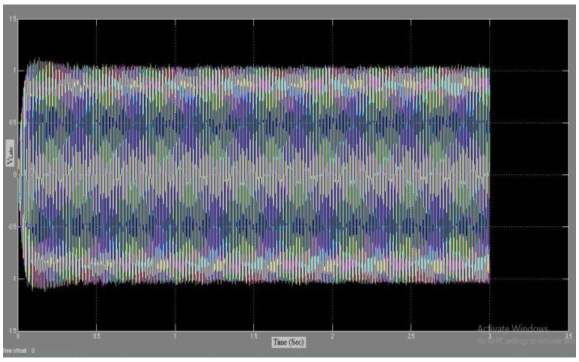

Fig. 6. Load Voltage Waveform

Fig. 5 shows the input source voltage waveform and Fig. 6 shows load voltage waveform which is get stabilized to normal value due to inrush mitigation technique.

C) Output load current

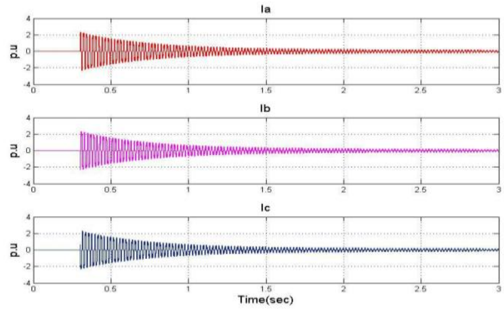

Fig. 7. Load Current waveform

D) Magnetic Flux of Load Transformer

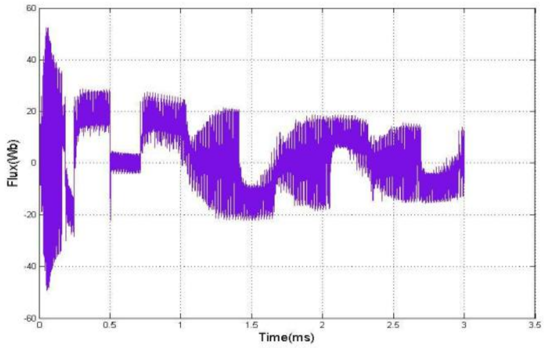

Fig. 8. Magnetic Flux Waveform

- ***Offline mitigation technique (SVPWM) :***

Fig. 9 shows the simulation model with inrush current with online mitigation technique with series voltage sag compensator in which space vector pulse width modulation (SVPWM) technique is used.

In offline mitigation technique at 0.3 sec load connected without compensator at 1 sec compensation on, from 1.5 to 2 sec load is disconnected, at 2 sec and 2.3 sec load 2 and 3 connected with compensation.

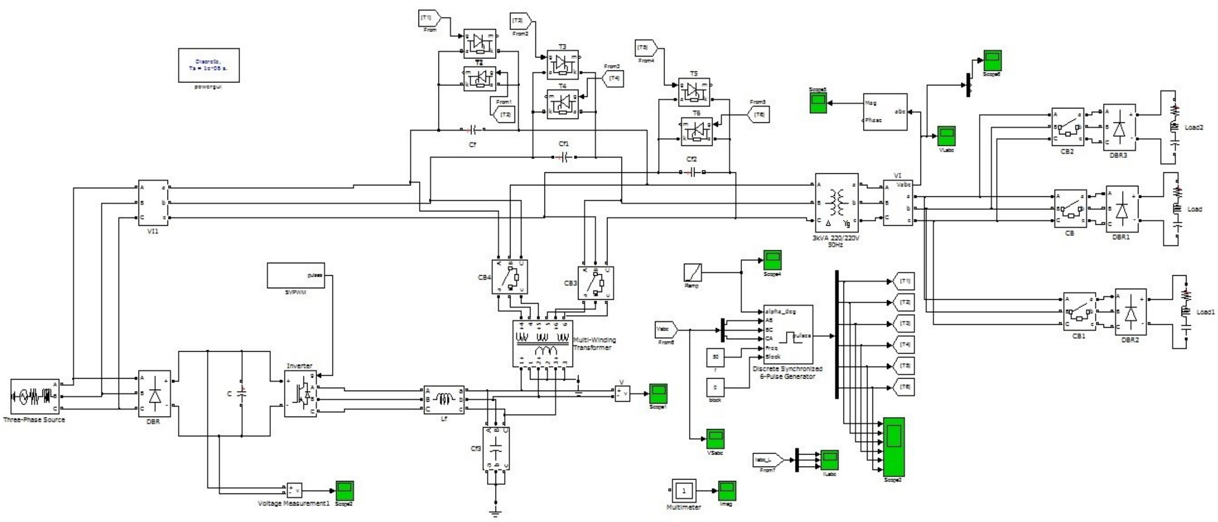

Fig. 9. Simulation model With Migration Technique (SVPWM)

A) Source voltage

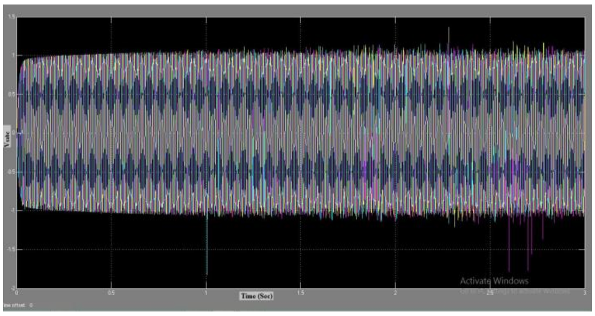

Fig. 10. Source voltage waveform

B) Load voltage

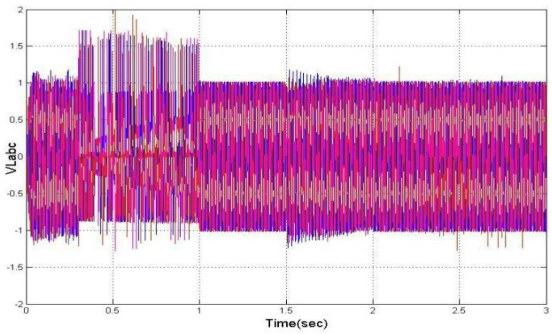

Fig. 11. Load Voltage Waveform

Fig. 10 shows the input source voltage waveform Fig. 11 shows the output load voltage waveform which is get stabilized to normal value due to inrush mitigation. At 0.3 sec load connected without compensation so load voltage waveform get disturb up to 1 sec where compensation on. After 1 sec waveform get stabilized.

c) Output load current

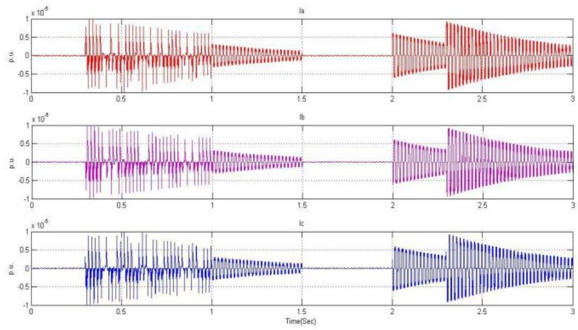

Fig. 12. Load Current waveform

d) Magnetic Flux of Load Transformer

As shown in magnetic flux waveform in Fig. 13 the flux linkage in load transformer increases due to voltage sag occurs by connection of critical load in system in which at 1 sec due to mitigation technique flux linkage in load transformer is reduced.

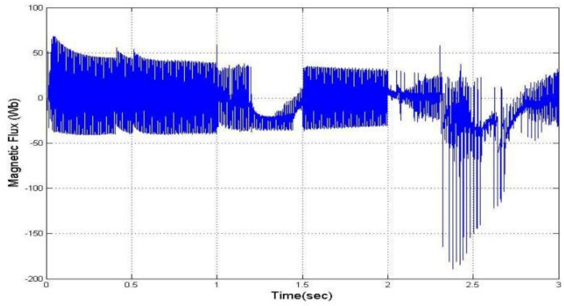

Fig. 13. Magnetic Flux Waveform

Harmonics Analysis:

TABLE 2 TOTAL HARMONIC DISTORTION ANALYSIS RESULT

Sr. No.	Mitigation Techniques	THD value
1	PWM Techniques	5.06%
2	SVPWM Techniques	3.54%

V. CONCLUSION

As the distribution system is connected with number of critical load, electronics load which are very sensitive load as change in supply occurs they get damage to avoid this need of mitigation of inrush current is required.

In this dissertation work, a new technique used for mitigation of transformer inrush current has been presented and simulated. A relative comparative study was done with and without mitigation techniques. The proposed technique based on the thyristor control pulse width modulation (PWM) and space vector pulse width modulation (SVPWM) control. SVPWM technique offers flexible control of output voltage as well as harmonic reduction. With the above topology in a simple test grid system with non-linear load the voltage profile of the system is maintained even in the different load condition also.

- We have studied, designed and simulate inrush mitigation technique of load transformer for series voltage sag compensator with different compensator technique and found that the SVPWM technique is better over PWM technique and system goes on improving the performance.
- We also have tested results for two different load condition and we can conclude that this technique can be used for different load conditions.
- We also have done graphical comparison of pulse width modulation (PWM) and space vector pulse width modulation (SVPWM) on the basis of total harmonic distortion (THD) and it is found that

SVPWM control technique offers less harmonic distortion as compare to PWM control technique. References

REFERENCES

[1] D. Sabin, An assessment of distribution system power quality, Elect. Power Res. Inst., Palo Alto, CA, EPRI Final Rep. TR-106249-V2, vol. 2, Statistical Summary Report, May 1996.

[2] C. J. Huang, S. J. Huang, F. S. Pai, Design of dynamic voltage restorer with disturbance-filtering enhancement, IEEE Transactions on Power Electronics, vol.18, pp.1202-1210, Sept. 2003.

[3] P. K. Lim, D.S. Dorr, Understanding and resolving voltage sag related problems for sensitive industrial customers, IEEE Power Engineering Society Winter Meeting, vol.4, pp.2886-2890, 2000.

[4] P. T. Cheng, C. L. Ni, J. M. Chen, Design of a state feedback controller for series voltage sag compensators, Power Conversion Conference, pp. 398-403, April 2007.

[5] Po-Tai Cheng An Inrush Mitigation Technique Of load Transformers For The Series Voltage Sag Compensator978-4244-1668-4/08/$25.00 2008 IEEE.

[6] Yogesh K Chauhan Bhavnesh Kumar and Sajid Ali.GBU Study and Performance of DVR for Voltage Quality Enhancement 987-1-4673-6150-7/13IEEE2013.

[7] Ajinkya M. Bhaware, 2M.F.A.R Satarkar Series Transformer Inrush Mitigation Technique during Change in Load for Distribution System Proceedings of 32nd IRF International Conference, 12th July 2015, Pune, India, ISBN: 978-93-85465-54-3.

[8] Venkatesh Dugyala, Ch.Nagalaxmi, V.K.R.Mohan Rao A Novel Control Strategy to Reduce Transformer Inrush Currents by Series Voltage Sag Compensator Science International Journal of Engineering Research and Development ISSN: 2278-067X, P-ISSN: 2278-800X,Volume 8, Issue 5 (August 2013), PP. 54-63.

[9] S.F. Torabi ,D. Nazarpour, Y. Shayestehfard Compensation of Sag and Swell Voltage using Dynamic Voltage Restorer (DVR) during Single line to Ground and Three phase faults ISSN 2077-3528 IJTPE Journal, September 2012.

[10] R.H. Salimin M.S.A .Rahim Simulation Analysis of DVR Performance for Volt-age Sag Mitigation the 5th International PEOCO 2011, Shah Alam , Selangor, Malaysai:6-7 June.

[11] Fawzi AL Jowder Modeling and Simulation of Dynamic Voltage Restore (DVR) Based on Hysteresis Voltage Control Member, IEEE. Apurva Kulkarni, Vinesh Choudhari, Rupesh Juware Mitigation of an Inrush Current of Power Trans-former by Using PWM-Inverter based Series Voltage Compensator.