Design of PI controller for seven level symmetrical MLI with minimal quantity of switches plus snubber circuit

R.Venkateswara rao[#1], K. Ramash Kumar*[2],V S N Narasimha Raju [*3]

[#]*PG Student & Department of Electrical & Electronics Engineering & Vishnu Institute of Technology (JNTUK),) Bhimavaram, Andhra Pradesh, India*

Abstract— *In the current days, multilevel inverters (MLIs) are very popular in industrial applications. The main problems of MLIs are large size (i.e. high cost) and high switching losses (i.e. voltage stress). In this article studies on a design and implementation of classical proportional integral (PI) controller for seven level symmetrical MLI (SLSMLI) with minimum number of switches plus snubber circuit. The classical linear proportional P controller is not able to regulate the output voltage of MLI particularly in larger line and load disturbances. In order to regulate the output voltage, minimize the switching losses, reduce the size and cost of MLI, a PI controller for seven levels symmetrical MLI with reduced quantity of switches plus snubber circuit (SC) is designed. Here, inverted sine carrier variable frequency (ISCVFPWM) technique is used to generate the PWM pulses for designed MLI switches. The performance of designed model is investigated at different working states by making the MATLAB/Simulink model in comparison with P controller. The simulation results of designed MLI have produced minimized total harmonic distortion (THD), excellent output voltage/output current regulations and good power factor.*

Keywords— *Multilevel inverter, Carrier Based PWM, MATALAB/Simulink, Snubber Circuit*.

1. Introduction

In current days, many topologies of Multi Level Inverters (MLIs) are developing very fast and most popular for many applications such as renewable sources, industrial drives, high voltage applications, blowers, fans, conveyors and battery operated car vehicles etc., [1]. The initial stage of multi-level starts with the three level inverter. Later on three main topologies of MLIs are designed namely Diode-Clamped MLI (DCMLI), Flying Capacitor MLI (FCMLI) and cascaded H bridge MLI [2]. Among this topology, cascaded H Bridge MLI has no need of flying capacitor or clamping diode but it need separate DC source only. The cascaded H Bridge MLI voltage imbalance is absence. Therefore, this topology more fit for renewable energy source applications.

The MLIs are regulated by modulation techniques (MTs) [3]. Generally, MTs are classified based on the switching frequency and again it has two types namely high frequency and low frequency. Commonly, high frequency carrier based sinusoidal pulse with modulation (SPWM) is most famous method, whereas the low frequency space vector modulation (SVM) is most popular for three levels MLI.

According to industrial application, need more number of MLIs that can lead to large size, more total harmonic distortion (THD), more number of switches, high initial cost and more switching losses. In order to reduce such problems, many reduced switches based MLI topologies has been designed and reported [4-5]. The seven-level MLI with minimum number of switches is well addressed in [6]. However, this article done only for simulation study of designed MLI without filter and controller design.

The verifications of the inverted sine pulse width modulation (PWM) techniques for symmetric MLI is reported in [7]. From this article, filter and controller designs have not been developed. The seven levels symmetrical MLI with small number switches is deigned [8]. However, filter and controller design is major gap for this article. The classical linear proportional integral (PI) controller for various MLI topologies has been executed in [9]. Main function of the controller to regulate the MLI output voltage.

From the above survey, it is clearly observed that design of PI controller plus snubber circuit for seven-level symmetrical MLI (SLSMLI) with reduced switches has not been developed. Therefore, in this article is to design the PI controller plus snubber circuit for symmetrical seven MLI with minimal number of switches. The PI controller parameters are derived with help of the Ziegler Nicholas Tuning Method. The performance designed model is verified at different operating conditions by making the MATLAB/Simulink software platform.

2. OPERATION OF SEVEN LEVEL SYMMETRICAL MLI

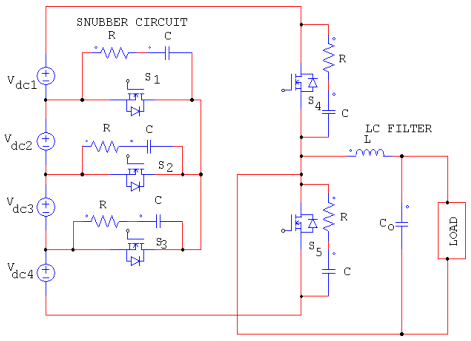


Fig.1: Topology of seven levels MLI.

The topology of SLSMLI with reduced switches is depicting in **Fig. 1**. It consists of four voltage sources like Vdc1, Vdc2, Vdc3, Vdc4, five MOSFET switches (S1 to S5), filter circuit, snubber circuit and loads. The designed topology has no H-bridges which can lead to reduce the number of switches. From this SLSMLI, three switches are used for generating the level output voltage whereas the remaining two switches are used for polarity changing. The generalized expression for output voltage of this topology is m= (2*n-2) or m= (2*V-1), Where, n is the number of switches and V is the number of voltage sources. The main merits of the designed SLSMLI are low ON/OFF losses, minimum THD, proficient power factor, good efficiency and producing pure sinusoidal output voltage in comparison with the conventional MLI topologies. The working and switching level of SLSMLI are detailed in Table 1.

Table 1. Switching operations of designed SLSMLI

Sl.no	S1	S2	S3	S4	S5	Output voltage
1	OFF	OFF	ON	OFF	ON	+1Vdc
2	OFF	ON	OFF	OFF	ON	+2VdC
3	ON	OFF	OFF	OFF	ON	+3Vdc
4	OFF	OFF	0FF	OFF	OFF	0
5	ON	OFF	OFF	ON	OFF	-1Vdc
6	OFF	ON	OFF	ON	OFF	-2Vdc
7	OFF	OFF	ON	ON	OFF	-3Vdc

2.1. Inverted Sine Carrier Variable Frequency PWM

There are many modulation strategies are used to required outputs from MLIs. As per the MLIs modulation technique concern, the carrier based strategies of modulating techniques has produced controlling ability for it. As our requirement (n levels at the output) of output levels multi carrier PWM strategies are used for designed SLSMLI. In this article inverted sine carrier variable frequency (ISCVFPWM) is used for required variation in amplitude and frequency.

In general, the amplitude modulation index is defined as

$$Ma=2Am/(m-1)Ac \quad (1)$$

Where,

m - no. of output levels,

Am-Amplitude of reference wave, Ac-Amplitude of carrier wave,

$$\text{Frequency ratio, } mf=fc/fm \quad (2)$$

Where,

Fc-carrier wave frequency

Fm –reference wave frequency

The ISCVFPWM strategy is applied two different frequency's f1 and f2.The remaining three carriers are having same frequency and same peak to peak amplitude (Ac). The carrier wave frequency values are f1=500Hz and f2=1000Hz. The reference wave placed at middle of the carrier waves are shown in Fig.2.

The SLSMLI with carrier over lapping technique, m-l carriers with the same frequency f_c and same peak-to-peak amplitude Ac are disposed such that the bands they occupy overlap each other; the overlapping vertical distance between each carrier is Ac/2. The reference waveform has amplitude of Am and frequency of fm and it is centered in the middle of the carrier signals. The reference wave is continuously compared with each of the carrier signals. If the reference wave is higher than a carrier signal, then the active devices corresponding to that carrier are switched ON. Else, the devices switch OFF. The amplitude modulation index ma and the frequency ratio mf are defined in the carrier overlapping method is expressed as (3)

$$ma = Am/((m/4)*Ac) \quad \text{and} \quad mf = fc/fm \quad (3)$$

In this paper seven level MLI generating by using **six carrier signals (Fc-50Hz ,Mc-0.3)** and one reference waveform (Fr-50Hz,mr-0.8) is show in fig-2

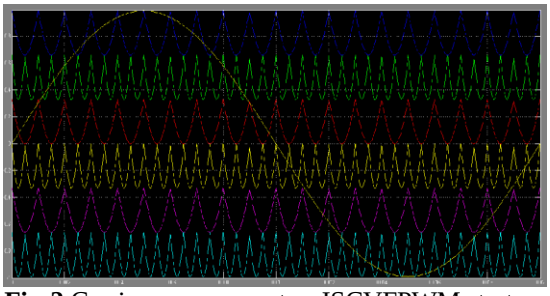


Fig-2 Carrier arrangement or ISCVFPWM strategy with sinusoidal reference wave (ma=0.8)

3. Design of LC Filter

Power quality and grid integration, a pure sinusoidal voltage-current waveform is necessary. For such reason a design of various filters are necessary. Filters have property to smooth current and voltage waveform. Many filters available in electronic systems like LC, RL, RLC filters etc. This paper proposes filter design guideline for L-C filter with Mosfet based multi-level inverter. The basic LC filter is show in Fig-3. An L-C circuit used at the inverter output for filtering purposes and ensuring that the THD is lower. The L-C filter cancels all harmonics and pure sinusoidal output voltage and current is obtained.The load current flows differently depending on the kind of loads such as linear and nonlinear load. Therefore it is difficult to represent the transfer function of inverter output voltage to load current. The plant composed of L-C low-pass filter satisfies linear property, so it is possible to represent the system which has two inputs of inverter output voltage and load current. LC Filter with the closed relation between the filter capacitor value and the system time constant, the capacitor value can be calculated. The effect of the load current to the voltage distortion can be calculated from the closed form**.**

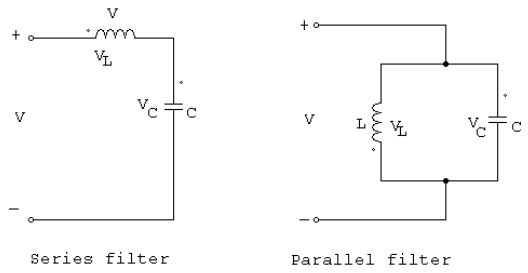


Fig-3 Basic LC filter designing

3.1 Mathematical modeling:

This filter consists of two unknown components, L and C, and the load is linear or non-linear loads. The transfer function of LC filter designing is show **fig-4.**

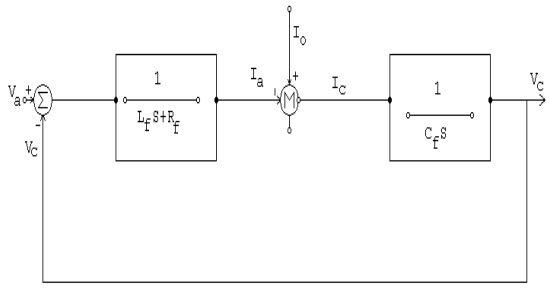


Fig-4 Block diagram of single phase PWM-VSI

The transfer function of single phase PWM-VSI is

$$V_C(s) = \frac{1}{L_f C_f S^2 + J R_f C_f} V_a(s) - \frac{1}{L_f C_f S^2 + J R_f C_f} I_a(s) \quad (4)$$

To determine the transfer function:

$$V_a(s) - SL_f I_a(s) - R_f I_a(s) - V_c(s) = 0 \quad (5)$$

$$V_a(s) - V_c(s) = I_a(s)\,(SL_f - R_f) \quad (6)$$

$$\frac{V_a(s)}{V_c(s)} = 1 + \frac{I_a(s)\,(SL_f - R_f) SC_f}{I_c(s)} \quad (7)$$

As $I_a = I_c + I_o$ (8)

$$I_a(s) = I_c(s) + \frac{V_c(s)}{Z_L} \quad (9)$$

$$\frac{I_a(s)}{I_c(s)} = 1 + \frac{1}{SC_f Z_L} \quad (10)$$

$$\frac{V_a(s)}{V_c(s)} = 1 + \left(1 + \frac{1}{SC_f Z_L}\right)(SL_f - R_f)\, SC_f \quad (11)$$

$$\frac{V_a(s)}{V_c(s)} = \frac{L_f C_f S^2 + SL_f + R_f C_f S Z_L + R_f + Z_L}{Z_L} \quad (12)$$

$$\frac{V_c(s)}{V_a(s)} = \frac{Z_L}{L_f C_f S^2 + SL_f + R_f C_f S Z_L + R_f + Z_L} \quad (13)$$

Now, through transfer function we can find the step response, corner or cross over frequency from bode plot and stability from root locus method.

The above equation can be simplified by neglecting the imaginary part in both the terms as equivalent series resistance of inductor is very small that means

$$(1\text{-}L_f C_f \omega^2) \ggg (R_f C_f \omega) \quad (14)$$

So,

$$V_c(j\omega) = \frac{1}{1 - L_f C_f \omega^2} V_a(j\omega) \quad (15)$$

$$\frac{V_c(j\omega)}{V_a(j\omega)} = \frac{1}{1 - L_f C_f \omega^2} \quad (16)$$

In the conventional output filter design method, the load current is treated as the disturbance so it can be neglected.

The filter output to input voltage harmonics must be less than 3%

So,

$$\frac{V_c(j\omega)}{V_a(j\omega)} = 3\% \quad (17)$$

$$\frac{1}{1 - L_f C_f \omega^2} = 3\% \quad (18)$$

$$\frac{1}{f^2 \frac{X_L}{X_C} - 1} \leq 0.03 \quad (19)$$

$$\frac{X_L}{X_C} \geq \frac{34.2}{f^2} \quad (20)$$

Where, f=corner or cutoff frequency

So, the above processes we can find out the L and C for the filter.

4. Snubber circuit designing:

The drawback of MLI is it generating more voltage spikes in this condition doesn't possible power quality and generating pure sinusoidal wave etc. so necessary for avoiding this voltage spikes.

Snubber circuits are needed to limit the rate of change in voltage or current (di/dt or dv/dt) and over voltage during turn-on and turn-off. There are many kinds of snubbers like RC, diode and solid state snubbers but the most commonly used one is RC snubber circuit. This is applicable for both the rate of rise control and damped. This circuit is a capacitor and series resistor connected across a switch (thirstier). For designing the Snubber circuits is

$$I_{PK} = \frac{V_0}{R_s} \quad (21)$$

$R_s =$ snubber resistance

$V_0 =$ open circuit voltage

From the snubber circuit

$$I_{PK} = C\frac{dv}{dt} \quad (22)$$

Substituting (1) into (2)

$$\frac{dv}{dt} = C\frac{V_0}{R_s} \quad (23)$$

The energy stored in the capacitor is

$$E = \frac{1}{2}C(V_0)^2 \quad (24)$$

The snubber resistance is equal to

$$R = \frac{V_0}{I} \quad (25)$$

I = switching current

V_0 = open circuit voltage

The amount of energy the snubber resistance is to dissipate is the amount of energy stored in the snubber capacitor. It is recommended that you choose a capacitance value that causes the resistor to dissipate one half the wattage rating of the resistor.

$$P = \frac{1}{2}C(V_0)^2\,2f \quad (26)$$

f = switching frequency

$$P = C(V_0)^2 f \quad (27)$$

$$C = \frac{P}{(V_0)^2 f} \quad (28)$$

The above process calculate the snubber circuit R & C values

5. Design of PI Controller:

Fig. 5 shows the complete structure of SLSMLI with classical PI controller. The output voltage of the system is measured and compared with its reference output voltage that gives the error signal. This error signal is processed through the PI controller to generate the control signal. This control signal is compared with the repeating sequence signal to generate the gating pulses, which in- turn regulates the output voltage of the SLSMLI. PI controller parameters, proportional gain (K_p) and integral times (T_i), are obtained by using Zeigler – Nichols second tuning method (trial and error method). The values proportional gain K_p = 11 and integral time T_i=0.05s.

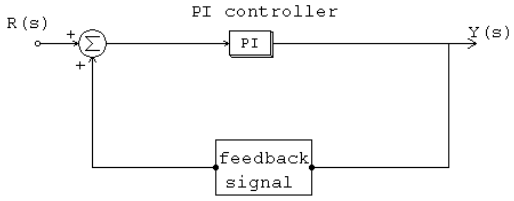


Fig-5 Basic block diagram of PI controller

6. Simulation Results and Discussion

Table.1Specifications of SLSMLI.

Parameter	*Value*	*Unit*
Switching frequency (Fs)	500	KHZ
DC source voltage (V_{dc})	10	Volts
Rated output voltage	40	VP-P
Rated output frequency	50	HZ
Rated output current	10	Ap-p
Rated load	10	OHM
Filter inductor (Lf)	3	mH
Filter capacitor (Cf)	1000	nF

Table. 2 Different load THD values of with /without filter and power factor.

Loads	**THD** (Without filter)	**THD** (With filter)	**P.F**
Resistance(R)	45.52	5.882	0.994
Resistance & Inductance (RL)	36.79	10.40	0.835
Non-linear	36.08	4.29	0.825

Table.3 Different load THD values of with/without snubber circuit with filter.

Loads	THD (Without snubber)	THD (With snubber)
Resistance(R)	9.72	5.882
Resistance & Inductance (RL)	17.79	10.40
Non-linear	22.24	4.29

The performance of designed SLSMLI with/without snubber circuit using controller is catloged in Tables 2 and 3. From these results, it is found that the designed model has showed good performance over wihout snubber circuit.

Case (i): R-load with snubber circuit:

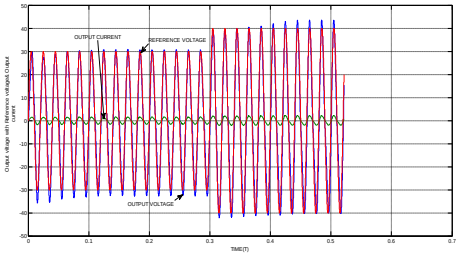


Fig.6 Simulated output voltage , output current and refernce output voltage of SLSMLI with filter and snubber circuit using PI controller.

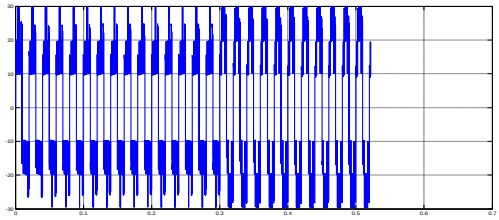
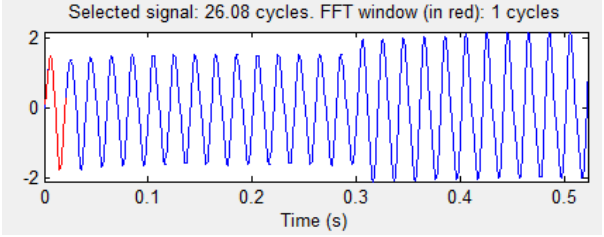


Fig.7 Simulted output voltage of SLSMLI without LC filter usinf PI controller in set point output voltage.



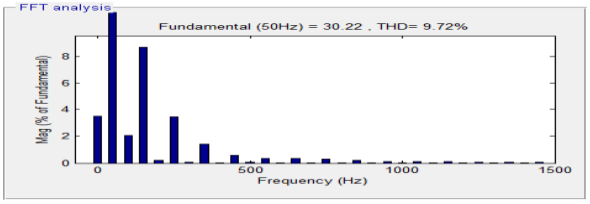


Fig.8 simulated the output voltage THD spectrum analysis of SLSMLI R-load without snubber circuit.

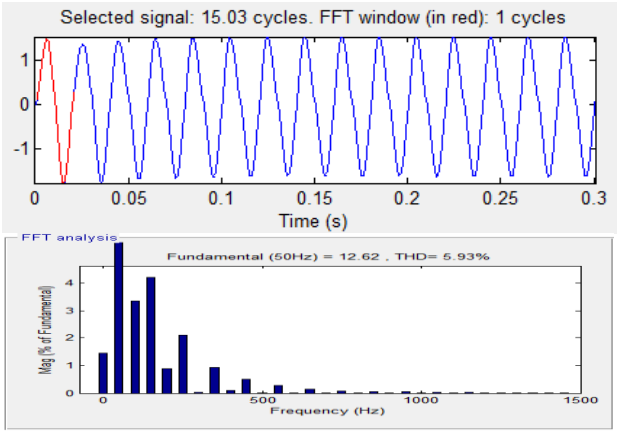


Fig.9 simulated the output voltage THD spectrum analysis of SLSMLI R-load with snubber circuit.

Case (ii): R-L LOAD WITH SNUBBER CIRCUIT

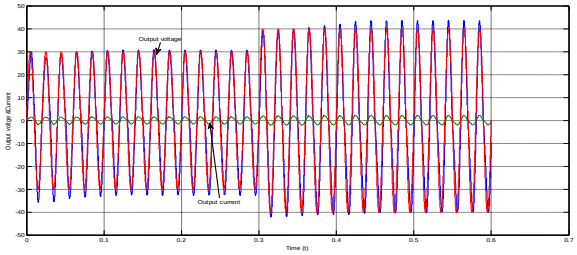


Fig.10 Simulated output voltage , output current and refernce output voltage of SLSMLI with filter and snubber circuit using PI controller.

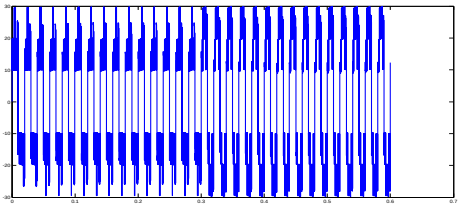


Fig.11 Simulted output voltage of SLSMLI without LC filter usinf PI controller in set point output voltage.

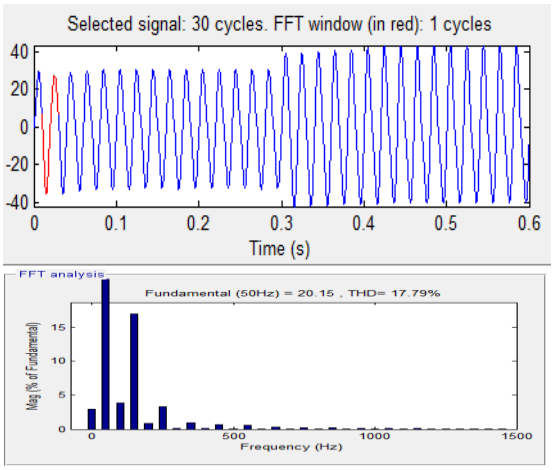


Fig.12 simulated the output voltage THD spectrum analysis of SLSMLI RL-load without snubber circuit.

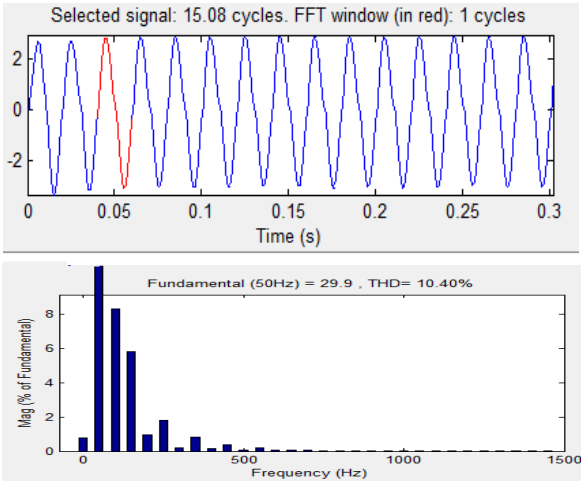


Fig.13 simulated the output voltage THD spectrum analysis of SLSMLI RL-load with snubber circuit.

Case (iii): Nonlinear load with snubber circuit:

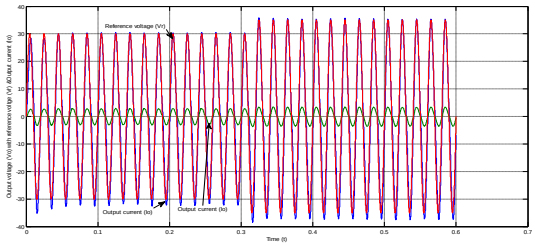


Fig.14 Simulated output voltage , output current and refernce output voltage of SLSMLI with filter and snubber circuit using PI controller.

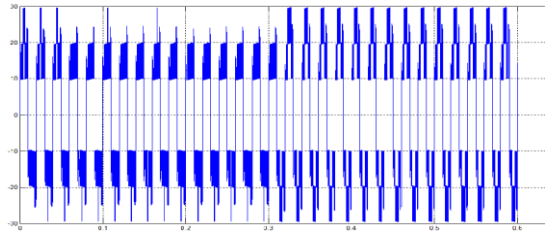


Fig.15 Simulted output voltage of SLSMLI without LC filter usinf PI controller in set point output voltage.

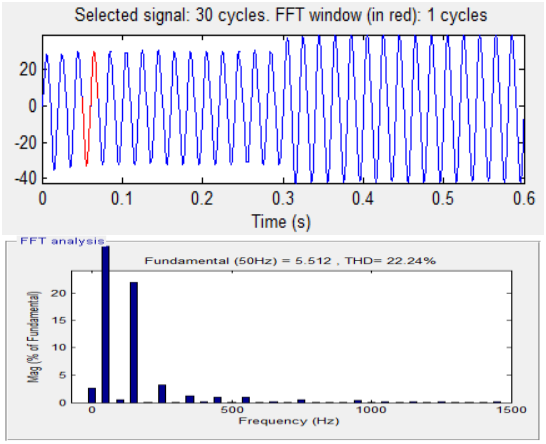


Fig.16 simulated the output voltage THD spectrum analysis of SLSMLI Nonlinear load without snubber circuit.

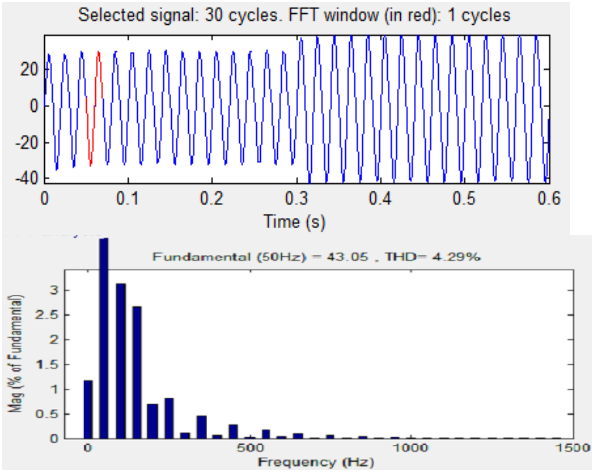


Fig.17 simulated the output voltage THD spectrum analysis of SLSMLI Nonlinear load with snubber circuit.

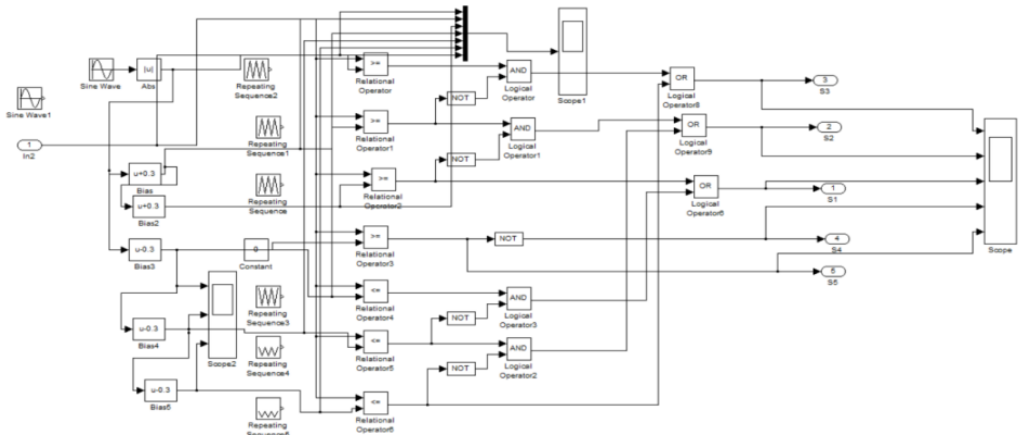


Fig. 18 MATLAB/Simulink PWM pattern for designed MLI.

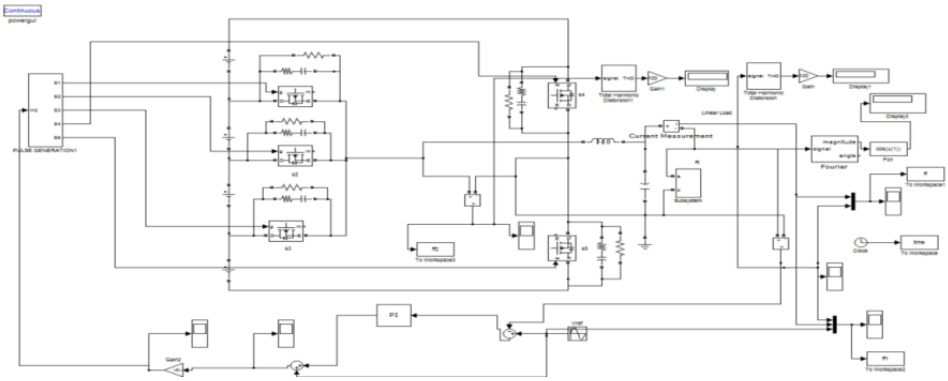


Fig.19 MATLAB/Simulink PWM pattern for designed MLI using PI controller.

From Fig.1 to Fig 17 shows the simulated output voltage, current and THD analysis of designed MLI fed different loads (LC filter) with/without snubber circuit using controller. From these figures, it evident that the output voltage and THD of designed MLI using controller has produced excellent performance at load conditions. Fig.18and19 show the MATLAB/Simulink model of the designed model.

Conclusion

The snubber circuit design based SLSMLI with ISCVFPWM has been successfully demonstrated using MATLAB/Simulink software platform. The performance of the designed SLSMLI with ISCVFPWM with and without snubber circuit is tested at different loads. Many results are presented to show the efficacy of the designed system particularly in snubber design. Also, THD analysis for SLSMLI with ISCVFPWM at different loads is studied and also it produced less THD for designed MLI with snubber circuit. The output voltage of SLSMLI with ISCVFPWM is regulated by using PI controller. The set point tracking is also carried out for the designed MLI using PI controller. The THD value of snubber based SLSMLI with ISCVFPWM using controller has produced very less over without snubber circuit. It can be more suitable for industrial drives, textile mills and centrifugal pumps etc,

References

[1] D. Mohan and S. B.Kurub, "Performance analysis of SPWM control strategies using 13 level cascaded MLI," in IEEE International Conference on Advances in Engineering Science & Management (ICAESM'12).

2. T. V. V. S. Lakshmi, N. George, S. Umashankar, and D. P. Kothari," Cascaded seven level inverter with reduced number of switches using level shifting PWM technique," International Conference on Power, Energy and Control(ICPEC'13),pp.676– 680,February2013.

3. J. Rodr´iguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, andapplications,"IEEETransactionsonIndustrialElectronics, vol.49, no.4, pp.724–738, 2002.

4. O.L.Jimenez, R.A.Vargas, J.Aguayo, J.E.Arau, G.Vela, and A.Claudio, "THD in cascade multi-level inverter symmetric and asymmetric," in Proceedings of the IEEE Electronics, Robotic sand Automotive Mechanics Conference (CERMA '11), pp. 289–295, November2011.

5. P.PalanivelandS.S.Dash, "Analysis of THD and output voltage performance for cascaded multilevel inverter using carrier pulse width modulation techniques," IET Power Electronics, vol. 4, no.8, pp.951–958, 2011.

6. Babaei and S. H. Hosseini, "New cascaded multilevel inverter topology with minimum number of switches," Energy Converse. Manage, vol. 50, no. 11, pp. 2761–2767, Nov. 2009.
7. Gregory, D. Patangia, H. "A Novel Multilevel Strategy in SPWM Design‖ Industrial Electronics," IEEE International Symposium, ISIE 2007, pp.515-520.