Design of a Capacitor-less Low Dropout Voltage Regulator

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Abstract **-** *With the growing need of battery powered mobile devices, power management has been of great concern in the electronics industry, an essential component being a low drop-out (LDO) voltage regulator. LDO voltage regulators improve battery's power efficiency and life. The designed LDO voltage regulator is designed with self-compensated error amplifier, along with PMOS current sourcing for quick charging and discharging at the output node. It provides a stable regulated output voltage in the range of 40-45mV with a dropout voltage of 200mV. Simulated results demonstrate that the proposed LDO voltage regulator has power consumption of 10.78uW thereby, reducing the power consumption by 30.18% which makes it more economic for power management architectures.*

Keywords-*LDO;drop-out; PMOS current sourcing; Kickback effect.*

I. INTRODUCTION

There has been a rapid increase in the demand of efficient and compact power management systems owing to the growth in electronics industry. The circuits are desired to operate such that they consume minimum amount of power, lower values of standby current, lesser area, lower pin count henceforth improving the battery life and making it more reliable for low voltage low power management solutions. Hence, making it optimal to be implemented on system-on-chip (SoC) [6]. Thus in achieving high level of integration thereby accounting for manufacturing of cost effective devices.

Low power low dropout regulators form an essential part of the power management system providing constant voltage supply along with improved power efficiency and fast transient response.LDO voltage regulator produces constant, stable and regulated voltage supply. It consists of an error amplifier followed by a Pass Transistor and a Current feedback amplifier. Power and noise cancellation is formed by rail to rail output stage of the Error Amplifier. It reduces the size of the Pass transistor. Due to this reduction LDO regulators lead to an area efficient chip.

LDO voltage regulator is used in portable electronic devices because it converts the unregulated input supply voltage to a stable supply voltage with very low dropout voltage because of which it has received attention in the recent years [1]. Portable electronic circuits should operate with minimal power consumption driving for low power solution in wide applications. The LDO voltage regulator has better efficiency at the cost of jeopardizing so it is the most popular linear regulator. The proposed paper highlights the development of an area efficient LDO voltage regulator which primarily focuses on a capacitor free LDO for advanced integration of CMOS chip power controlling[12]. As power is a basic constraint in portable electronic devices as it is responsible for the quality and runtime, hence the LDO voltage regulator is a vital module which offers low noise and low power consumption. The drop out voltage is defined as the input to output difference voltage where the control loop starts regulating. The operation of the circuit depends on feeding back the amplified error signal used to control the output current flow of the pass transistor which is driving the load. Section II and III describe the architecture of the existing LDO voltage regulator, section IV describes the architecture of the proposed LDO regulator. The simulation results have been discussed in section V.

II. LDO REGULATOR

Classification of low dropout regulators can be made as either low power or high power. Low power LDO voltage regulator have a maximum output current of less than 1A which makes them suitable for portable applications. Whereas, high power LDO voltage regulator give a current equal to, or greater than 1A which find application in automotive and industrial purposes. LDO voltage regulator has the capability to produce regulated voltage with very low dropout voltage. A low dropout regulator is a circuit that provides dc regulation of voltage even when the difference between input and output voltages is very less

[4]. The dropout voltage is defined as the minimum voltage required across the regulator to maintain the regulation.

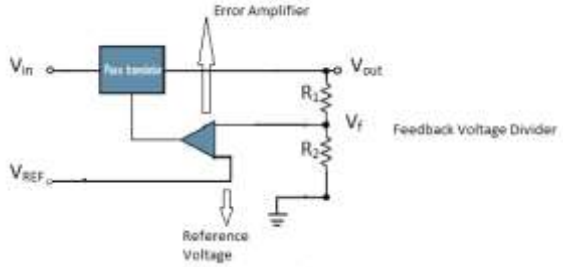

Fig 1. A conventional LDO voltage regulator

The conventional LDO voltage regulator, as shown in Fig. 1, comprises of Error amplifier, Pass element (pass transistor logic), along with a voltage divider feedback. Output of the LDO voltage regulator is controlled by pass transistor which is in turn controlled by the error amplifier. The job of error amplifier is to compare the reference voltage V_{REF} with the feedback voltage from the output and amplify the difference between these two signals. If $V_f < V_{REF}$ then output V_{out} is increased by the pass transistor and if $V_f > V_{REF}$ then the output is decreased.

III. SCHEMATICOF LDO VOLTAGE REGULATOR(EXSISTING)

A. Error amplifier

The block diagram of error amplifier, as shown in Fig. 2, mainly comprises of a preamplifier stage, followed by latch stage. In the preamplifier stage, the input signal is amplified in order to improve the sensitivity of the comparator and to prevent the kickback effect.

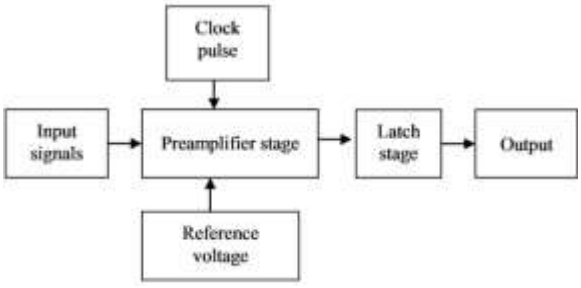

Fig. 2. Block diagram of Error Amplifier

The next stage is the latch stage which amplifies the difference between the two input signals. Kickback effect is observed when high voltage level variations at regeneration nodes are coupled to the input of the comparator through parasitic capacitance, the voltage level of the input signal gets disturbed [3]. Kickback effect can be reduced by neutralization technique which is applicable to those circuits whose differential inputs are directly connected to regenerative nodes. The disturbance is caused by parasitic capacitance C_{gd}. Hence adding a capacitor of the same value between the drain and bulk would cancel the effect of noise. Another alternative is inserting sampling switches, and reducing the voltage swing at the drain of the input transistor.

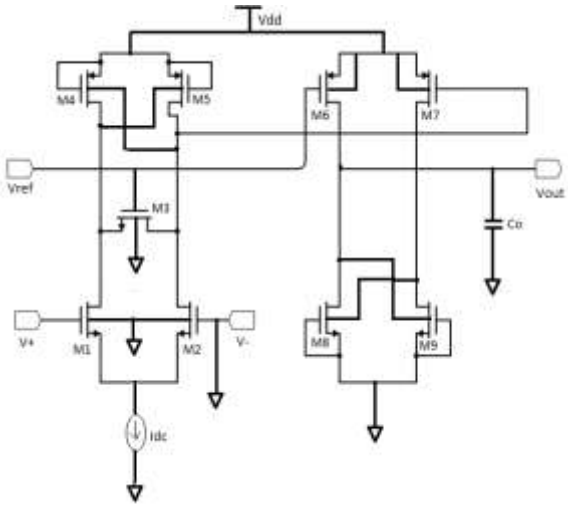

Fig. 3. Existing Error Amplifier

The existing error amplifier in Fig. 3 comprises of two stages, namely, the pre-amplifier stage and the regenerative latch. Transistors M_1, M_2, M_3, M_4, M_5 account for the pre-amplifier stage which incorporates a differential amplifier (M_1 and M_2) with PMOS cross coupled transistors (M_4 and M_5) as load. Transistors M_6, M_7, M_8 and M_9 form the regenerative latch. The differential amplifier operates in differential mode with one of the inputs grounded (V-) and the output is single ended output V_{out} which is measured with respect to ground.

B. Pass element

There are 5 basic possible configurations for the pass element namely, NPN darlington, NPN follower, PNP, NMOS follower and common source PMOS. In the existing circuit, PMOS transistor has been used as the pass element as it exhibits lowest dropout voltage because of its variable resistance property [3]. The source-drain voltage changes with the change in W/L ratio. It proves to be better than the rest in terms of quiescent current flow, output current and speed [2].

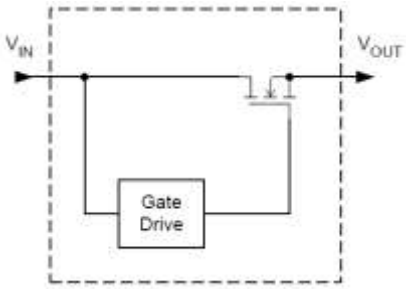

Fig. 4. PMOS transistor as pass element

C. *LDO voltage regulator Circuit*

The existing LDO voltage regulator circuit in Fig. 5 comprises of PMOS input drivers and PMOS pass elements. It consists of differential amplifier stage consisting of M_3 and M_4, with PMOS connected load M_6 and M_7. The transistor M_4 is provided with self-bias. The transistors M_3 and M_4 are matched i.e. they have the same width to length ratio (W/L ratio) and same quiescent current. Input $V_{in}$is applied to M_9 and output V_{out} is measured across a capacitive load C_{out} of 2 pF.

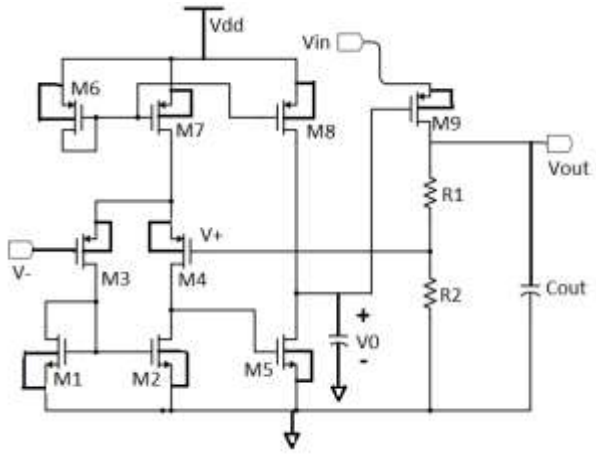

Fig. 5. Existing LDO voltage regulator Circuit

IV. PROPOSED LDO VOLTAGE REGULATOR DESCRIPTION

A. *Error amplifier*

A high gain differential amplifier serves as an error amplifier, with one end of the input connected to the input voltage source, while the other being connected to the ground. A current mirror circuitry is used as differential amplifier, which comprises of NMOS load and PMOS tail current source. The current mirror circuitry is used so as to provide high output impedance, and high gain [5].When the value of regulated voltage changes, the error amplifier generates the error signal which then drives the pass transistor element in order to regulate the output [10].

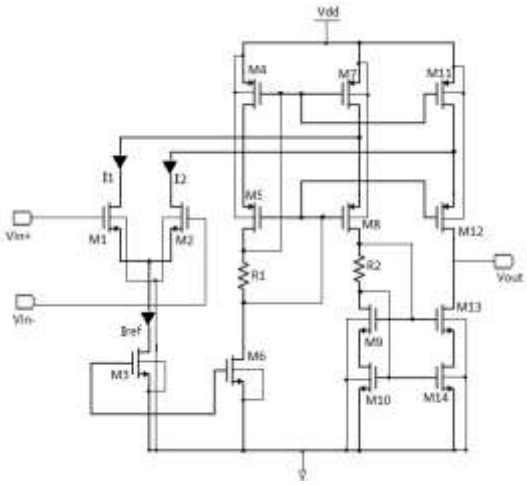

Fig. 6. Folded Cascode Error Amplifier

The proposed error amplifier as shown in the Fig. 6, is made of current sourcing PMOS circuitry which employs the use of folded cascode amplifier. Transistors M_1 and M_2 form a differential pair with constant common current I_{ref}, wherein M_3 works as current sink. The design is such that the following group of transistors are matched (i) M_1 and M_2, (ii) M_9, M_{10}, M_{13} and M_{14}, (iii) M_4, M_5, M_7, M_8, M_{11} and M_{12}. In this configuration, transistors M_3 and M_4 provide self biasing. This self-biasing keeps M_3 and M_4 always in saturation region. Self-biasing also eliminates the requirement of bias voltage, making V_{dd} sufficient enough to drive the circuit.

B. *Pass element*

PMOS transistor is used as pass element accounting to its quick charging and discharging of the output capacitor of 2pF and increases the slew rate as high as 10^6. As the pass transistor exhibits a large parasitic capacitance at its input, therefore, slew rate of the pass element should be high enough so as to drive a high capacitive load.

C. *Proposed LDO voltage regulator schematic*

The proposed circuit uses a current-sourcing PMOS which accounts for quick charging and discharging of the output node which is suitable for increasing the slew rate. The schematic of the LDO voltage regulator shown in Fig. 7 consists of an error amplifier, pass transistor and passive elements.

The proposed design consists of the following group of matched transistors (i) M_1 and M_2, (ii) M_3, M_4, M_{10}, M_{11}, M_{12} and M_{14}, (iii) M_5, M_6, M_7 and M_8, (iv) M_{15} and M_{16}. A bias voltage of V_b was given as 300mV while the input was given to M_3. M_{14} is the current-sourcing PMOS, as it accepts current from the positive supply V_{dd}.

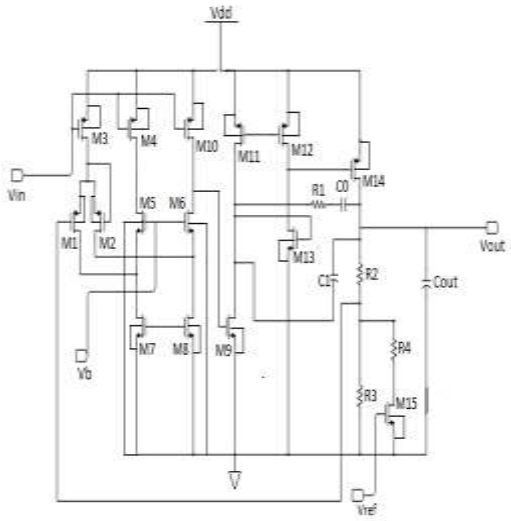

Fig. 7.Proposed LDO voltage regulator schematic.

A voltage divider feedback is provided from input to the output [9]. If a large deviation occurs in load current, despite the voltage source being constant, the feedback loop regulates the loop impedance in order to match the output level with the desired level[11].

TABLE 1. DESIGN PARAMETERS OF LDO VOLTAGE REGULATOR

Design	Value
Supply voltage	1.8 +/-10% V
Technology	TSMC 90nm
Pass transistor	PMOS (W=40um, L=250nm)
Feedback resistors	$R_1 = R_2 = 200K\Omega$
Feedback resistors	Cout= 0.1 pF

V. SIMULATION AND RESULTS

The designed LDO voltage regulator is simulated with 90nm TSMC CMOS technology in CADENCE ADE tool. The input voltage of the LDO voltage regulator ranges from 0.8-1.8V .The maximum output current is 0.5mA when the input voltage is 1.8V. Fig. 9 shows the results of the existing LDO voltage regulator

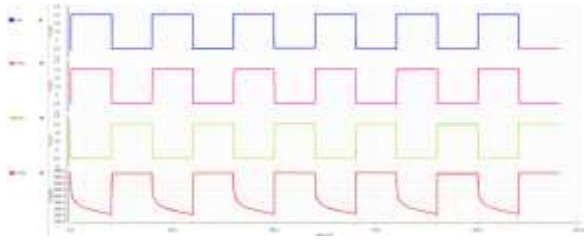

Fig. 8. Simulation waveform of existing Error Amplifier

The adjoining Fig. 8 shows the waveforms of existing Error Amplifier, comprising of the two input signals V_{in+} and V_{in-} and the output V_{out} which is the amplified version of the difference between the input signals. It can be observed that Vout varies from 350mV to 650mV when the inputs varying between 0 to 2V are applied with different cycles.

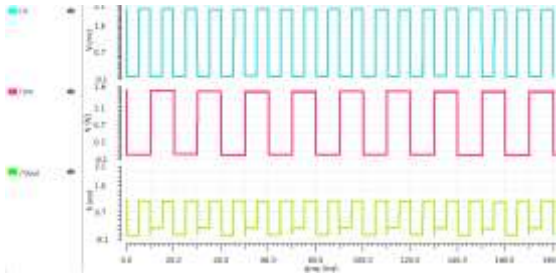

Fig. 9. Simulation waveform of existing LDO

The simulation waveform of the existing LDO (Fig. 9) shows that even when the input voltage V_{in} rises till 2V, the output V_{out} always remains below 1.5mV, when the reference voltage V- is as high as 2.1mV.

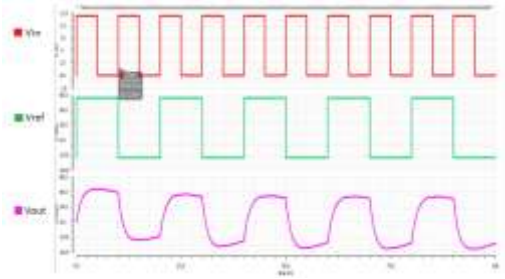

Fig. 11. Simulation waveform of proposed LDO

In the simulation waveform of proposed LDO, from Fig. 11, it can be observed that even when the input voltage V_{in} is as high as 1.25V, the output V_{out} doesn't go beyond 40-45mV, when the reference voltage V_{ref} applied is 60mV. The final output is a regulated wave, which does not allow any fluctuations in input voltage to affect the output voltage.

TABLE 2. COMPARITIVE RESULTS

Parameter	LDO[8]	LDO[9]	This work
Technology	45nm	35nm	90nm
V_{dd}(V)	1	3	1.8
Load Capacitance	0.01pF	0.5uF	0.1pF
Drop-out Voltage	200mV	0.2V	200mV
Number of NMOS and PMOS	5,6	8,6	8,8
Power Consumption	15.446uW	14.67uW	10.78uW
Regulated Output Voltage	28mV	60mV	43.66mV

VI. CONCLUSION

In this paper a power efficient (200 mV dropout voltage) Low dropout voltage regulator is successfully designed and implemented using 90nm CMOS technology .The implemented architecture consists of an error amplifier a current sourcing PMOS transistor and a feedback network. By incorporating current buffer compensation technique there is a decrease in the dropout voltage. The designed LDO gives a stable output voltage in the range of 40-45 mV. A reduction of 30.18% in power consumption has been attained[8]. The proposed external capacitor-less scheme overcomes AC stability issues and load transients over the conventional LDO schemes which incorporated the use of external capacitors. The component reduction makes this design more compact in terms of size and economical in terms of power management.

VII. REFERENCES

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