Simulation study of CMOS based 6 Transistors SRAM

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Abstract:
In this paper we computes the Static Noise Margin , Power consumption of 6T SRAM at different voltage supply and temperature. Further, the Simulation of various Waveforms of the 6T SRAM have been presented. SNM is present in SRAM cell which is effect the stability in read operation of the 6T SRAM cells. SRAM cell stability analysis is a based on Static Noise Margin (SNM) investigation when in read mode, although many memory errors may occur during read operations. In this paper we investigate the SRAM cell SNM during read operations analyzing various alternatives to improve cell stability in this mode. We show that it is possible to improve cell stability during read operations while reducing word line voltage by SNM.

Index Terms— *Power Consumption, Cell Ratio, CMOS, Pull-up Ratio, Static Noise Margin (SNM), VLSI.*

I. INTODUCTION

SRAM is faster and can save the use of power supply compared with DRAM. The structure of SRAM is more complex compared with DRAM. DRAM is less expensive to manufacture than SRAM. This reason SRAM is normally used in smaller application like CPU cache memory and user electronic and DRAM at all time used
in larger application like main memory for personal computers. The power consumption has become an important consideration on the VLSI system design and microprocessor as the demand for the portable devices and embedded systems continuously increases [1- 2]. The on-chip caches can reduce the speed gap between the processor and main memory. These on-chip caches are usually implemented using SRAM cells. The write power is usually larger than the read power due to large power dissipation in driving the cell bit lines to full swing. The sum of the power consumption in decoders, bit lines, data lines, sense amplifier, and periphery circuits represents the active power consumption. The power dissipated in bit-lines represents 70 per cent of the total SRAM power consumption during a write operation [3-5]. Many techniques have been proposed to reduce the write power consumption by reducing the voltage swing level on the bit lines [6-10].

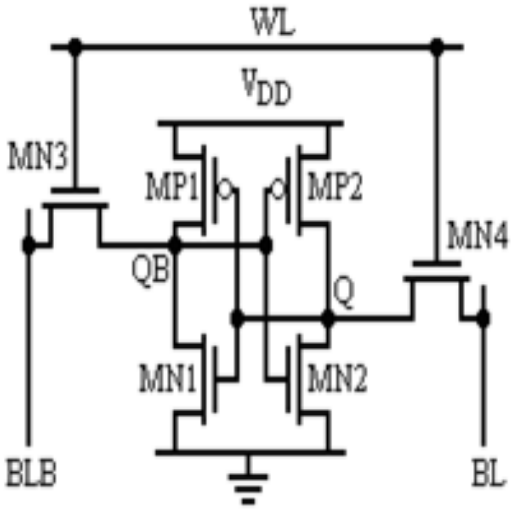

Figure 1: Proposed (A) 6T CMOS SRAM cell

Simulation and Analysis

Static Noise Margin of the SRAM cell depends on the cell ratio, supply voltage and also pull up ratio. For stability of the SRAM cell, good SNM is required that is depends on the value of the cell ratio, pull up ratio and also for supply voltage. Cell ratio is the ratio between sizes of the driver transistor to the load transistor during the read operation. Pull up ratio is also nothing but a ratio between sizes of the load transistor to the access transistor during write operation [11].SRAM cell stability analysis is typically based on Static Noise Margin (SNM) investigation and SNM affects both read and write margin. This work represents the simulation of SRAM cells at different voltages and temperatures. All simulations of SRAM cells have been carried out at HSPICE tool.

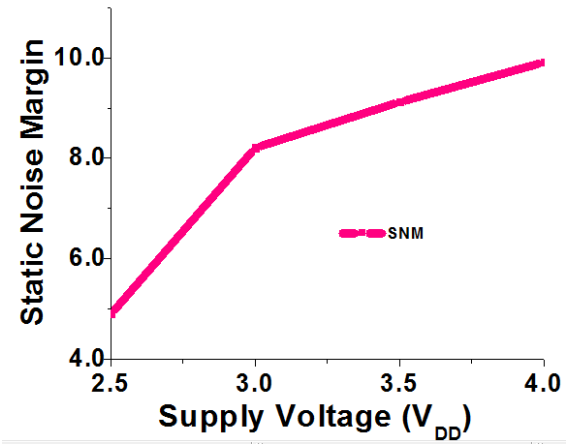

Figure 2 : SNM Vs VDD for 6T SRAM

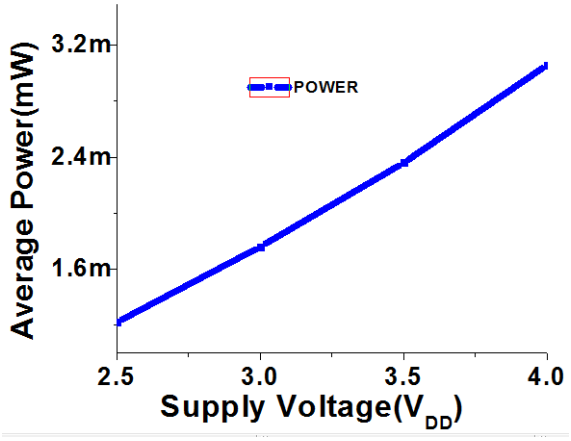

Figure 3 : Power Vs VDD for 6T SRAM

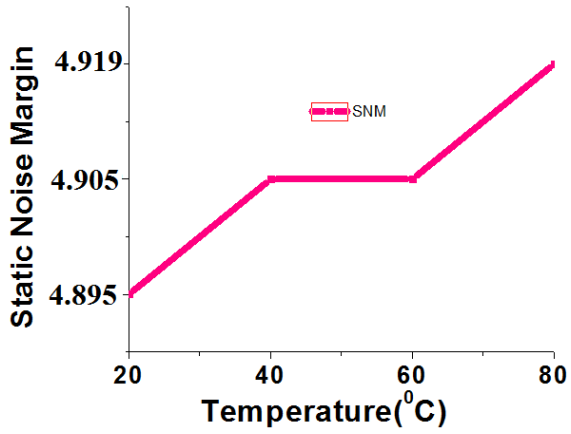

Figure 4 : SNM Vs TEMP for 6T SRAM

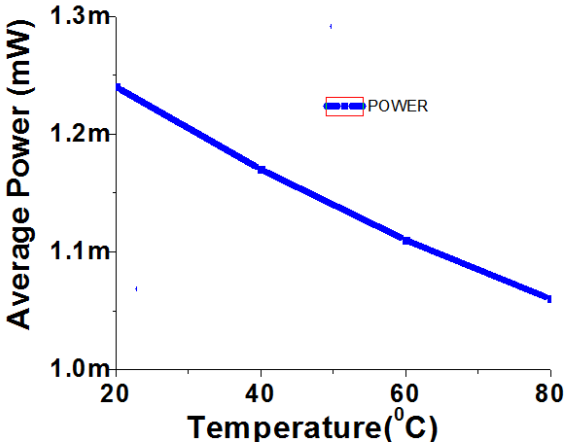

Figure 5 : Power Vs TEMP for 6T SRAM

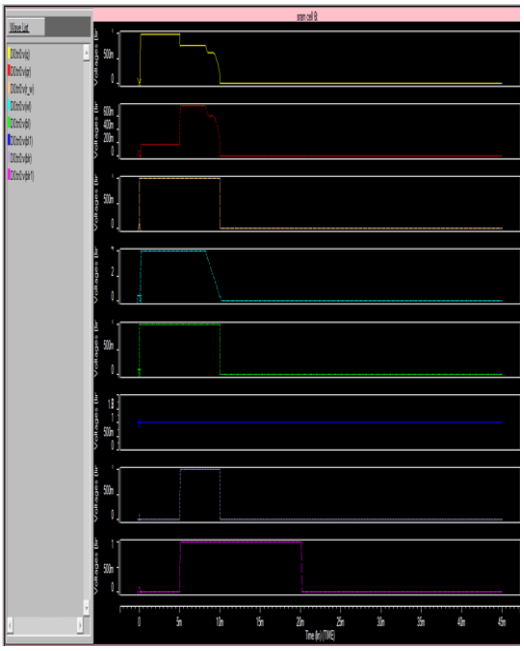

Figure 6 : Waveforms at different node

Result and Conclusion

The Static Noise Margin analysis increasing with both supply voltage and temperature .The Power consumption is increasing with supply voltage but decreasing with temperature. The supply voltage also play vital role in SRAM cell stability during read mode of SRAM cell also by lower power supply may reduce the leakage current for all cells in the memory. The world-line voltage, the bit-line voltage and the power-supply voltage all three voltages could be used to improve the SNM.

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