MPPT Based Dc-Dc Converter with ZVS & ZCS Technique

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ABSTRACT

In this paper, a DC–DC converter topology with a zero voltage and zero current switching control technique [8] has been proposed for solar PV applications. The proposed converter combine the feature of buck–boost operation capability, at the same time, it can carry out zero voltage and zero current switching on the primary side of the converter transformer. The proposed work has been carried out using Matlab/Simulink and results are presented.

KEYWORDS: *DC–DC converter, ZVS, ZCS, Z-source network.*

I.INTRODUCTION:

Renewable energy systems have become very popular. As a result, many new types of converters from the source to the grid have emerged. In order to extend the voltage regulation capability, the intermediate boost DC–DC converters are often used. At the same time, the challenges faced in the field are to decrease the cost [1],[2], size, and weight and to increase the reliability. All these parameters depend on the converter efficiency, switching frequency of semiconductors, and EMI problems, particularly in the system where galvanic isolation is required. In order to achieve afore mentioned responsibilities, main efforts of the power electronics research are concentrated on the soft-switching converter topologies [4-7]. These techniques permit reducing the losses in semiconductors, and as a result, the switching frequency can be raised or the heat sink may shrink in size. There are several ways to achieve soft switching. The implementation of resonance circuits seems to be most suitable [7]. This method is known to contain the disadvantage of increased conduction losses and the presence of additional passive components. The resonance frequency may float, and complex zero crossing control circuits sometimes make its practical implementation complicated.

II.DESCRIPTON OF THE PROPOSED CONVERTER

This section describes the operation principle of the proposed converter. Initially, this solution
Was intended for FC and PV power systems i.e, low voltage applications that require galvanic isolation along with a wide input voltage Regulation range. In the discussed converter, the quasi zero switching network can boost up the input voltage by utilize an extra switching state the shoot through (ST) state. The ST state now is the instantaneous conduction of both switches of the similar phase leg of the inverter. The ST states are used to boost the magnetic energy stored in the dc-side inductors (L1 and L2) without short-circuiting the capacitors C1 and C2. This adds to in inductive energy, in turn, provide the boost of voltage seen on the transformer input winding during the on states of the inverter. Thus, the changing input voltage is first pre regulated by adjusting the ST[6] duty cycle. Afterwards, the isolation transformer is being supplied by a voltage of steady amplitude value.

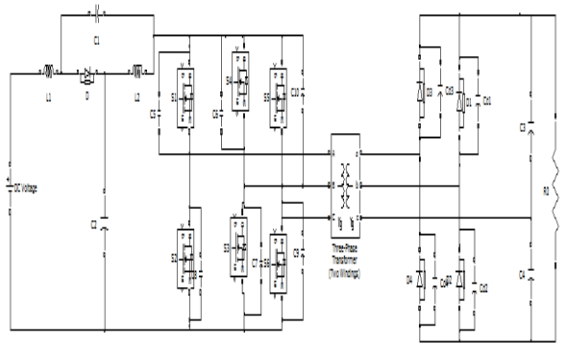

Fig 1: Quasi Zero Switching DC–DC Converter.

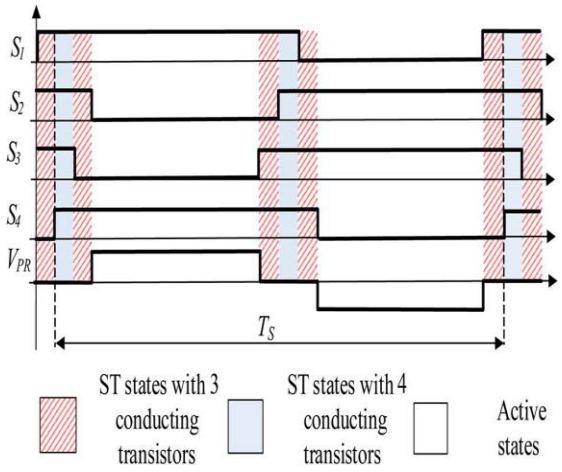

Fig 2: Gate pulses of switches of the ZVS DC-DC Converter

The main aim of our study was to achieve the full soft switching operation of the ZVS based dc–dc converter. The key idea consists of operating in the boundary conduction mode of the ZVS network along with snubber capacitors in the two out of four transistors and small snubbers across the diodes. Fig 2 shows the proposed control algorithm of the FB transistors. It differs by the additional shifting of control signals that leads to the three simultaneously conducting transistors instead of four in the conventional overlap control. Fig 2 shows the operation principle of the proposed solution. The inductor current IL2 has the BCM operation, while current IL1 of the inductor L1 may have BCM or continuous conduction mode, close to the BCM. As a result, full ZVS turn-on of transistors S2 and S4 is reachable. Due to the
Same reason, the ZVS turnoff of the top transistors S1 and S3 is achievable. At the same time, in order to eliminate the turn-on switching losses of the transistors S1 and S3, the inductor current IL2 is forced into the BCM. As a result, the turn-on of the transistors S1 and S3 corresponds to the ST[6] conduction mode start-up under the ZCS[1] condition.

III.MODES OF OPERATION

MODE 1: t_1–t_2*:* At the moment of time t_1, the transistor S_3 turns on, and the qZS network is transferred to the ST conduction mode. Initially, the snubber capacitor C_{S_2} is partially discharged through the leakage inductance and the upper transistor s_1. At the very end of this transient process, the transistor S_2 can be turned on. final simulation and experimental waveforms would depend on the certain ratio between the snubber capacitor and the leakage inductance values.

MODE 2: t_2–t_3*:* during the t_2–t_3 time interval. Transistors S_3 and S_4 are conducting. It corresponds to the ST conduction mode when only one leg is involved in the ST generation.

MODE 3: t_3–t_4*:* during the t_3–t_4 time interval. All transistors are conducting. Since all transistors are under zero voltage, there are no dynamic losses after the transistor S_2 turns on. The current is shared between two legs of the FB.

MODE 4: t_4–t_5: when the transistor S_1 is turned off. It occurs under the full ZVS condition and does not influence the converter behavior because the ST state is still valid.

MODE 5: $t5$–t_6*:* At the moment of time t_5, the transistor S_4 is turned off under the full ZVS condition due to the snubber capacitor.
The snubber capacitor C_{S_4} charges through the qZS network and the transistor *S*3. This process continues to the moment of time t_6.

MODE 6: t_6–t_7*:* during the t_6–t_7 time interval. The aforementioned time intervals correspond to the half period operation. Further switching process goes on symmetrically. It should be mentioned that time intervals t_1–t_3 and t_4–t_5 correspond to the ST conduction mode when only one leg is conducting. These time intervals are required in order to provide full soft-switching operation but, at the same time, should be as short as possible in order to decrease conduction losses.

IV. RESULTS AND DISCUSSION

To verify the previously described idea, a PSIM simulation model, along with a 100-W experimental prototype, was developed. Table I shows the parameters used for the simulation.

Table 1: System Parameters

PARAMETER	VALUE
Input voltage range/ Output Voltage	15V—30V
Maximum power	100W
L1/L2	0.75μH , 0.35H
C1,C2/$C_{s2,}C_{S4}$	26.5μF/24nF
Transformer leakage inductance L_L/Magnetizing inductance L_M	1400nH/60 μH
$C_{d1,}C_{d2}/C_{3,}C_4$	120pF/22 μF

ST Switching frequency	600KHz
diode, forward voltage drop	0.62V
VDR diodes, forward voltage drop	1.5V
MOSFET, Open drain-source Resistance/ R_S	0.25m Ohm/10hm

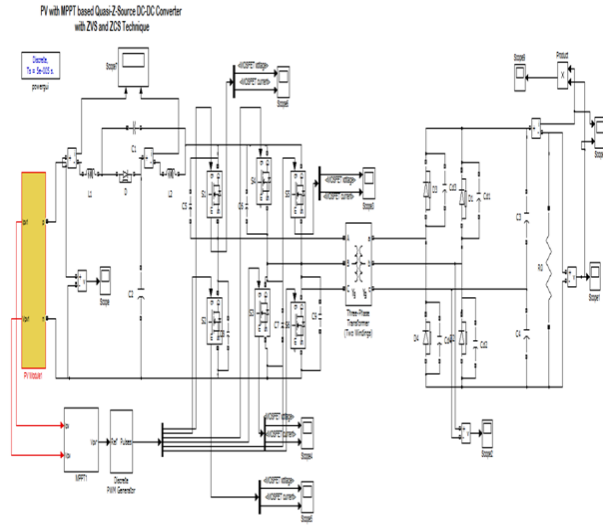

Fig 3: Simulink model of proposed converter

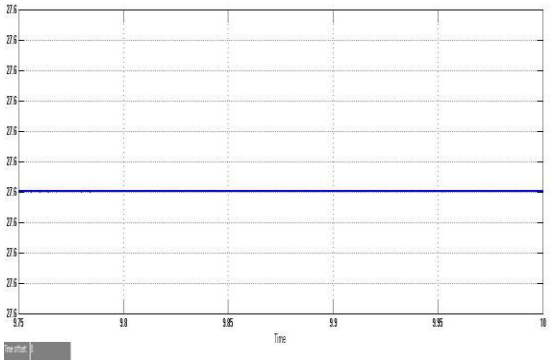

Fig 4: InputVoltage

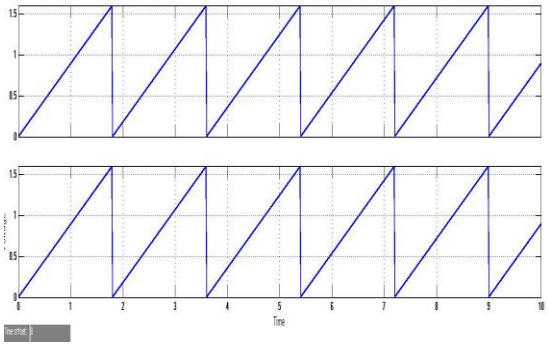

Fig 5: Inductor Voltage

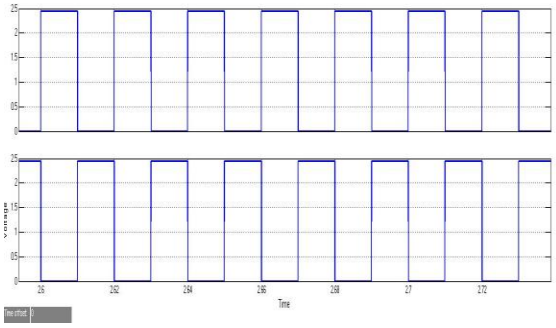

Fig6: Voltage & Current waveforms of switch

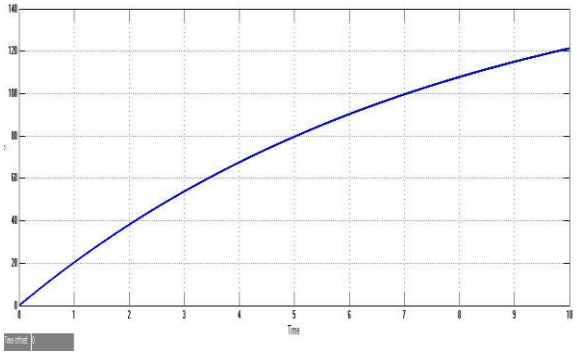

Fig 7: Output voltage

Working points were tested. Fig 4 illustrates simulation results of the operation point with the proposed control approach where the maximum ST duty cycle is required (*DS* = 0.25). In this working point, the ST states consist of *DSF* =0.23 and *DSH* = 0.02. It means that the ST state is realized by means of only one leg for a very short moment of time.This short moment of time is enough to realize full soft switching conditions. Fig 5 shows the inductor currents I_{L_1}, I_{L_2}. It can be seen that, despite the DCM mode in the inductor current I_{L_2}, the input current has

the CCM. The input voltage V_{IN} was about 14 V, and the input power was about 80W. The output voltage was about 300V.fig 5 presents the study of the transistors' switching conditions. It can be seen that the diagrams correspond to the theoretical expectation.

V.CONCLUSION

This paper has presented a modified quasi-Z-source dc–dc converter with a novel ZVS and ZCS technique. Increased ripples in the inductor currents lead to the increased RMS current value, which, in turn, leads to the increased conduction losses of the semiconductors. However, the major aim of the proposed work lies in the elimination of the switching losses and resulting rise of the switching frequency. A higher switching frequency will result in a further decreased value of the passive components and, consequently, also in a more compact design of the converter. It should be noted that the proposed idea could be applied for different kinds of impedance source and current-fed dc–dc converters

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