Design And Simulation Of 10-Bit Pipeline Adc Using Switch Capacitor Circuit And Opamp Sharing In 0.25 µm CMOS Technology at 2.5 V

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Abstract**—** *A 10-bit pipeline Analog-to-digital Converter (ADC) is designed using switched capacitor circuit. ADC is designed in 9 stages, 1.5 bit/stage pipeline is used in eight stages and ninth stage uses two bit flash ADC. The ADC uses Opamp sharing techniques which are shared between amplifying and MDAC stage. Load capacitance has been removed which reduced the number of capacitors used and power consumption. The ADC is designed on 0.25 µm CMOS technology at 2.5 V supply voltage. S/H is used in first stages that consume most of the power consumed by the ADC, after first stage S/H circuit is removed, and also the scaling is done to reduce the power consumption. Cascodeopamp is designed with gain of 72.52 dB, phase margin of 66º and unity gain bandwidth of 162.61MHz. The ADC is designed at sampling rate of 5 MS/s and consumes 158.1208mWpower.*

Keywords — *ADC, MDAC, sample and hold, pipeline ADC, DAC*

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I. INTRODUCTION (SIZE 10 & BOLD)

Advantages of digital systems over analog systems made it popular in system designing, but the natural signals are analog in nature that is why it becomes important to have a system which can convert the analog signal into the digital signals. Analog to digital converts are such circuits which can connect the analog domain into the digital domain. There are various types of ADCs which are used and every ADC has its own advantages and disadvantages. Pipeline ADC can resolve medium to high resolution at higher speed. Which make it popular for modern digital systems where high resolution with higher speed is required.

Pipeline ADC uses several stages to convert analog signal to digital signal every stage has flash ADC of 1 to 3 bit and converts portion of input signal to output. The first stage produces most significant bit (MSB) while the last stage produces least significant bit (LSB).

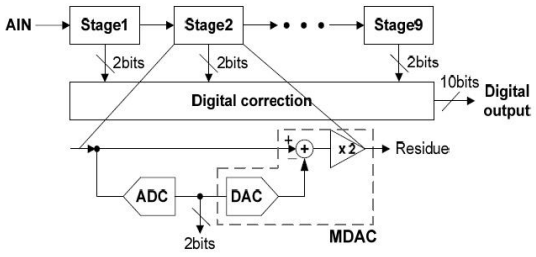

Figure 1: 10-bit Pipeline ADC

II. PIPELINE ADC ARCHITECTURE

The pipeline ADC is consist of cascade of low resolution stages that generates parallel ADC output and residue signal for next stage. Residue is un-quantized output which is the output of subtraction of input signal and the digital to analog (DAC) signal. The architecture of the 10-bit pipeline ADC is shown in figure 1. In pipeline ADC each stage consist of low resolution flash ADC, DAC and subtractor, DAC consist of multiplying digital to analog converter (MDAC) that converters digital signal to analog signal followed by the amplifier. The residue generated from first stage goes to next stage, for 10-bit ADC eight stages are of 1.5 bit/stage and the last stage uses two bit flash ADC.

To synchronize the output of the stages delay elements is used which reduces with the stage, last stage does not require MDAC and delay element. Each stage has two output lines which is later given to the error correction block that generates the 10-bit output lines. The block diagram of MDAC is shown in the figure 2.

III.1.5 BIT/STAGE PIPELINE

Comparator's offset saturates the input signal which cause the error in the bit. 1.5 bit/stage pipeline sub ADC quantizes the input to three levels and the residue is limited to half the full scale range.

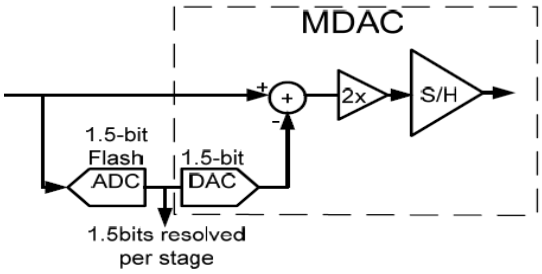

Figure 2 : Pipeline ADC Block diagram for 1.5 bits/stage

If comparator threshold offsets forces the residue signal to fall outside normal range, the residue signal will be accurately passed into the next stage provided the offset is within $\pm V_{ref} / 4$. Figure 3 demonstrates this by showing the transfer function of a 1.5-bit MDAC when there are threshold offsets in the sub-ADC. The fourth level is removed because the MDAC only needs to indicate whether the residue output is above or below $V_{ref} / 2$ and therefore, there is only an overlap of half bit. The accuracy of the 1.5-bit sub-ADC reduces from N bit to 2 bits using DEC. Generally, by using DEC, the accuracy of the sub-ADC can be increase if fewer bits are resolved in each stage.

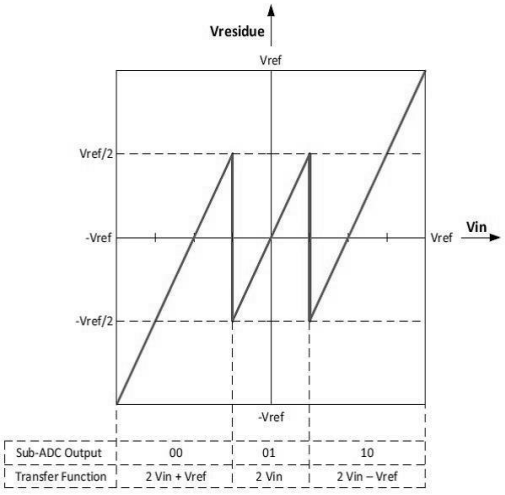

Figure 3: Transfer function of 1.5 bits/stage MDAC [12]

The pipeline ADC applies DEC and consists of a front-end S/H, 8 pipeline stages, and a 2-bit flash ADC in last stage. Each pipeline stage resolves 1.5 Bits/stage, which is represented by a 2 output lines of single bit. In the end, a total of 18-bits are generated from a single input sample. To apply DEC, the bits from each adjacent pipeline stage Overlap by half a bit and form the expected 4-bit output.

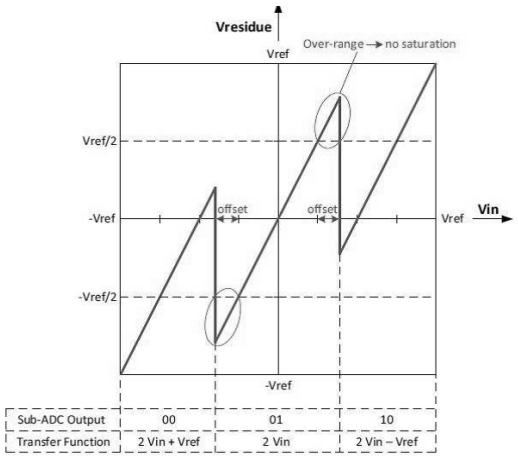

Figure 4: Transfer function of a 1.5 bit/stage MDAC with comparator with offset

IV. CASCODE OPAMP

Cascade opamp is used for the pipeline ADC design the opamp is designed in two stages first stage is the preamplifing stage that provides most of the gains and has higher input impedance.

A. Gain

The settling accuracy refers to how close the residue output settles to its intended value and therefore, it can limit the accuracy of the ADC. Assuming the opamp has sufficient time to settle to its final value, the opamp's open-loop gain, A, sets the settling accuracy. This is because a higher open-loop gain results in a more accurate stage gain and in turn, the residue output follows a more accurate transfer function. To ensure the residue settles to with ΔLSB, the loop gain of the closed-loop, $A\beta$, must be: $A\beta > \frac{2^N}{\Delta}$ Where β is the feedback factor of the closed-loop circuit and $1LSB = \frac{1}{2^N}$. The loop gain, as the name suggests, is the gain around the opamp closed-loop circuit. Considering there are other sources of error (e.g. thermal noise), a reasonable choice is $\Delta = 0.25LSB$. For instance, the front-end sample and hold and first pipeline stage in a 4-bit pipeline ADC requires a loop gain of:

$$\frac{2^{10}}{0.25} = 4096 \text{ or } 72\text{dB}$$

B. Bandwidth

Assuming the opamp has sufficient gain to accurately settle to its final value, the opamp speed, which determines how fast the residue output settles to a final value, sets the settling accuracy. The bandwidth must be high enough for the opamp to settle to a sufficiently accurate value within the required time of half a sampling period, $0.5 / f_s$

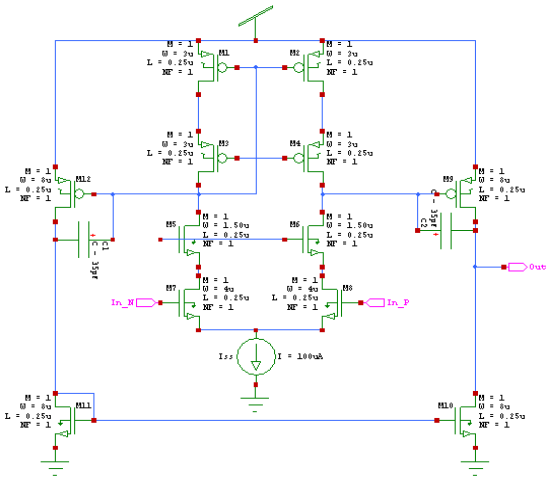

Figure 5 Schematic of Opamp [27]

The bandwidth of the opamp closed-loop circuit, f_{3dB}, so that the residue settles to within 0.5 LSB in half a sampling period.

$$f_{3dB} = \frac{(N+1).\ln 2.f_S}{\pi}$$

The frequency response opamp is shown in the figure 7.

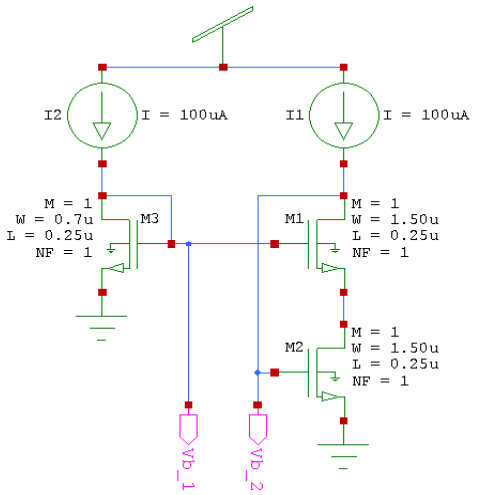

Figure 6: Bias Circuit for Opamp

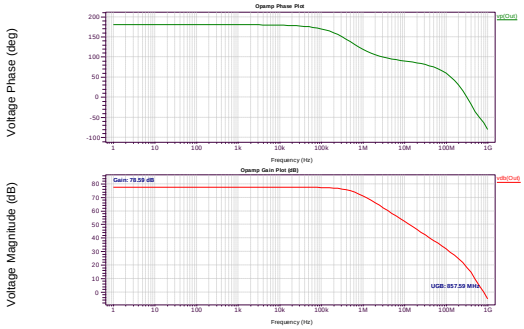

Figure 7: Frequency response of Opamp

V. COMPARATOR DESIGN

The comparator is unclocked of three stages, pre-amplification, decision circuit and output buffer. Pre-amplification stage consist of differential input stage with active PMOS load. M1 and M2 NMOS transistor act as input it also provides the high input impedance, it also improves the sensitivity.

Decision circuit uses positive feedback that increases the gain, cascading of pre-amplification and decision circuit increases the gain with large amount. To make the output compatible with the digital circuit output stage is used which uses inverter it also provides small gain. The transfer characteristics of comparator is shown in the figure 9.

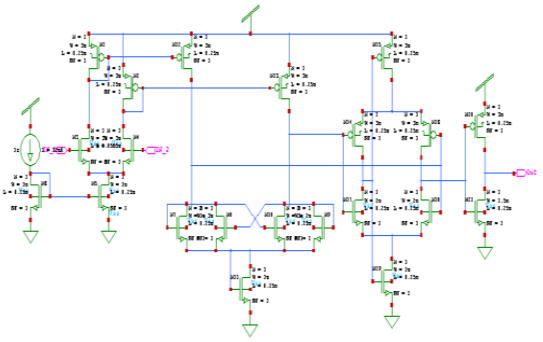

Figure 8: Schematic of Comparator

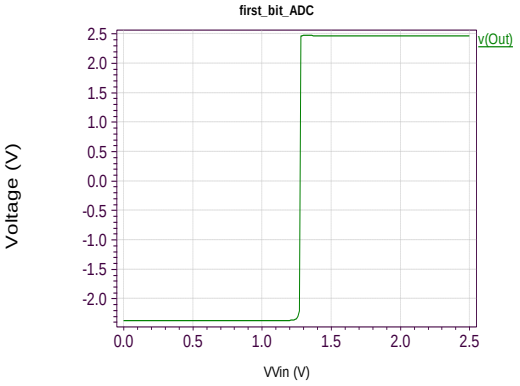

Figure 9: DC transfer characteristics of Comparator

VI. NON-OVERLAPPING CLOCK GENERATOR

Non-overlapping clock is required for the MDAC switch capacitor circuits and sample and hold circuit. The schematics of non-overlapping is shown in the figure 10. The response of the non-overlapping clock is shown in the figure 11.

VII. SAMPLE AND HOLD CIRCUIT

Switch capacitor sample and hold circuit is used the schematic of sample and hold is shown in figure 12. ϕ_{1p} clock is advances clock which triggers the M4 transistor, capacitor's bottom plate is connected to the ground.

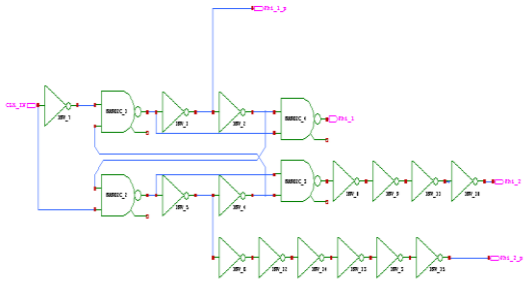

Figure10: Schematic of Non Overlapping clock

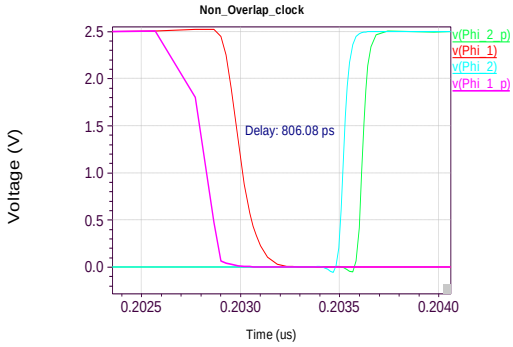

Figure 11: Transient response of non-overlapping clock

ϕ_1 clock connects the output of the opmap to ground by triggering the M1 transistor, which discharge the initial charge stored in the opamp at the same clock pulse input is connected to the top plate of the capacitor C1, the input is stored in the capacitor in the form of charge. At this time signal is sampled and stored in the capacitor.

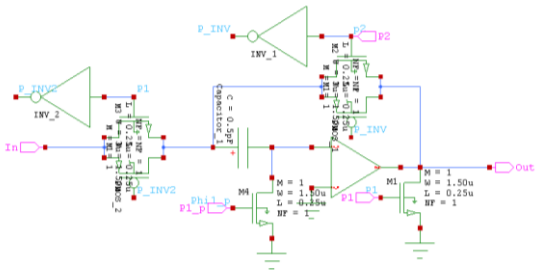

Figure 12: Switched capacitor sample and hold circuit

At ϕ_2 capacitor top plate is connected to the output of opamp and charge stored at the capacitor is transferred to the output. The transient response of sample and hold circuit is shown in the figure 13.

VIII. MULTIPLYING DIGITAL TO ANALOG CONVERTER (MDAC)

Figure 14.shows the schematic of Multiplying Digital to Analog (MDAC) using a switched capacitor approach.[10].

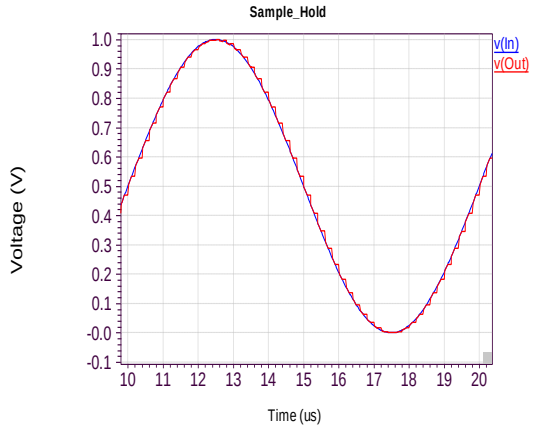

Figure 13: Transient response of sample and Hold circuit

Since 1.5 bits/stage architecture has one of three digital outputs, thus the DAC has three operating modes.

ADC output=01: No over range error (stage input is between $-\frac{V_{ref}}{4}$ and $+\frac{V_{ref}}{4}$).

During ϕ_1: $Q_{C1} = C_1 V_{in}, Q_{C2} = C_2 V_{in}$

During ϕ_2 : C_1 is discharged, thus by charge conservation: $C_1 V_{in} + C_2 V_{in} = C_2 V_{out}$

(noting negative feedback forces node V_p to a virtual ground) Thus

$$V_{out} = \frac{C_1 + C_2}{C_2} V_{in} \rightarrow if C_1 = C_2, then: V_{out} = 2V_{in}$$

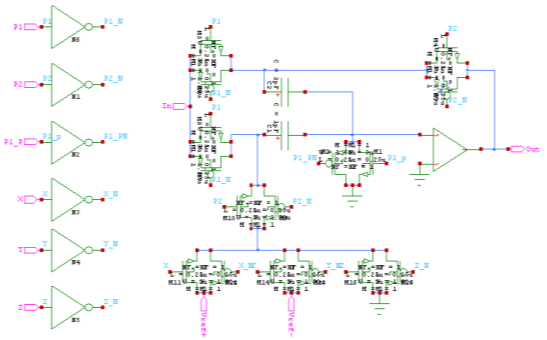

Figure 14: Schematic of MDAC

ADC output=10: Over range error-Input exceeds $+\frac{V_{ref}}{4}$, thus subtract $\frac{V_{ref}}{2}$ from input

During ϕ_1: $Q_{C1} = C_1 V_{in}, Q_{C2} = C_2 V_{in}$

During ϕ_2 : C_1 is charged to V_{ref}, thus by charge conservation

$$C_1 V_{in} + C_2 V_{in} = C_1 V_{ref} + C_2 V_{out}$$

$$\therefore V_{out} = \frac{C_1 + C_2}{C_2} V_{in} - \frac{C_1}{C_2} V_{ref} \rightarrow if, C_1 = C_2, then: V_{out} = 2V_{in} - V_{ref} = 2(V_{in} - V_{ref}$$

ADC output=00: Under range error-Input below $-\frac{V_{ref}}{4}$, thus add $\frac{V_{ref}}{2}$ to input

During ϕ_1: $Q_{C1} = C_1 V_{in}, Q_{C2} = C_2 V_{in}$

During ϕ_2 : C_1 is charged to $-V_{ref}$. Thus by charge conservation $C_1 V_{in} + C_2 V_{in} = C_1(-V_{ref}) + C_2 V_{out}$

Thus the switched capacitor circuit can be used to implement the sample-and-hold, gain stage, DAC, and subtraction blocks of ADC. To reduce the signal dependent charge injection bottom plate sampling technique is where the use of an advanced clock ϕ_{1p}, makes charge injection signal independent [10]. The total input sampling capacitance in ϕ_1 is $C_{iT,MDAC} = C_1$.

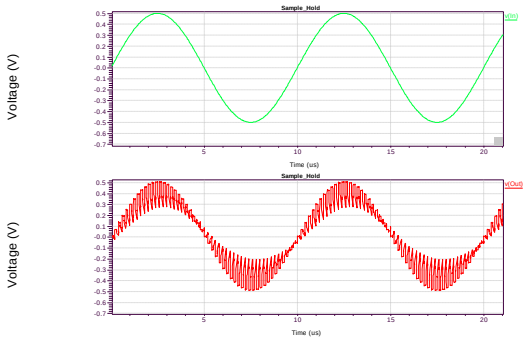

Figure 15: Transient response of MDAC for sinusoidal signal

In ϕ_2, the two $C_1/2$ capacitors apply a load of $C_1/4$ on the MDAC opamp. Taking into consideration the loading effects of the next stage and of the parasitic ccapacitance C_{n2}, the total output load on the MDAC opamp is:

$$C_{L,flipMDAC} = C_1/4 + C_{iT,subADC} + C_{iT,nextstageMDAC} + C_{n2}$$

Transient response of MDAC is shown in the figure 15.

IX. 10-BIT PIPELINE ADC

A. Sub analog to digital converter

Sub ADC is a 1.5 bit Flash ADC in which two comparators are used to compare the input signal with two reference voltages $\frac{+V_{ref}}{4}$ and $\frac{-V_{ref}}{4}$

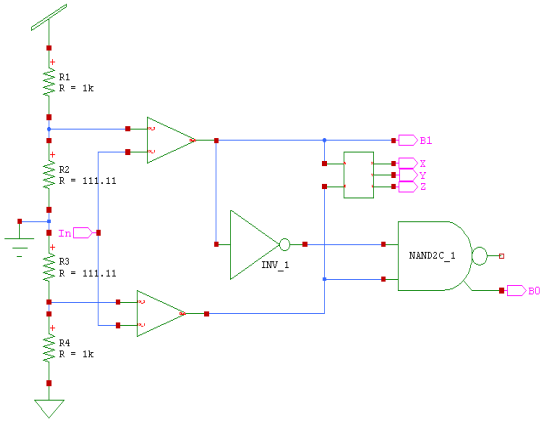

Figure 16 Schematic of sub ADC

Respectively as shown in Figure 16. The reference voltage selected in this ADC is 1V which means the $+V_{ref}$ =0.25 V and $-V_{ref}$ =-0.25 V [6]. It generates the thermometer code at the output of the comparators that need to convert into the binary code. This can be converted by adding thermometer to binary encoder circuit. Transient response of sub ADC is shown in the figure 17.

B. First stage pipeline ADC

First stage pipeline ADC is shown in figure 18 first stage have sample and hold which samples the input signal, sampled signal is given to sub ADC which converted it to digital signal. MDAC converts this digital signal to analog signal the switches of MDAC

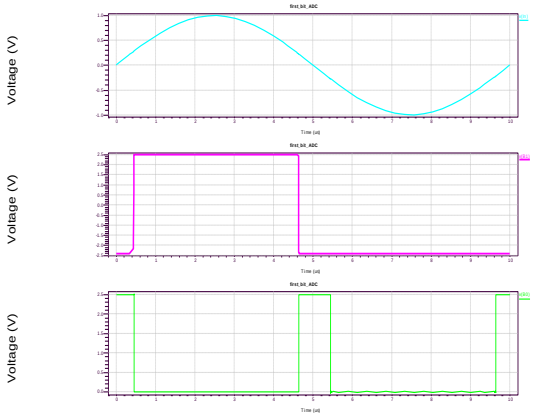

Figure 17: Transient response of sub ADC

Driven by the digital output of first stage by encoding circuit. After first stage sample and hold circuit is removed and scaling is also done which reduces the power consumption

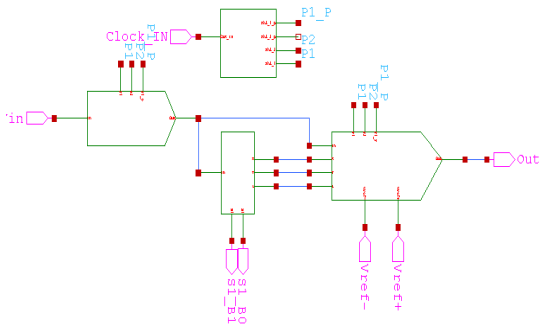

Figure 18: Block diagram of first stage pipeline ADC [18]

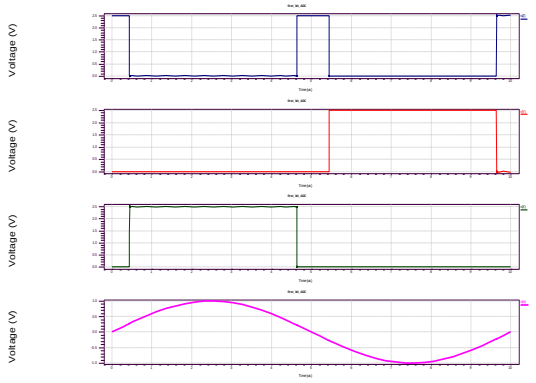

Figure 19: Transient response of first stage pipeline ADC

The transient response of first stage pipeline ADC is shown in the figure 19.

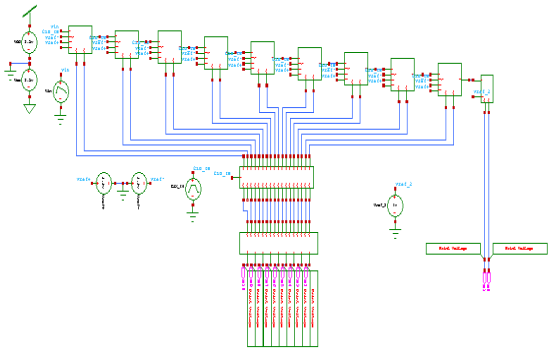

Figure 20: 10-bit pipeline ADC test setup

C. 10-bit pipeline ADC

The complete schematic of 4-bit pipeline ADC is shown in figure 20, First and second stage are identical and sampled capacitor C2 =C1= 1 µF is used. After second stage scaling is done to reduce the power consumption and uses C1=C2=0.5 µF and 0.25 µF for third, fourth stage respectively

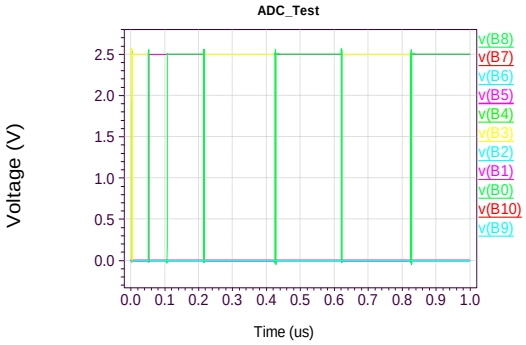

Figure 21: Transient response of 10-bit pipeline ADC

Transient response of 10-bit pipeline ADC is shown in figure 21.

X. PERFORMANCE SUMMARY

Technology	0.25 µm CMOS process
Resolution	10 bit
Supply Voltage	2.5 V
Conversion rate	5 MS/s
Power	158.1208

XI. CONCLUSION

The goal of this dissertation was to design a 2.5 V, 1.5 bit/stage 4bit ADC by using switched capacitor technique. The ADC is designed in 0.25 µm CMOS process at 2.5 V supply voltage. It also shows the comparison between the power consumption of stages with the S/H and without S/H which gives 28.33 mW in first stage (with S/H) and 19.59 mW third stage (without S/H).Further the ADC is tested at input frequency of 1 MHz and sampling rate of 5 MS/s, at which ADC consumes 158.12mW power.

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