Implementation of 16x16bit and 32x32bit Vedic Multiplier using FPGA board

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Abstract-*This paper proposed the implementation of 16x16bit and 32x32bit Vedic Multiplier using modified Ripple Carry Adder, modified Kogge Stone Adder and BRENT KUNG ADDER on **Spartan 6 family xc6slx4 -3-tqg144 FPGA** and its synthesis using **XILINX ISE 14.1 simulator** and coding is done using **VERILOG HDL**. Vedic Mathematics is the ancient system of mathematics which has a unique technique of calculations based on 16 Sutras. The work has proved the efficiency of Urdhva Tiryakbhyam– Vedic method for multiplication which strikes a difference in the actual process of multiplication itself. It enables parallel generation of intermediate products, eliminates unwanted multiplication steps with zeros and scaled to higher bit levels using Karatsuba algorithm with the compatibility to different data types. Urdhva Tiryakbhyam Sutra is most efficient Sutra (Algorithm), giving minimum delay for multiplication of all types of numbers, either small or large.*

Keywords- Kogge Stone Adder, Ripple Carry Adder, BRENT KUNG ADDER, FPGA board, Urdhva Tiryakbhyam, Verilog HDL.

I. INTRODUCTION TO FPGA

The Field Programmable Gate Array is also known as FPGA board. This is basically a board consisting of semiconductors engineered to remain programmable after production. Rather than locking in projects prior to manufacturing, engineers utilizing FPGA boards can test a wide range of different variables after building the entire board. In essence, the boards consist of hundreds or thousands of logic cells, and generally contain a number of inputs and outputs.

The FPGA board is a computing technology that has been in use nearly thirty years by engineering students and professionals alike. In design of an electronics project that requires computation and programming, the FPGA board is the best choice. The ease and flexibility afforded by the boards have made them incredibly popular. Fig.1 shows an FPGA board.

Fig.1 FPGA BOARD

II. DEVELOPMENT OF FPGA BOARDS

The first commercial FPGA boards were developed in the mid-1980s. This technology grew in popularity through the late 1990s. Today, the market for these boards is estimated at nearly \$3 billion. While the boards have used a number of different types of processing technologies in the past, today's FPGA boards predominantly utilize SRAM processing. Xilinx and Altera are the most prominent manufacturers of FPGA boards. Xilinx, which first developed the technology, remains the leader with 50% market share. Companies such as QuickLogic, SiliconBlue Technologies, Actel and Lattice Semiconductor also offer these products.

Predefined circuits available from FPGA board manufacturers or from independent developers are often used to expedite the design of projects. Most vendors also provide software that engineers can use to design, run simulations and program the boards.

III. STEPS OF IMPLEMENTATION

Connect FPGA kit with the machine and select JTAG after connecting JTAG cable of FPGA kit with CPU and then follow the following steps:

Step1: Open the File. Go to Project Do Design Properties; change the Design properties as shown in an example in Fig.3, Family name as Spartan3, Device as XC3S200, Package as TQ144 and Speed as -4.

Fig.3

Step2: Go to User Constraints → Double Click on I/O Pin Planning (PlanAhead)-Pre-Synthesis or I/O Pin Planning (PlanAhead)-Post-Synthesis as shown in Fig.4; and provide Pin names for inputs and output according to FPGA Kit.

Fig.4

Step3: Go to Implement Design → Right click on Generate Programming File, click on Process Properties, click on Startup Options, select JTAG clock in FPGA Start-up Clock, click OK, then double click on Configure Target Device or right click on it and click Run as shown in Fig.5.

Fig.5

Step4: After clicking on Run in previous step click OK in the dialogue box to open iMPACT; then Double click on Boundary Scan, right click to Add Device, click on Add Xilinx Device as shown in Fig.6.

Fig.6

Step5: After adding device in previous step a message will appear in the message box as 'Added Device selected successfully', then right click and click on Initialize Chain as shown in Fig.7, then click on bypass. A figure as Fig.8 will appear then.

Fig.7

Fig.9

Step7: Now on the connected FPGA Spartan6 Development Kit provide the input with the switches according to provided Pin names in Step2. Here, in Fig.10 and Fig.11 Spartan 3 FPGA kit is shown just to make understand the implementation of a Vedic Multiplier on FPGA. A Spartan 3 can work only for 2x2bit and 4x4bit Vedic Multiplier as only 8 output providing LEDs are available with the Spartan3 kit.

Suppose for vedic multiplier 4x4bit, we have selected switch names for 4bit input A as P14 for A[0], P15 for A[1], P17 for A[2] and P18 for A[3] in which A[3] is LSB and A[0] is MSB. Select switch names for input B as P20 for B[0], P21 for B[1], P23 for B[2] and P24 for B[3] in which B[3] is LSB and B[0] is MSB. Suppose we are providing inputs for 4bit input A as 0011(i.e. 3 in Decimal) and for 4bit input B also as 0011(i.e. 3). Output multiplication of 3 with 3 must be 9(i.e. 00001001 in 8bit binary). For 8bit output we are providing pin names as P25, P26, P27, P28, P30, P31, P32, P33 in which P25 is for MSB and P33 is for LSB. LEDs glowing for output 9 is shown in Fig.10.
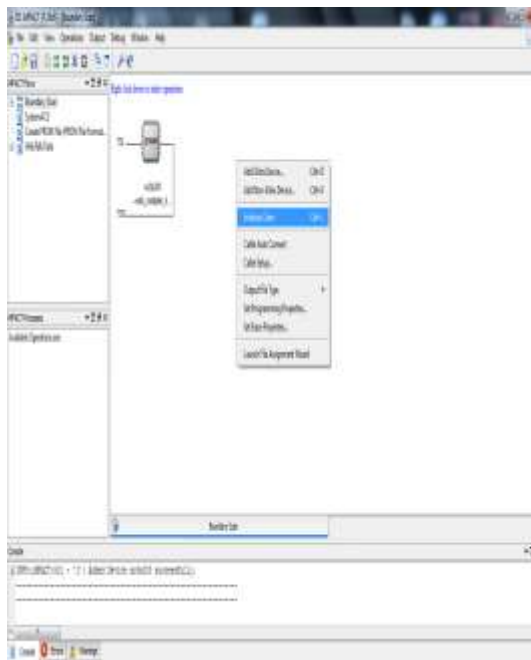

Fig.8

Step6: Now a message will appear in the message box as 'Boundary scan-chain validated successfully' and it started executing command as shown in Fig.9.

Fig.10 FPGA Implementation of 4x4bit Vedic multiplier on Spartan 3 FPGA kit

Another input-ouput combination is shown in Fig.11.

Fig.11

RESULTS

Simulation Results of 16x16bit Vedic Multiplier is shown in Fig. 12

Fig.12 Simulation Results of 16x16 bit Vedic Multiplier

Simulation Results of 32x32bit Vedic Multiplier is shown in Fig.13.

Fig.13 Simulation Results of 32x32bit Vedic Multiplier

IV. CONCLUSIONS

In our design, efforts have been made to reduce the area and propagation delay and achieved an improvement in the reduction of maximum combinational path delay with 51% when compared to array multiplier, booth multiplier and conventional Vedic multiplier implementation on XILINX software. It is coded in Verilog HDL and synthesized using XILINX ISE 14.1.

The proposed 32x32bit Vedic multiplier architecture has been designed, synthesized and successfully implemented using Spartan 6 XC6SLX4 FPGA board. The proposed Vedic Multiplier with Brent Kung Adder is compared with the existing Vedic multiplier using Kogge Stone Adder and ripple carry adder and can be inferred that proposed architecture is faster compared to existing Vedic multiplier. The work has proved that delay and area of proposed Vedic multiplier is less than the existing 32 bit Vedic Multipliers. In comparison with existing multiplier that is synthesized using Kogge Stone Adder, the delay of proposed 32x32bit Vedic Multiplier is reduced from 38.63ns to 30.001ns i.e. 22.337% reduction in delay and 5.190% reduction in area.

In future the proposed multiplier performance parameters can be improved by high level pipelining operations and applied in signal processing applications like image processing and video processing.

V. BENEFITS OF FPGA BOARD

1. The immediately obvious benefit of an FPGA board is the flexibility to quickly and easily configure programming in the course of development. These chips deliver better computing power than comparable alternatives, and are often more affordable.

2. It is more efficient to evaluate new product functionality and design using an FPGA board.

3. An FPGA board can perform both digital and analog functions, making it a versatile solution for engineers.

4. Some boards also support encryption to address security concerns raised by the essential flexibility of their architecture.

VI. APPLICATIONS

1. Due to the low cost and high performance, FPGA boards are now used for a wide variety of computing applications.

2. FPGA boards are also ideal for teaching electronics engineering and programming.

3. Amateur engineers can use an FPGA board to develop a variety of fun projects. These can include sound and music generators, LED displays and even games.

4. From the amateur hobbyist to the multinational corporation, tinkerers of all types are using the FPGA board to test new designs and ideas.

5. The field programmable gate array allows for rapid prototyping, testing and deployment. Many engineers today rely on FPGA board technology to explore innovative products.

VII. REFERENCES

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