Design and Performance Analysis of low Power Reversible Multipliers

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Abstract-*Multipliers are one the greatest significant component of numerous schemes. So we continuously need to find a superior solution in case of multipliers. Our multipliers must always consume a smaller amount of power and cover less power. So over and done with our project and try to control which of the three algorithms works the best. In this dissertation obtainable circuit alternatives related with enterprise of a 4x4 nameless digital multiplier in RL and delineated the reversible multiplier application of minimal complexity. Unquestionably, the 4x4 multiplication circuit can be rummage-sale as a structure block for building RL multipliers of a superior bit-width. As upcoming research, we plan learning methods for complexity minimization in RL array multipliers having great bit-width as well as RL operations of signed multipliers.*

I. INTRODUCTION

Multipliers are key mechanisms of many high presentation schemes such as FIR filters, microprocessors, digital signal processors, etc. A scheme's presentation is usually determined by the presentation of the multiplier because the multiplier is usually the slowest clement in the scheme. Furthermore, it is usually the most area overwhelming.

Hence, optimizing the haste and area of the multiplier is a main design issue. However, area and speed are typically conflicting restraints so that refining speed results typically in larger parts. As a result, a whole spectrum of multipliers with dissimilar area-speed constraints have been intended with fully similar. Multipliers at one end of the range and fully serial multipliers at the other end. In among are digit serial multipliers where single digits containing of numerous bits are functioned on. These multipliers have reasonable presentation in both speed and area. However, current digit serial multipliers have been plagued by complex switching systems and/or indiscretions in design. Radix 2^n multipliers which function on digits in a parallel fashion in its place of bits bring the pipelining to the digit level and avoid most of 'the overhead glitches. They

were presented by M. K. Ibrahim in 1993. These constructions are iterative and modular. The pipelining done at the digit level brings the advantage of constant process speed regardless of the size of' the multiplier. The clock speed is only strong-minded by the digit size which is previously fixed before the design is applied. [1]

II. BINARY MULTIPLIER

A Binary multiplier is an electronic hardware scheme used in digital electronics or a computer or other electronic method to achieve rapid multiplication of two numbers in binary demonstration. It is built using binary adders.

The instructions for binary multiplication can be stated as follows

1. If the multiplier digit is a 1, the multiplicand is basically derivative down and signifies the product.
2. If the multiplier digit is a 0 the creation is also 0.

For scheming a multiplier circuit we must have circuitry to deliver or do the following three things:

1. It must be capable classifying whether a bit is 0 or 1.
2. It must be capable of shifting left partial products.
3. It must be talented to add all the incomplete products to give the products as sum of partial products.
4. It should examine the sign bits. If they are alike, the sign of the product will be a positive, if the sign bits are opposite product will be negative. The sign bit of the product stored with above criteria should be displayed along with the product. [1]

Notations:

x – Multiple and

y – Multiplier

p – Product

Binary multiplication (eg. $n = 4$)

$$p = x \times y$$

xn − 1 xn − 2x1x0

yn − 1 yn − 2y1y0
p2 n − 1 p2 n − 2 p1 p0
x x x x x
x x x x y
– – – – – – – – – –
x x x x y0x20
x x x x y1x21
x x x x y2x22
x x x x y3x23
– – – – – – – – – – – – – – – – –
x x x x x x x x p

III. BOOTH MULTIPLICATION ALGORITHM

Booth Multiplication Algorithm for radix 2
Booth algorithm gives a process for multiplying binary numbers in signed –2's accompaniment demonstration.

I will exemplify the booth procedure with the following example:

Example 2_{ten} x $(-4)_{ten}$

$0010_{two} * 1100_{two}$

Step 1: Making the Booth table

From the two numbers, pick the amount with the minimum change among a series of successive numbers, and make it a multiplier.[2]

i.e., 0010 -- From 0 to 0 no alteration, 0 to 1 one alteration, 1 to 0 additional alteration, so there are two variations on this one 1100 -- From 1 to 1 no change, 1 to 0 one change, 0 to 0 no change, so there is only one change on this one.

I. Therefore, increase of 2x (– 4), where 2_{ten} (0010_{two}) is the multiplicand and $(-4)_{ten}(1100_{two})$ is the multiplier.
II. Let X = 1100 (multiplier)
Let Y = 0010 (multiplicand) Take the 2's complement of Y and call it –Y
–Y = 1110
III. Load the X worth in the table.
IV. Load 0 for X-1 value it must be the preceding first least important bit of X
V. Load 0 in U and V rows which will have the creation of X and Y at the end of process.
VI. Make four rows for all cycle; this is since we are multiplying four bits numbers.[3]

Step 2:

Booth algorithm necessitates inspection of the multiplier bits, and instable of the partial creation. Prior to the instable, the multiplicand may be added to partial creation, deducted from the partial produce, or left unaffected according to the next rules: [4]

Look at the first smallest important bits of the multiplier "X", and the previous least significant bits of the multiplier "X - 1".

I. 0 0 Shift only
   a. 1 1 Shift only.
   b. 0 1 Add Y to U, and shift
   c. 1 0 Subtract Y from U, and shift or add (-Y) to U and shift
   d. Take U & V together and shift arithmetic right shift which preserves the sign bit of 2's
II. Complement number. Thus a positive number remains positive, and a negative number remains negative.
III. Shift X circular right shift because this will prevent us from using two registers for the X value. [5]

IV. BOOTH MULTIPLICATION ALGORITHM FOR RADIX 4

One of the answers of understanding high rapidity multipliers is to improve parallelism which assistances to reduction the number of following control stages. The original form of the Booth algorithm (Radix-2) had two disadvantages. They are: (i) the amount of add subtract processes and the number of shift processes develops mutable and develops troublesome in scheming parallel multipliers. (ii) The algorithm develops incompetent when there are remote 1's. These glitches are overwhelmed by using modified Radix4[6]

Booth algorithm which scan cords of three bits with the procedure given below: [4]

I. Extend the sign bit 1 position if necessary to ensure that n is even.
II. Append a 0 to the right of the LSB of the multiplier.
III. Rendering to the value of all course, each Partial Product will he 0, +y , -y, +2y or 2y.

The negative standards of y are complete by taking the 2's accompaniment and in this Carry-look-ahead (CLA) fast adders are used. The multiplication of y is complete by instable y by one bit to the left. Thus, in any circumstance, in scheming an n-bit parallel multipliers, only n/2 partial crops are produced. [7][8]

V. REVERSIBLE LOGIC GATE

A reversible logic gate is a device which performs such a one to one mapping. If a reversible logic gate has N inputs, then to perform [9] one to one mapping, the number of outputs should also be N. Then this device is said to be a N × N reversible logic gate. The inputs are denoted by $I_1 I_2 I_3$ ... I_N and the outputs are denoted by $O_1 O_2 O_3$ ... O_N.[8]

VI. PROPOSED WORK

We proposed a new method to design a Multipliers using reversible gates. In this we design Multipliers using simple conventional gates and reversible gates MUX using Fredkin gates are also designed by using and in this chapter previous work is also described and shows how our proposed method is better than the previous design which are explained below.

A characteristic digital multiplier inputs two binary statistics, i.e. multiplicand $X = x_n - 1 \dots x_1 x_0$and multiplier $Y = y_{n-1} \dots y_1 y_0$and productions the product $P = P_{2n-1} \dots P_1 P_0$, which can be printed in the subsequent form:

$$P = \Sigma_{i=0}^{i=n-1} \Sigma_{j=0}^{j=n-1} (x_i y_j) 2^{i+j} \quad (3.1)$$

Operation of partial product group module and $n \times n$ multiplier necessitates $n \times n$ summands and accordingly AND logic processes. To instrument them reversely in a dense way, we can use either Peres gate (PG) or Toffoli gate (TG). For each of these gates, a continuous value of logic 0 has to be complete to the input C in order to instrument AND logic procedure. If we select PG as application basis, the multiplier bits can be spread along the row of PA gates finished direct joining among output P and input A of head-to-head PG gates. The multiplicand bits, though, cannot be broadcasted and therefore must be simulated by using an extra motherboard. [10]

Lemma 1. The smallest quantum difficulty of reversible circuit to produce four copies of four bits is 12.

Proof:

Because in reversible logic the amount of inputs generations the number of outputs and fan outs are not allowable, creating four copies of a bit x_i necessitates two FG, each of which consuming x_i as one input and zero as additional input. To produce these two copies of x_i another FG is desirable. Thus, the minimal number of $2x2$ gates to harvest 4 copies of x_i is 3. Since FG has QC of 1, the smallest QC of a reversible circuit that produces 4 copies of four dissimilar bits is 12. EOP The amount of gates in the fan-out cohort circuitry can be condensed by using 4x4 gates, such as F2G or BVF gate, as exposed in Fig.3.1. In any case, the smallest difficulty fan out generation motherboard has 8 gates and QC=12 but not 4 gates and QC=8, as [24] untruthfully intelligences. Thus, we claim that the negligible difficulty realization of partial product compeer's circuit based on PG (Fig.3.1) requires 24 gates, 28 continuous inputs, 20 garbage outputs and has the total quantum quality of 76. Now, if we realize the partial product age group module based on Toffoli gates, no additional circuit is essential.

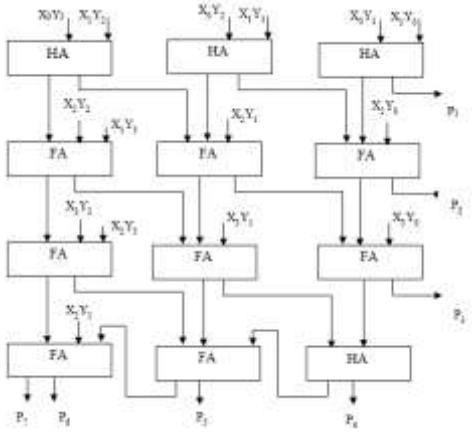
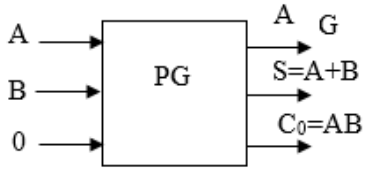


Figure 1: Addition array

Also, because TG gates have two undistinguishable inputs and outputs, their use permits broadcasting both the multiplicand bits and the multiplier bits after gate to gate, as exposed in Fig.1, thus plummeting the number of trash outputs as well. The only drawback of TG is large quantum cost. To decrease the total quantum cost of the circuit, we suggest substituting TG by PG at the end of data transmission. This progresses the QC by 4 deprived of any influence on the other limits. [10]

To device the reversible FA, we can usage two Peres gates mutual together as shown in Fig.2 (b) or a single 4x4 gate, such as HNG [10], PFAG, etc., particularly industrialized to achieve the full adder process. Both these replacements utilize a single continuous input and have 4 output lines. Since only two outputs of each FA are used in the addition array, both reversible implementations produce two "garbage outputs" per FA. As entitlements, the reversible FA enterprises founded on HNG, PFAG, or new gates described in have same circuit difficulty and QC of 6, whereas the QC of FA realized by two PG gates is 8. [10]



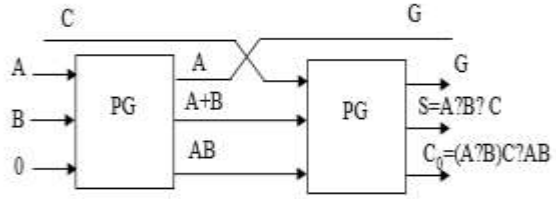


Figure.2: Reversible circuit of Half Adder (a) and Full Adder (b) [10]

Lemma 2. The minimum number of garbage outputs in an addition array of 4x4 unsigned reversible multiplication circuit is 20.[10]

Proof:

The accumulation array uses 16 inputs for summands produced by PPGC and 12 control inputs to withstand reversibility on 12 gates. Since in any reversible circuit the amount of outputs generations the amount of inputs, a 4x4 nameless reversible multiplier must have 28 outputs, amongst which only 8 are used to output the produce bits. Hence the least number of garbage productions in the array is 20. EOP. [10]

VII. PROPOSED MULTIPLIER

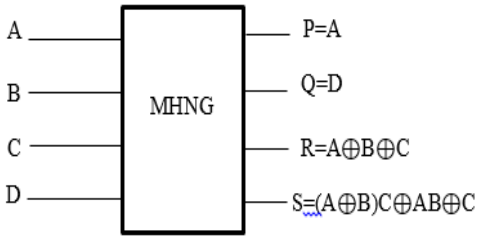


Figure 3: MHNG Gate

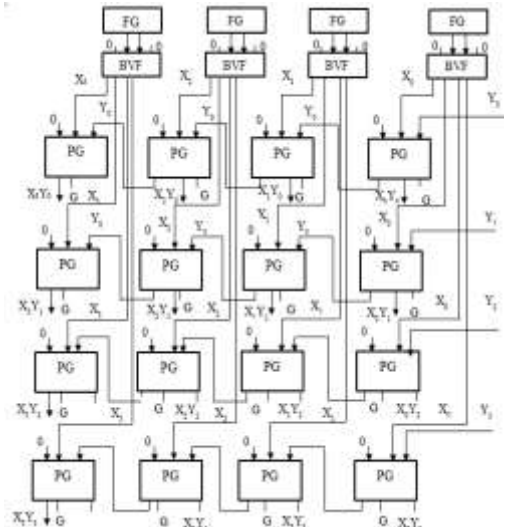
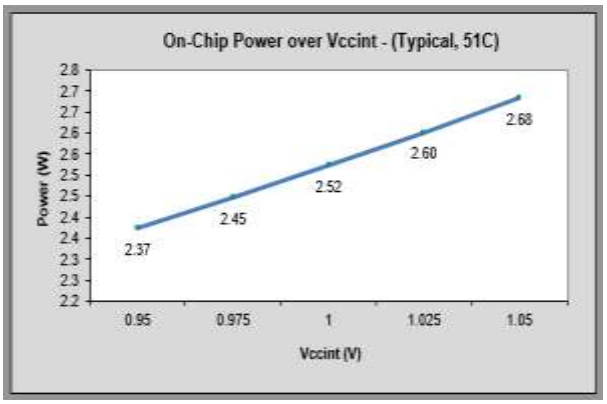


Figure 4: Partial product generation circuit 1 [10]

VIII. RESULTS



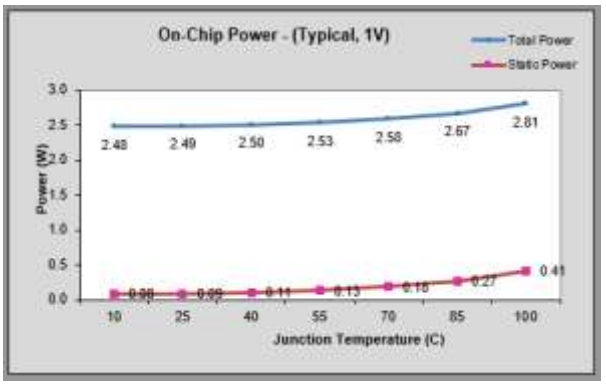
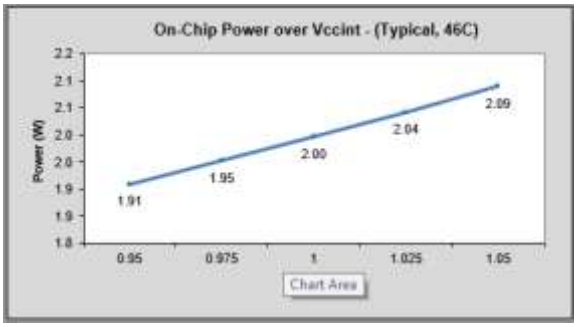


Figure 5: Graphs showing power estimation for Addition Array using Existing methods



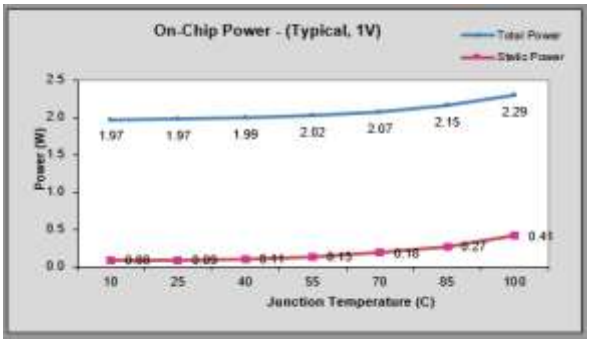


Figure 6: Graphs showing power estimation for Modified Addition Array

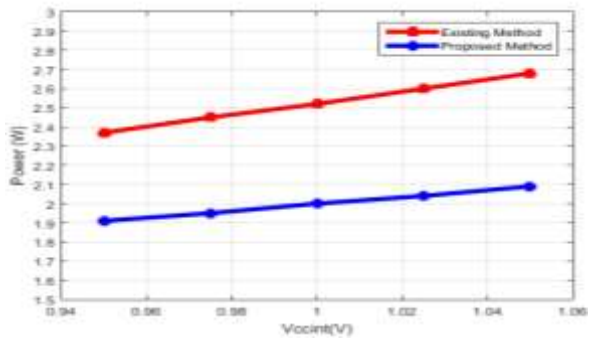


Figure 7: Comparison of Power vs. Vccint for Addition Array and Modified Addition Array

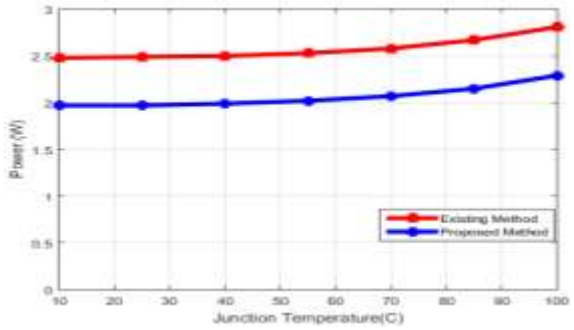
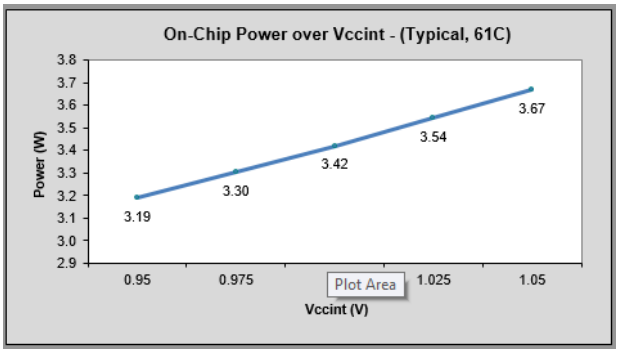


Figure8: Comparison of Power vs. Junction Temperature for Addition Array and Modified Addition Array



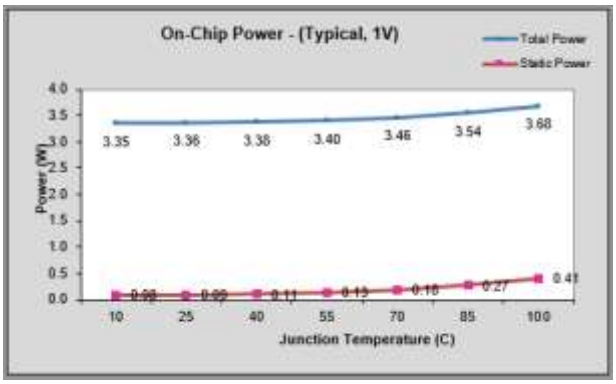
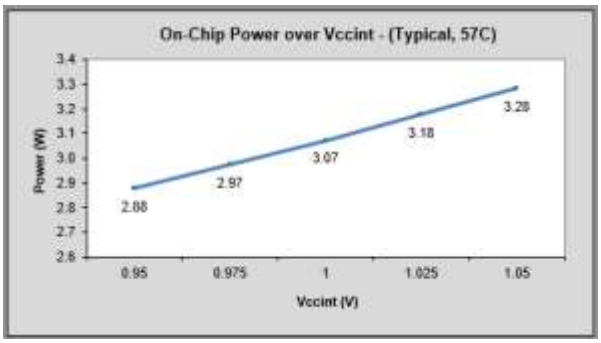


Figure 9: Graphs showing power estimation for 4x4 Urdhva Tiryagbhyam Multiplier Unit



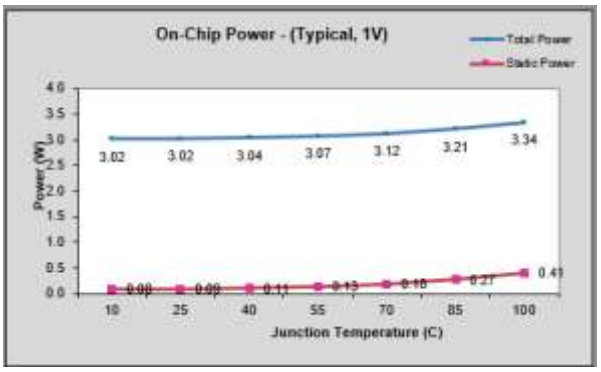


Figure 10: Graphs showing power estimation for Modified 4x4 Urdhva Tiryagbhyam Multiplier Unit

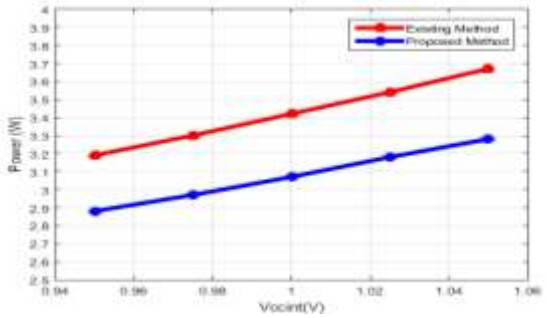


Figure 11: Comparison of Power vs. Vccint for 4x4 Urdhva Tiryagbhyam Multiplier Unit and Modified 4x4 Urdhva Tiryagbhyam Multiplier Unit

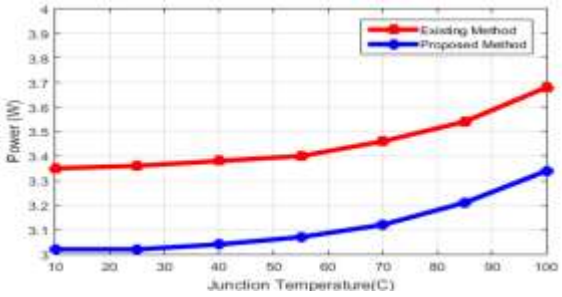
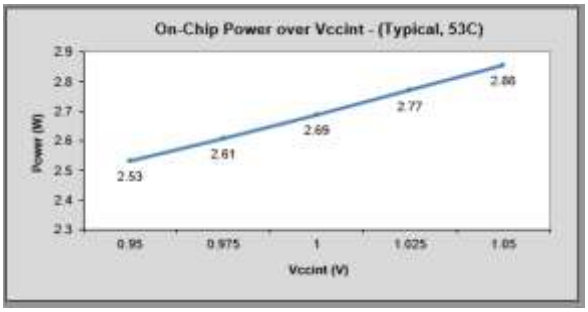


Figure 12: Comparison of Power vs. Junction Temperature for 4x4 Urdhva Tiryagbhyam Multiplier Unit and Modified 4x4 Urdhva Tiryagbhyam Multiplier Unit



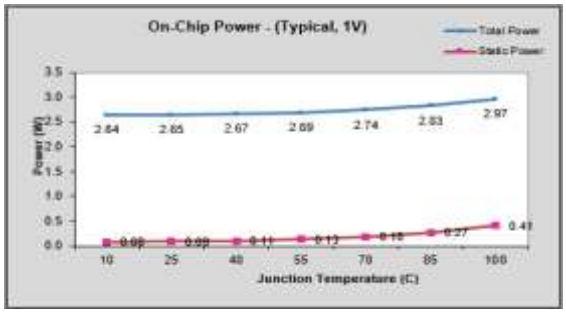
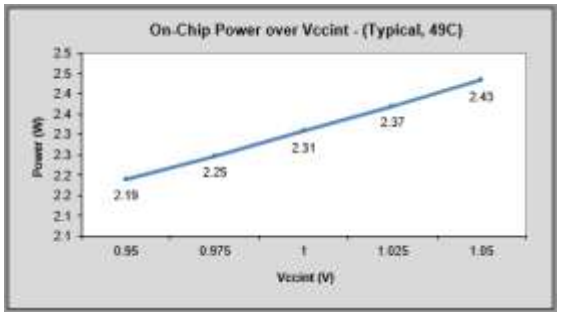


Figure 13: Comparison of Power vs. Junction Temperature for 4x4 Urdhva Tiryagbhyam Multiplier Unit and Modified 4x4 Urdhva Tiryagbhyam Multiplier Unit



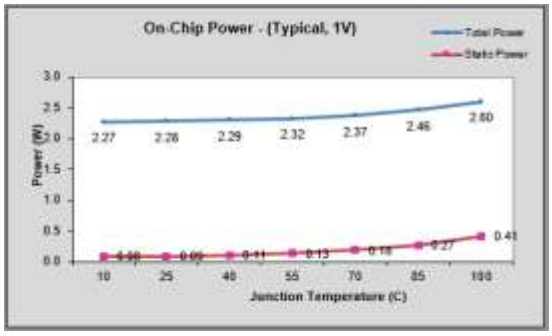


Figure 14: Graphs showing power estimation for Modified Ripple Carry Adder using MHNG gates

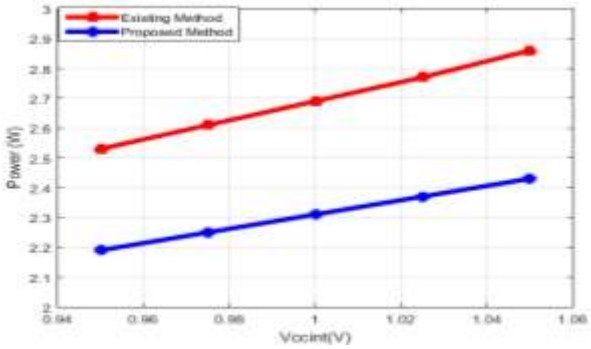


Figure 15: Comparison of Power vs. Vccint for Ripple Carry Adder and Modified Ripple Carry Adder

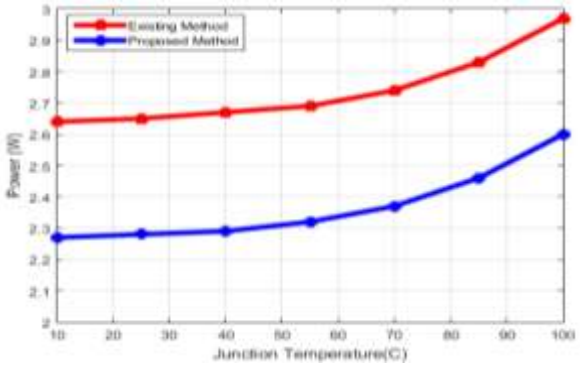


Figure 16: Comparison of Power vs. Junction Temperature for Ripple Carry Adder and Modified Ripple Carry Adder

Table 1: Comparison table of proposed multipliers and existing multipliers in terms of Quantum Cost

Circuit Name		Quantum Cost
Multiplier using Method I	Existing Results	140
	Proposed Results	132
Multiplier using Method II	Existing Results	143
	Proposed Results	135
Vedic Multiplier (Method III)	Existing Results	156
	Proposed Results	144

Table 2: Comparison table of proposed multipliers and existing multipliers in terms of Power Estimation

Circuit Name		Power (W)
Addition Array	Existing Results	2.52
	Proposed Results	2.00
4x4 Multiplier Unit	Existing Results	3.42
	Proposed Results	3.07
Ripple Carry Adder	Existing Results	2.69
	Proposed Results	2.31

IX. CONCLUSION

Multipliers are one the most significant factor of many organizations. So constantly need to discover a better solution in circumstance of multipliers. Our multipliers must permanently consume less power and cover less power.

In this dissertation accessible circuit alternatives related with design of a 4x4 unsigned digital multiplier in RL and drew the reversible multiplier operation of minimal complication. Undoubtedly, the 4x4 multiplication tour can be used as a building block for building RL multipliers of a superior bit-width.

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