A Efficient Low-Power High Speed Digital Circuit Design by using 1-bit GDI Full Adder Circuit

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Abstract **-** *To achieve low power consumption with less area, static CMOS logic styles has become the most suitable design approach for the past three decades. New designs of GDI based basic digital (AND, OR, XOR) gates are presented using single pass transistors to improve proper swing level of the output waveform of GDI gates. The new design of basic gates with combination pass transistor and GDI logic form a hybrid GDI technique. In such designs of hybrid GDI gates, pass transistors are activated only in cases where threshold drop occurs at the output. In this paper we presented a new 13T full adder design based on hybrid –CMOS logic design style. Proposed new design is compared with some existing designs for power consumption, delay, PDP at various frequencies viz 10 MHz, 300 MHz and 1 GHz. From the simulation results, it is observed that, hybrid GDI based digital circuits consumes less power, delay and area as compared to static CMOS based circuits. Proposed technique shows less power dissipation and less propagation delay as compared to existing GDI technique with slight increase in area. it shows less power and less delay with about 60% area increase as compared to basic GDI.*

Keywords — *C-CMOS, CPL, Hybrid Adder, GDI, Floating adder.*

I. INTRODUCTION

For many designs, optimization of power is important as timing due to the need to reduce package cost and extended battery life. Power optimization is possible at each level of design process from higher architecture level to lower physical level [1,2]. Although over the past several years, silicon CMOS technology has emerged as the most dominant fabrication process for relatively high performance and cost effective VLSI circuits, the revolutionary nature of new systems such as the wired and wireless communication technologies, high performance imaging systems, smart appliances and the like are constantly challenging the boundaries of various technological fronts including silicon CMOS. The technology is continuously and rapidly evolving the production of smaller systems with minimized power dissipation, the IC industry is facing major challenges due to constraints on power density (W/cm^2) and high static (standby) and dynamic (operating) power dissipation [3]. The key to overcome these challenges lies in improvements in design, material and manufacturing processes.

Full adder proves to be the nucleic element in many complex arithmetic operations such as addition, subtraction, multiplication, division, exponentiation etc [1,2]. The critical path in such applications usually goes from carry-in to the carry-out of the full adders [3]. Hence the generation of carry out signal must be fast. Slower generation of carry out signal leads to increased worst case delay, increased glitches in the later stages resulting in higher power dissipation. Also in a full adder it is desired to generate the sum and carry outputs simultaneously to minimize the glitches in the lower stages [4-6].

The ever-increasing trend of battery operated portable devices have inspired the development of several logic styles over the years with reduction of power consumption and enhancement of speed as the central goals. The first design is the conventional static CMOS full adder [7] which utilizes regular CMOS structure. The conventional pull up and pull down transistors provide full swing output and good driving capability. The main drawback of the design is high input capacitance and degraded speed due large number of PMOS transistors which also account for more area. Another conventional design uses complementary pass transistor logic(CPL) [7], which results in full swing output and good driving capability along with high speed on the cost of increased number of transistors and internal nodes due to which CPL adder have high power dissipation.

In 2002, GDI technique shows great potential as an alternative to Standard static CMOS Logic [4]. The design methodology of GDI technique allows the use only two transistors for designing various complex logic functions. It is written in different research papers, that the total layout area and dynamic power dissipation of GDI digital logic are reduced, as compared to static CMOS designs [8,9]. Similar to other design styles, the GDI circuits

suffered from a reduced swing due to threshold drops. However, a significantly reduced transistor count and the logic flexibility of the basic GDI cell provided significant power reduction, despite the need for swing restoration circuits. This research analysed the different aspects, reasons and effects of swing restoration problem and find the alternate way of buffer as swing restoration circuits.

The floating adder [10] is another low power high speed full adder circuit which works well at high frequencies. Its low power characteristics and performance stability at frequencies as high as 1 GHz is of great advantage at such high speeds. The disadvantage of the floating adder is that it produces weak '0' and '1' at sum and carry output respectively.

II. LITERATURE REVIEW

CONVENTIONAL ADDER

One bit full adder is a combinational circuit that forms the arithmetic sum of three input bits. It consists of three inputs and two outputs. Two inputs (A, B) are the bits to be added, the third input (C_{in}) represents the carry form the previous position. Two outputs are sum (S) and output carry (C_{out}). Truth table for full-adder is shown in Table 1.

Table 1: Truth Table of Full-Adder

A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Simplified expression for the output variables sum (*S*) and output carry (C_{out}) are given in following equations [3]:

$$S = (A \oplus B) \oplus C_{in} \quad (2.1)$$

$$C_{out} = (A \oplus B)C_{in} + (\overline{A \oplus B})\,A \quad (2.2)$$

From the above equations, the logic diagram for full adder can easily drawn in Fig. 1. The full adder is implemented by two XOR gates, two AND gates and OR gate. The given XOR gates are used to obtain the sum output of the full-adder and other logic gates are used to get the carry output of the full-adder.

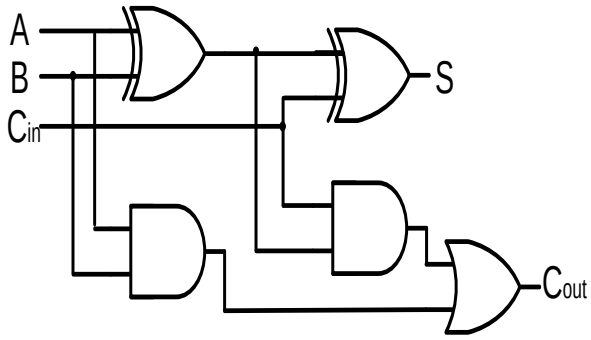

Fig. 1: Gate level logic diagram of full adder

COMPLEMENTARY PASS TRANSISTOR LOGIC (CPL)

The complementary pass transistor logic based full adder [7, 15] consists of 32 transistors in a dual rail structure. CPL adder provides high speed operation due to the fast differential stage of the cross coupled PMOS transistors and The static output inverters used in this adder contribute towards the full swing output, hence good driving capability of the full adder. the increased number of internal nodes and static inverters lead to increase in leakage and static power dissipation due to which large power consumption occurs in the adder which makes it obsolete for low power applications.

GDI ADDER

In 2002, GDI technique shows great potential as an alternative to Standard static CMOS Logic [4]. The design methodology of GDI technique allows the use only two transistors for designing various complex logic functions. It is written in different research papers, that the total layout area and dynamic power dissipation of GDI digital logic are reduced, as compared to static CMOS designs [4]. Similar to other design styles, the GDI circuits suffered from a reduced swing due to threshold drops. However, a significantly reduced transistor count and the logic flexibility of the basic GDI cell provided significant power reduction, despite the need for swing restoration circuits. This research analysed the different aspects, reasons and effects of swing restoration problem and find the alternate way of buffer as swing restoration circuits is shown in the Fig. 2.

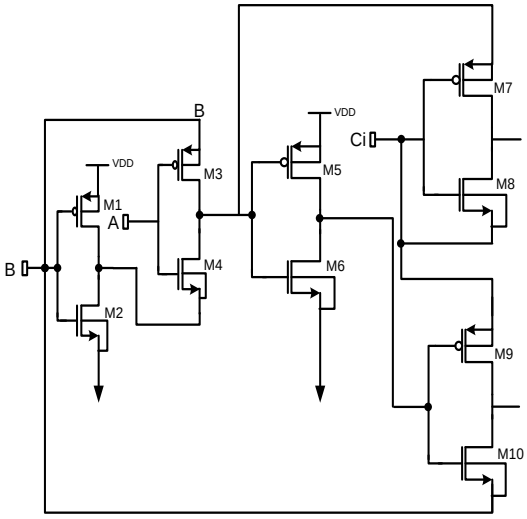

Fig.2. One bit GDI full adder

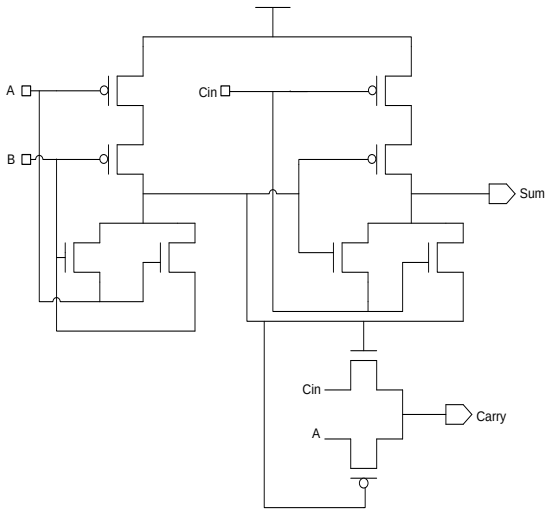

Fig.3. Schematic of SERF Full Adder

STATIC ENERGY RECOVERY FULL ADDER (SERF)

Design is compared with basic Static Energy Recovery Full adder (SERF) cell technique it consist of 10T transistor for energy recovery without providing any ground path to the circuit. Implemented of SERF technique to design 5 different topologies of full adder has been done using various Boolean equations. Performances of different full adders are compared with GDI, CMOS and PTL techniques at 0.25µm CMOS technology. Comparative parameters are delay, transistor count, power dissipation, AT (product of area and transistor count), AT^2 and PD (power- delay product). They conclude that pass transistor logic consumes more power as compared to other techniques due to low threshold drop across a single channel pass transistor. Overall from the simulation results shows that SERF technique save power consumption and delay for all adder topologies, when compare to existing GDI, CMOS and PT logic. No direct pathe to the ground energy of the circuit is saved with proper logic generation from the total power equation [11]. The combination of not having a direct path to ground and the re-application of the load charge to the control gate makes the energy recovering full adder an energy efficient design. To the best of our knowledge this new design has the lowest transistor count for the complete realization of a full adder.

FLOATING FULL ADDER

This adder utilizes 8 transistors for the design of an adder circuit if both input and its complements are available and uses 12 transistors if complement of the inputs is not available.

As can be seen from the figure, two of the internal nodes (X and Y) are not directly connected to any of the inputs, hence called floating adder. Power in the circuit is reduced due to the reduced switching activity in the circuit. The adder proves to be a promising design for high speed and low power circuit design and have good performance stability against high frequency. The main drawback of the circuit is the degradation of output voltage levels due to the inability of pmos and nmos transistors to pass 0 and 1 respectively. the weak '0' and '1' at the sum and carry out put respectively lead to poor driving capability but this can be sorted out using buffers at the output stages[10].

HYBRID ADDER

The hybrid logic style exploits the advantages of different logic styles to get the desired performance from an adder. In hybrid logic style the full adder is divided into different modules as shown in Fig.4 and different design styles are used to optimize each module[8],[11],[12].

Module 1 generates XOR and XNOR functions of inputs A and B, as intermediate outputs module 2 and module 3 consist of the circuitry that utilizes these intermediate signals along with Cin signal to generate the sum and carry outputs [13]. A 16 transistor hybrid adder[14].

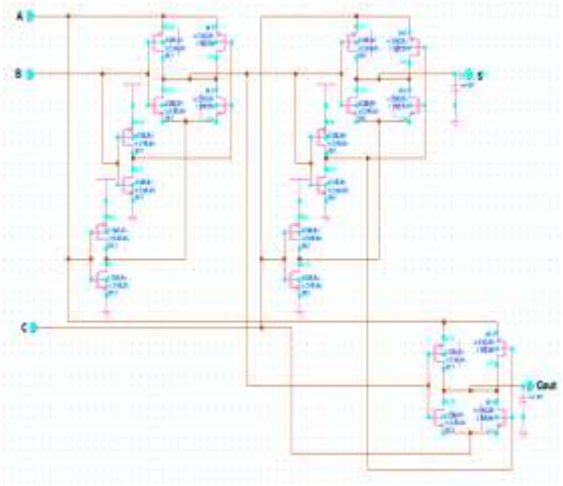

Fig.4. A 16 Transistor Hybrid adder

The hybrid adder shown gives full swing output at high frequencies and satisfactory performance stability performance stability at high speeds. This adder utilizes 16 transistors however we can reduce it to get reduced area and power of the circuit[14].

III. PROPOSED ADDER CIRCUIT

In proposed Hybrid GDI based design of XOR gate, the number of transistors required to design basic gates in Hybrid GDI is less as compared to both CMOS and GDI technique. In over proposed circuit we have generated XOR and XNOR operation with the help of three transistor (3T), when XOR pass through inverter it generate XNOR operation. Intermediate XOR and XNOR are generated using three transistor (3T) XOR and XNOR gate. Sum and Carry are generated using two double transistors multiplexers. 3T XOR and XNOR consume high energy due to short circuit current in ratio logic. Propagation delay of Hybrid GDI based XOR gate is less than CMOS but more in XNOR. Hence the total power delay product (PDP) value is also less only in OR gate. The trade-off between power and area is measured using PDP value of circuit and it should be as low as possible. The number of transistors required to design basic gates in Hybrid GDI is less as compared to both CMOS and GDI technique. Hence it occupies least area also. The PTL technique shows improved result as compared to Hybrid GDI but it suffers from low threshold problem since it contains only nMOS transistors in its design and here the PTL design is considered without swing restoration circuits.

In Hybrid GDI based XOR gate, one more GDI cell has been added which is controlled by inverted input gate signal of first GDI cell. When A = 0, pMOS of GDI cell 1 and nMOS of GDI cell 2 conducts simultaneously. When B = 0, GDI cell 2 acts as an inverter and provides inverted input signal A at output end. It means, for B = 0, A = 0, XOR out is '1' and for B = 0, A = 1, XOR out is '0'. Similarly when B = 1, GDI cell 1 act as an inverter and for B = 1, A = 0, XOR out is '1' (V_{dd}) and for B= 1, A = 1, XOR out is '0'.

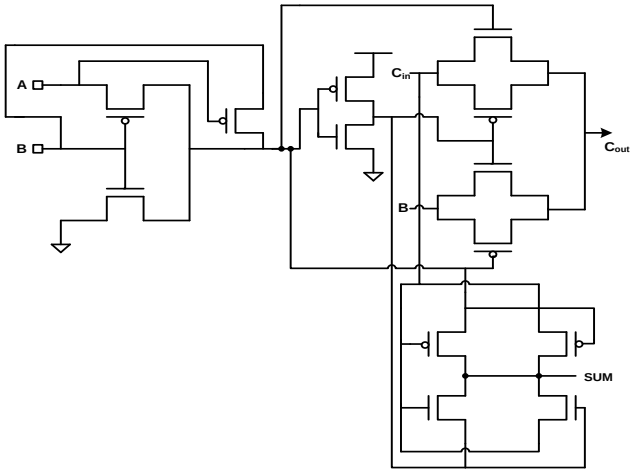

Fig 5. Proposed 13T Hybrid GDI Adder Circuit

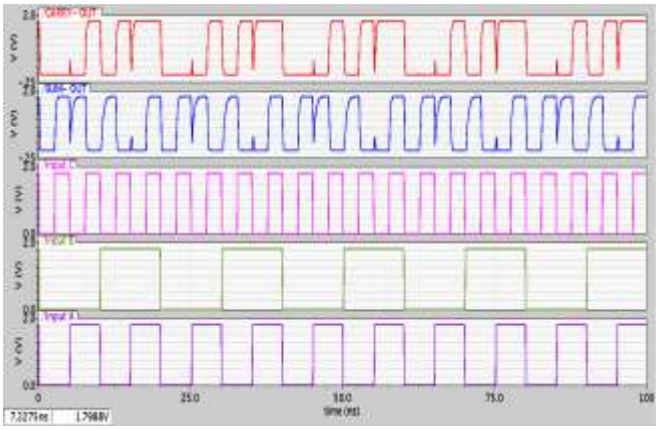

Fig 6. Output Waveform of Proposed Circuit

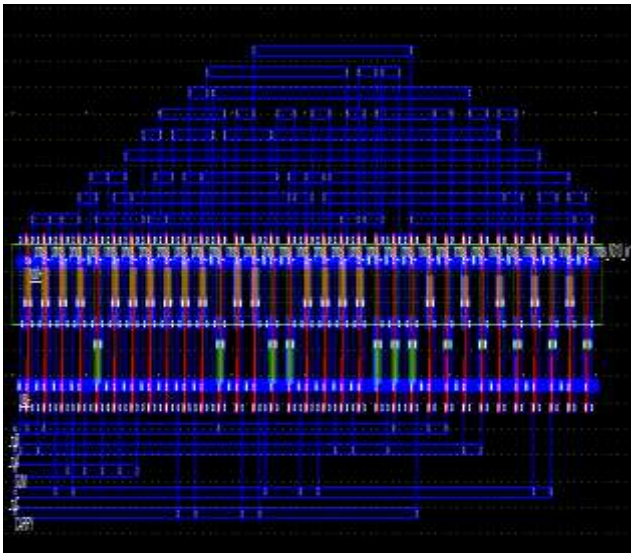

Figure 7: Layout of hybrid GDI based full adder

IV.SIMULATION RESULTS AND DISCUSSION

All the existing and proposed circuit is simulated Circuits are designed with transistor size of W = 240 nm and L = 180 nm. The transient analysis is done using Cadence Spectre at 1.8 volts. Area is calculated from layout design in Microwind tool. Power consumption is calculated with the variation of frequency at lower frequency (10MHz), middle frequency (300MHz) and high frequency (1GHz). The size (W/L ratio) of the transistors (N-CMOS and P-CMOS, respectively) is set to be the same, so that the comparison of power dissipation between different types of adder circuits is distinct. Hybrid GDI consumes 12% and 3% less power than CMOS and GDI technique. Delay is also less, 47% and 58% than other techniques. Figure of merit, the PDP is also less, 53% and 58% than CMOS and GDI respectively. Number of transistors and hence area occupied by Hybrid GDI based full adder is very less. The reason behind all improved parameters is the design of full adder with less number of transistors. Due to less transistors, the load capacitance is also low and so the switching capacitance that result less consumption of average power. Here, same inverted gate signal is applied to control the swing restoring pass transistors of XOR and OR gates. This reduces number of transistors and hence power and delay.

Table I Power consumption and Delay of existing and proposed adders circuit at 10MHz

Adder structure	Power (µW)	Delay (pS)	PDP (fWS)
Conventional	3.903	98.46	0.384
GDI Adder	2.449	31.48	0.077
SERF	3.494	24.18	0.084
8T	2.682	23.20	0.062
6T	3.128	20.06	0.062
Floating adder	3.903	12.44	0.048
Hybrid adder	4.103	6.706	0.027
Proposed adder	1.890	6.502	0.012

Table II Power consumption and Delay of existing and proposed adders circuit at 300 MHz

Adder structure	Power (µW)	Delay (pS)	PDP (fWS)
Conventional	7.778	97.22	0.075
GDI Adder	4.966	30.26	0.150
SERF	4.033	33.12	0.133
8T	6.148	25.82	0.158
6T	4.193	24.04	0.100
Floating adder	6.959	6.994	0.048
Hybrid adder	8.763	6.724	0.058
Proposed adder	5.354	6.589	0.035

Table II : Power consumption and Delay of existing and proposed adders circuit at 1GHz

Adder structure	Power (µW)	Dela y (pS)	PDP (fWS)
Conventional	37.31	79.52	2.966
GDI Adder	24.22	29.28	0.709
SERF	39.31	30.43	1.196
8T	45.63	21.32	0.972
6T	41.19	21.34	0.878
Floating adder	33.78	6.083	0.205
Hybrid adder	44.32	6.728	0.298
Proposed adder	30.35	5.583	0.169

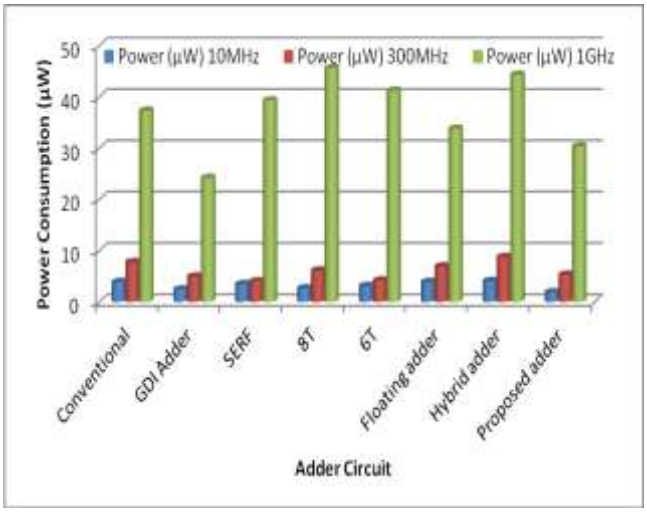

Fig.8. Average power consumption of existing and proposed Adder Circuit

IV. CONCLUSION

Basic gates and important building blocks of digital systems such as full adder, carry propagate adder, magnitude comparator, arithmetic logic unit, binary multiplier and booth encoded multiplier are designed using Hybrid GDI gates. The basic gates like two-input AND, OR and XOR gates are designed using conventional standard CMOS technique, other parallel techniques such as PTL, TG and existing GDI technique. The Hybrid GDI technique is strong alternative of CMOS for digital circuit design but it suffers from low threshold drop problem, existing GDI technique and proposed Hybrid GDI technique. Simulation result shows less power dissipation, less propagation delay and less area of proposed technique as compared to conventional CMOS technique. Also proposed technique shows less power dissipation and less propagation delay as compared to existing GDI technique with slight increase in area.

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