Design of Operational Amplifier in 45nm Technology

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Abstract-*This paper presents the designing and performance analysis of Operational Transconductance Amplifier using the 45nm Technology from mosis foundry. This transconductance design is having a biasing current of 5μA with supply voltage of ±1 V. The open loop gain obtained from this design is about 66.5 dB with UGB of 22 MHz is obtained from this design. This OTA design has a CMRR value of 74 dB and PSRR of 70 dB with Power dissipation of 68 μW and Slew Rate 5 V/μsec. Simulation is done using UMC 45nm technology file.*

Keywords— *Cadence, OperationTransconductance Amplifier (OTA), Slew Rate, Power Dissipation, Common mode rejection ratio.*

1. Introduction.

In recent world mostly we deals with the digital signals but most of the signals are analog in nature. So we need a device which can convert analog signals into the digital signals. Hence, for converting analog signals into digital we need an analog to digital converter and after converting we process the digtital signals using DSP[1]. Comparator is the Main building block in block in analog to digital converter. It compares the two analog signals and based upon the different conditions produce a binary value either logic 0 or logic 1. Comparator is the most important design for various applications like image and signal processing, general purpose processor, embedded processor; Build in self test (BIST) [2,3]. There are various approaches for designing the comparator. Each approach have its own operating speed, Power consumption and circuit complexity[4]. In the conversing process, the first step is to take the sample of input signals. Sampled signals are applied to the comparator circuits to find the binary equivalent of analog input signals. In today's world it is very important to develop different design techniques to reduce the power consumption and area required [5]. In this paper we will reduced the power and area using the 45 nm technology. Operational transconductance amplifier is different based upon the output from the convental operational amplifier. In Two stage amplifier it is not sue that improved phase margin will give better response always[6]. In transconductance operational amplifier output comes in the form of current and in case of convential operational amplifier output comes in the form of voltage. Operational Transconductance Amplifier are used in many application like Filter circuits, Instrumentation and control circuits, Neural networks, Analog to Digital Converter, Comparator[7]. In CMOS circuit power consumption may be dynamic or static in nature. dynamic power consumption happens with the transistor switching and static power consumption exists without the transistor switching. We can design the half adder and full adder by hybridzing PTL and GDI Techniques in vlsi design and make the area and power efficient [8,9]. This operational transconductance amplifier will work as a comparator and various approaches used in the designing of comparator. Based on the different approaches power consumption, speed, and circuit complexity will depends [10]-[12].

In this paper we describe design of OTA amplifier and this design is done in 45nm technology. The paper represents the following section: Section 2 describes the different stages of Operational Amplifier. Section 3 describes various parameters of two stage amplifier. Section 4 represents the various simulation results and section 5 and section 6 describe the conclusion and references section.

II. Two Stage Operational Transconductance Amplifier Design.

Two Stage Amplifier consist of three stages Differential amplifier stage, Bias Stage, and Output buffer stage.

A. Differential Amplifier Stage

As shown in figure Fig. I, the CMOS transistors PM0, PM1, NM0, and NM1make the Differential amplifier stage. NM0 and NM1 are NMOS transistors in which gate will act as a differential input node. Gate terminal of NM0 is the inverting input as well as the gate terminal of NM1 is the non-inverting input. In this Differential amplifier stage current will be reflected fromNM0 by the PMOS transistors PM1 and PM0. Reflected current will be subtracted from the current flowing through the transistor NM1.This reflecting topology is used to convert the differential input signals into single ended output signal.

B. Bias Stage

As shown in figure the Bias stage of the architecture is designed by the NMOS transistors NM2 and NM3 that deliver a voltage between the source and gate terminal of NM5 and NM2. NM2 and NM3 are diode connected so it assure that both will work in the saturation region. Biasing required for the remaining transistors is controlled by their node voltage

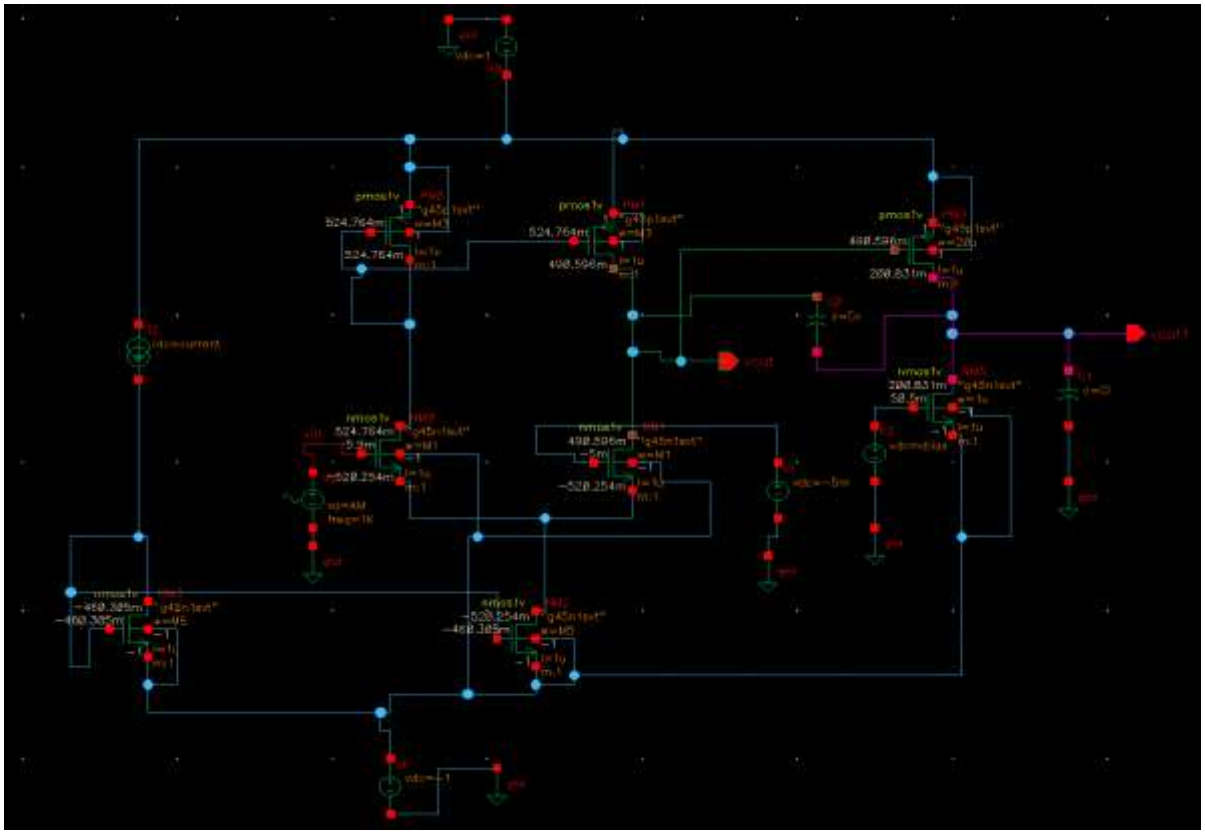

Figure: 1 Two Stage Amplifier

C. Output Buffer Stage

This Stage consist of transistor NM5 and PM3 as shown in figure I. This stage will provide additional gain to the amplifier. The output of differential amplifier stage will be the input for this stage. The gain achieved from this stage will be the product of trans- conductance of PMOS transistor PM3 and load resistance i.e. the output resistance of NM5 and PM3.

III. OTA Parameters

There are various parameters that we will discuss in this paper like Slew rate, Power dissipation, Gain margin, Common mode rejection ratio (CMRR), Phase margin, Gain Bandwidth.

A. Slew Rate

It is defined as the rate of change of output voltage per unit change in time. The unit of slew rate is V/µsec.

Slew Rate = 2. π. f.V

Where
f=the highest signal frequency, Hz
V = peak voltage of the signal.

B. Power Dissipation

Power dissipation is the summation of total dc power supplied and power delivered from the device to the load.

C. Common Mode Rejection Ratio

It is the relationship between the differential voltage amplification stage to the common mode voltage amplification stage. CMRR value ideally should be zero.

D. Unity gain bandwidth

It is defined as the range of frequencies under which open loop gain becomes unity. Beyond this range no more gain can be produced by the opamp.

E. Input common mode voltage range

It is defined as the input voltage ranges over which operational amplifier (OTA) will not work properly. So for normal operation of Operational Amplifier this value should not be exceeds from the specified range.

F. Common Mode Gain

Common mode gain is also referred as common mode voltage amplification. It is the relationship between output voltages to the input supplied voltage, when both the terminals of the op-amp are supplied same potential is known as common mode gain of op-amp.

IV. OTA Design Simmulation.

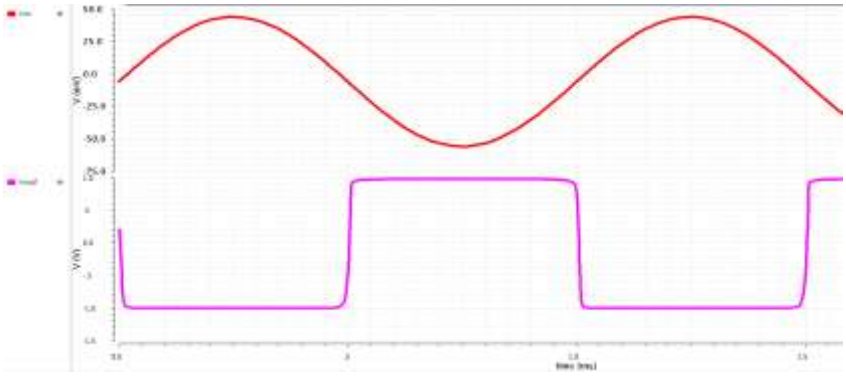

Fig. 2 Input & Output waveform/Signal (Transient Analysis)

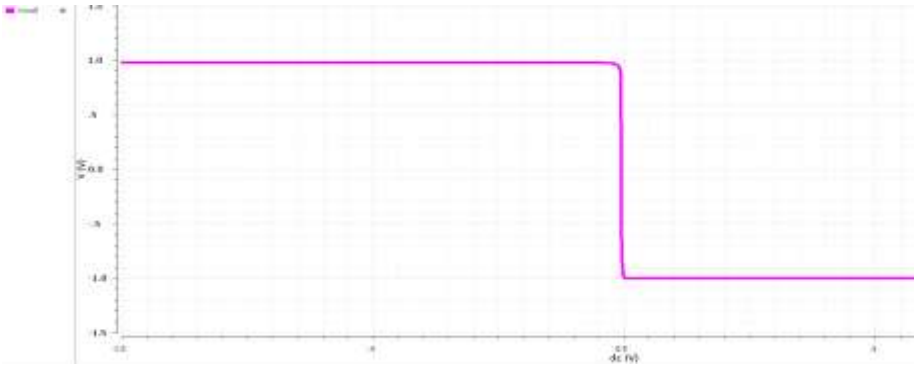

Fig. 3 VTC Curve (DC Analysis)

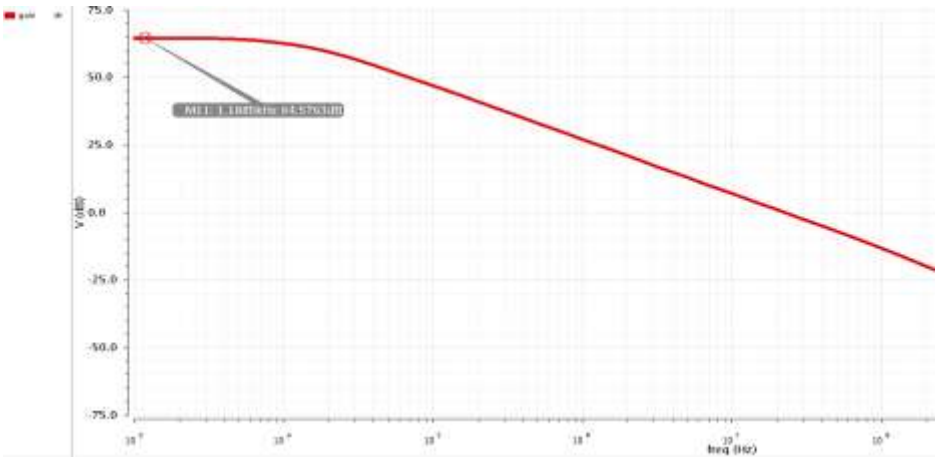

Fig. 4 Frequency Response (AC Analysis)

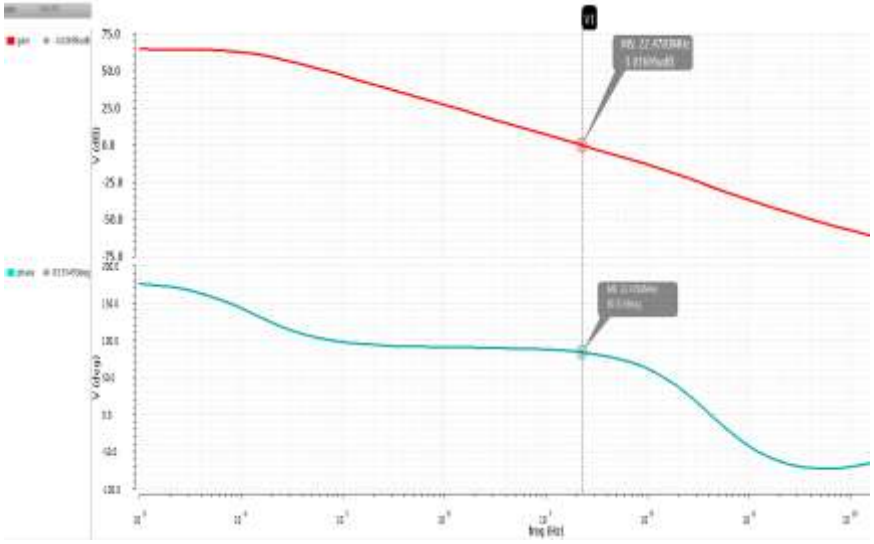

Fig. 5 Gain(db) & Phase(deg) Plot

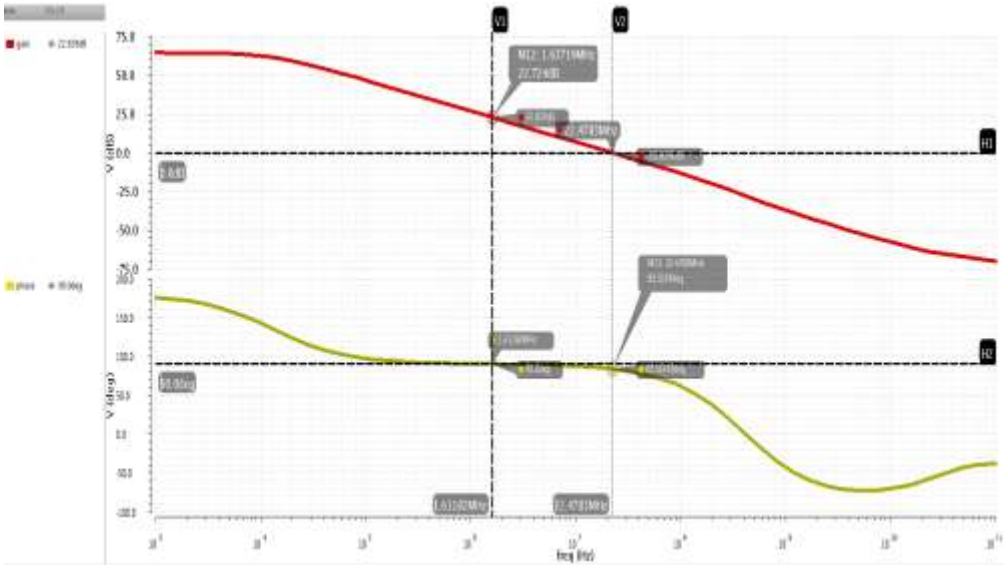

Fig 6.Calculating Gain Margin & Phase Margin

Table I. Parameter values for OTA

Parameter	Existing Work[13]	Proposed Value
CMOS technology	45nm	**45nm**
Open loop gain	52.68 dB	**66.5 dB**
Supply voltage	±1 V	**±1 V**
Load capacitance	10 pF	**10 pF**
PSRR	NA	**70 dB**
CMRR	59.432 db	**74 dB**
Power Dissipation	1.735 mW	**68 µW**
Slew Rate	NA	**5 V/µsec**
Gain Margin	NA	**30 dB**
Phase Margin	60.9652°	**61°**
Unity Gain BW	NA	**22 MHz**

V. Simmulation Result& Comparision

The Transient response of OTA design is shown in figure 2. Figure 3 shows VTC curve for this analysis. The frequency response (AC analysis) is shown in figure 4. Figure 5 shows the gain and phase plot of OTA design. Figure 7 shows calculation of gain and phase margin.The design of this Operational Transconductance Amplifier (OTA) is done using Cadence Tool. The Simulation results are done using Cadence Spectre Environment using UMC 45nm CMOS technology. The simulation result of the OTA shows that the open loop gain of 66.5 dB is achieved using 45nm technology. This design gives the 74db value of CMRR and GBW of about 22 MHz. Table given below shows the various result of this OTA design. This design worked on the supply voltage of **±1 V.**When we compare with the Existing work powe dissipation will be descreased and gain will be increased significantly .In the proposed work CMRR value of 74 db and PSRR value of 70 db is achieved which are used for various low power applications.Gain margin and phase margin has also been improved in the proposed work. Hence this OTA design will give the better performance.

VI. CONCLUSION

This paper presents a OTA with supply of **±1 V** and power dissipation 68 (µW). This proposed circuit we can use for various low voltages, low power applications. In this paper we apply different technic to improve the gain and to minimize the power dissipation.

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