Design &Analysis of Full Subtractor using 10T at 45nm Technology

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***Abstract*—*In this paper, a 1-bit full subtractor is designed. In VLSI, a digital circuit can be design with different techniques and most popular techniques are conventional CMOS technique, GDI technique and MTCMOS technique. We prefer a circuit which have minimum number of transistor with good performance, less power consumption, less propagation delay and fast switching. In this paper, a full subtractoris designed using XOR gate and GDI technique. The technology node used is 45nm. Transient analysis for XOR gate and GDI technique based full subtractor is performed. In analysis, we found that the full subtractor designed with XOR gate uses less number of transistor and consume less power than GDI technique based full subtractor.Full subtractor using XOR gate uses 10T where GDI based uses 14T. Power consumption and time delay is improved by 36.04% and 36.13% respectively when compared with GDI based full subtractor.*

Keywords*—*Full subtractor; GDI Technique; MTCMOS; XOR gate;

I. INTRODUCTION

With the development of technology, it becomes essential to have a chip which occupy minimum area, require minimum power and gives efficient output. In the field of electronic circuits, we have emphasized on VLSI technology in the last decade. In VLSI technology, we tried to improve the logic circuit design in terms of power consumption, power dissipation and leakage current[1-3]. Different techniques for improving logical circuits based on conventional CMOS have been proposed. These techniques are conventional CMOS technique, GDI technique, and MTCMOS technique. All techniques have their own advantages for different circuits[4, 5].With the increase of complexity on a chip increases the power consumption and chip area. High power consumption increases the temperature of the chip which further changes the characteristics of the chip[6, 7]. A full subtractor is one of the fundamental unit in digital circuits used for performing arithmetic operations. Full subtractor are used frequently in the digital electronics. A full subtractor designed with minimum number of transistors results an efficient circuit in terms of high speed, power consumption and area[8, 9]. Circuits of low power, high performance subtractor are of great interest due to VLSI applications.

In this paper, a full subtractor is designed using XOR gate and GDI technique. In section II we have discussed XOR gate based 1-bit full subtractor and GDI technique based 1-bit full subtractor. In section III we design full subtractor circuit using XOR gate and GDI technique. Section IV include the simulations and results and Section V concludes the results.

II. LITRERATURE REVIEW

A full subtractor is a combinational circuit that perform subtraction between two bits with the consideration of another bit known as borrow bit. So it has three input bits. At the output, it has two bits known as difference and borrow[10, 11]. In everyday life, we come across the different kinds of digital media like smartphone, computer, TV, gaming console etc. These devices are using processors in which we need to perform the arithmetic operations. Subtraction is one of the basic arithmetic operation. A subtractor may be used to do subtraction between one bit, two bits etc. A one bit full subtractor will have minimum of 3 inputs. A full subtractor can be designed with GDI technique, MTCMOS technique and conventional CMOS technique[9, 10].

A. XOR gate based technique

A full subtractor is a combinational circuit used to perform subtraction between three bits: minuend, subtrahend and borrow in. The output of full subtractor are Difference and Borrow. Here we have analyzed the full subtractor using XOR gate. NOT gate, AND gate and XOR gate also used. Fig 1 shows the gate level diagram of full subtractor. Here two half subtractor are combined to make a full subtractor.

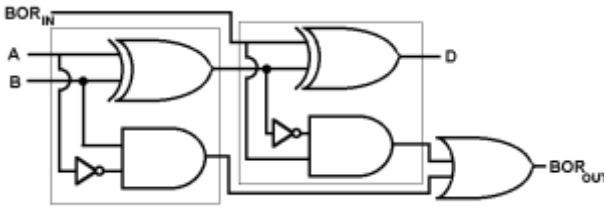


Fig 1. Gate level full subtractor

Truth table of 1-bit full subtractor is shown in below table.

Table 1. Truth table of 1-bit full subtractor

Input			Output	
A	**B**	**BORin**	**D**	**BORout**
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

B. GDI Technique

In GDI (Gate Diffusion Input) technique we use a basic cell as shown in Fig. 1below. In the below figure we can see that it looks similar to inverter. But there are certain difference between the inverter cell and GDI cell[12].

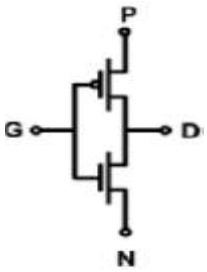


Fig. 2 GDI Basic Cell

A GDI cell consists of three inputs P, N and G. P is the input to outer diffusion node of PMOS transistor. This pin is not connected to Vdd. N is the input to outer diffusion node of NMOS transistor and it is not connected to GND and G is the common gate input to both NMOS and PMOS transistor[13]. Pin P and N deliver extra function which yields GDI technique.Different operation performed by GDI cell can be seen in the below table [3]. This table shows that only two transistors can perform six different operations.

Table 2. Various Logic function of GDI Cell

N	**P**	**G**	**Out**	**Operation**
0	B	A	A'B	F1
B	1	A	A'+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A'B+AC	MUX
C	1	A	A'	NOT

III. Subtractor Design

A full subtractor designed using GDI technique, MTCMOS technique and conventional CMOS technique is as follows:

A. XOR gate based full subtractor

A conventional CMOS subtractor is designed using XOR gate. Firstly 1 bit half subtractor using XOR gate is designed and simulated on the cad tool. After successful simulation, we designed the full subtractor circuit. The technology node that we use is 45nm. Then different analyses were performed to test the circuit. The schematic of full subtractor is shown below:

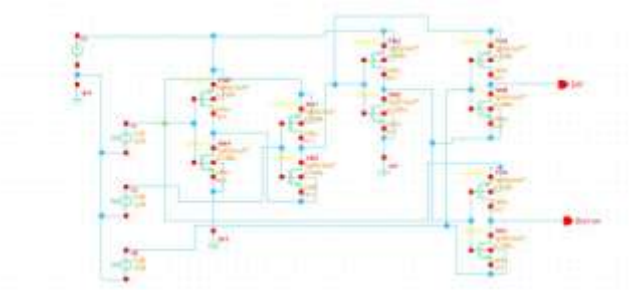


Fig 3. XOR gate based full subtractor

B. GDI Technique based full subtractor

GDI technique involves the use of a basic cell as shown in fig.2. A full subtractor circuit using GDI technique is as follows:

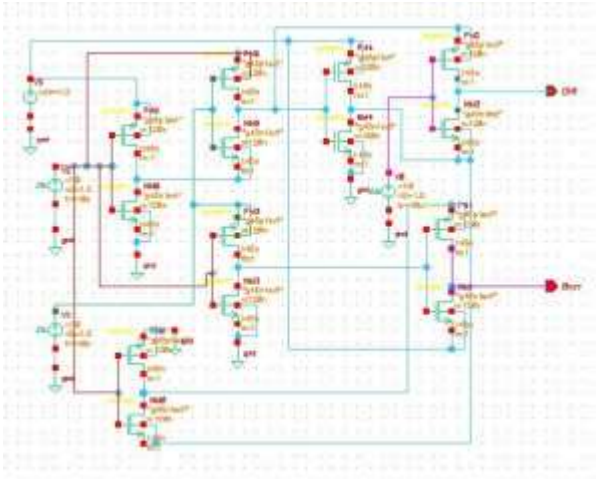


Fig 4. Full Subtractor using GDI technique

IV. Results and Discussions

1-bit full subtractor designed using XOR gate based and GDI based technique. The 45nm technology node used for designing both types of subtractor. In analysis we found that full subtractor designed using XOR gate uses less number of transistor, less power and less propagation delay. Below waveform figures and table shows the output and comparison between these two methods for designing full subtractor.

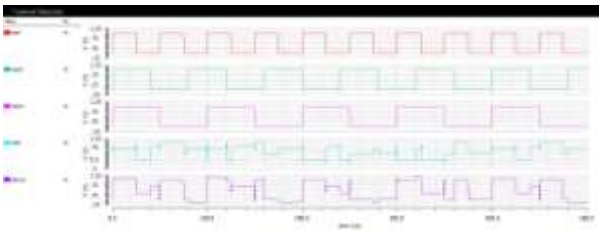


Fig 5. Simulations using XOR gate

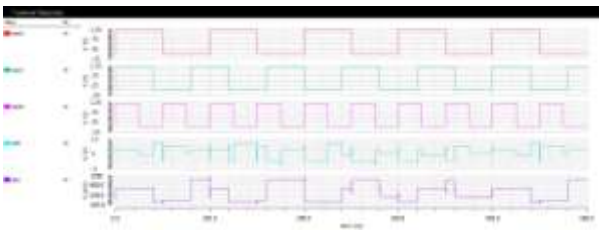
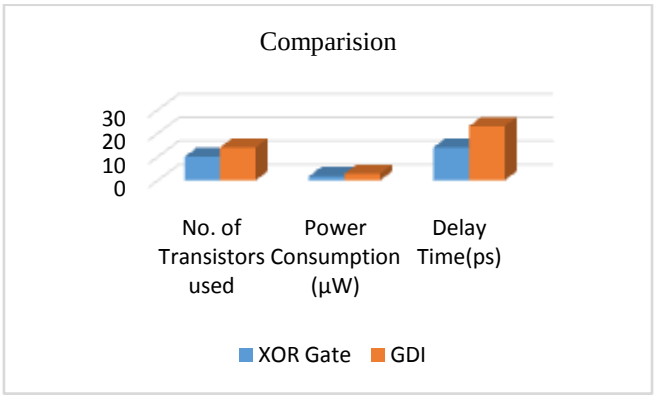


Fig 6 Simulations using GDI technique

Table 3. Comparison Analysis

Parameter	XOR gate based Subtractor	GDI Technique based Subtractor	Improved %age using XOR gate
No. of Transistors used	10	14	29.6%
Power Consumption	1.81µW	2.83µW	36.04%
Delay Time	0.014ns	0.023ns	39.13%



V. Conclusion

In analysis, it is concluded that a full subtractor can be designed using different techniques. In this paper,transient analysis for XOR gate based and GDI technique based full subtractor has been performed. It is found that XOR gate based full subtractor uses less number of transistors, less propagation delay and less power consumption when compared with GDI technique based full subtractor. XOR gate based full subtractor has power consumption of 1.81µW and delay time is 0.014ns whereas GDI technique based full subtractor have power consumption of 2.83µW and delay time is 0.023ns.

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