A Survey on Leakage Reduction on Logic Gate in Deep Submicron Technology

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Abstract**—** *The popularity and necessity of portable electronic systems by users have strongly influenced VLSI designers to make great effort for reduced silicon area, improved speeds, long duration battery life, and great reliability. The VLSI designers always try to save power consumption while designing a system. The performance of circuit is strongly influenced by the choice of logic style to design the digital circuit. Design optimization at circuit level is very important to avoid any degradation in output voltage level, to achieve less power consumption, to have less propagation delay in critical path and to be reliable at reduced supply voltage as we scale down towards deep sub micron technology. Switching activity of circuit affects the dynamic power consumption but with the technology scaling, the number of transistors is continuously reduced which increases the static leakage power at lower supply voltage. In a few technology generations, leakage power is supposed to become a main contributor of total power consumption. In this Paper we calculate impact of leakage power on conventional gate at 45nm and 32nm technology by using HSPICE simulator at supply voltage of 0.9V and 1V with 25^{0}C and 100^{0}C at 10MHz frequency.*

Keywords**—** *Leakage Power, Subthreshold Current, Gate oxide Current, Shorter channel Effect.*

I. Introduction

Today, electronic devices play a very important role in every one's day to day life. Devices such as mobile phone, ipad, laptop, pocket calculator become necessity to live a comfortable life. Consumer prefers portable and battery powered electronic devices. Earlier in 1990's, performance and speed was the important parameters to design any system but now with the growing trend towards portable computing and wireless communication, power dissipation has become one of the most critical factor in the continued development of microelectronics technology [1].
Minimizing power consumptions calls conscious effort at different levels of the overall design process as shown in Fig.1 [2]. In VLSI (Very Large Scale Integration) design, CMOS (Complementary Metal Oxide Semiconductor) processes are widely used and completely replaced nMOS process and bipolar transistor processes for designing all digital logic systems [3]. Circuit level choices have a good impact on power dissipation of CMOS circuits. Usually, a number of approaches and topologies are available for implementing various logic and arithmetic functions.

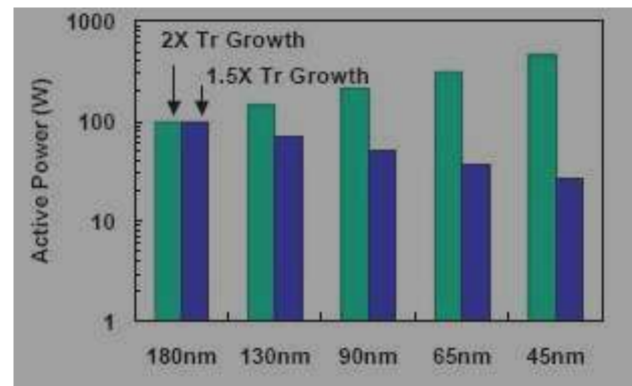


Fig.1: Growth in dynamic power of a microprocessor

Lower size transistor leaks more power through the source during idle state of the device which directly affects the battery life [3,4]. Now customer demands portable devices which give performance same as non-portable devices which not just occupy less area, should also have more battery life. In this way designer switch to low power CMOS VLSI design where the supply voltage of the IC is reduced which in turn reduces the switching power dissipation in micron devices which was the main cause of total power dissipation.

II. Literature Review

As discussed earlier, mainly two parameters which decide the performance of any CMOS chip are power consumption and propagation delay. These are discussed below.
There are mainly four sources of power dissipation in CMOS circuits [5].

1) P_D 2) P_{ST} 3) $P_{Short\text{-}circuit}$ 4) $P_{Static\text{-}DC}$

Total Power dissipation is calculated as:-

$$P_T = P_D + P_{ST} + P_{Short\text{-}circuit} + P_{Static\text{-}DC} \quad (1.1)$$

Where P_D is the dynamic or switching power dissipation, occurs due to charging or discharging the parasitic capacitances in node voltage transition. P_{ST} is the static or leakage power dissipation, combination of the subthreshold leakage power due to the not ideal off state MOSFET transistors and the gate leakage power caused by carrier tunneling over thin gate oxides. $P_{Short\text{-}circuit}$ is the short circuit power dissipation occurs during switching operation when both the Pull Up and Pull Down networks are in ON state, and current drawn from the power supply towards ground. $P_{Static\text{-}DC}$ is the static DC power dissipated when a CMOS IC is driven by a low voltage swing input signal.

There are various types of Leakage current present in CMOS devices as we scale down the channel length some of the Leakage current present in CMOS as shown in Fig.2.[6,7]

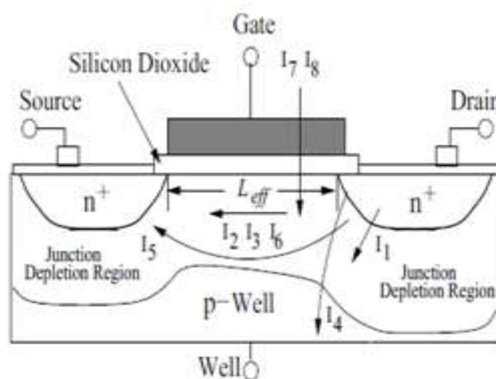


Fig.2. Leakage Mechanism in Short-Channel NMOS Transistor

I1= Reverse-bias p-n junction diode leakage current

I2 = Subthreshold leakage current

I3 = Gate Oxide tunneling current

I4 = Hot-carrier injection

I5 = Channel punch-through

I6 =Gate induced drain-leakage current

(a) Sub-threshols Leakage

Sub-threshold leakage current is very significant component of the leakage power and this current passes from drain to source through the channel [6-7]. The sub-threshold leakage current is caused basically due to carrier diffusion between the source and drain region of the transistor in weak inversion. For a particular MOS transistor whenever applied gate to source voltage is less than the threshold voltage of the transistor, there is no flow of current. Mathematically

When $V_{gs} < V_t$

$$I_{ds} = 0$$

The DIBL effect occurs at higher drain voltages where threshold voltage of transistor reduces. Depletion region of the p-n junction between the drain and body increases with the increase in drain voltages which increases more under the gate voltage. Responsibility to balance the electron charges in depletion region is more on drain voltage rather than gate voltage.

(b) Gate oxide tunnelling current

Tunnelling through gate oxide occurs because thickness of gate oxide layer is gradually reduced as technology is reducing[8,9]. The gate oxide tunnelling current is caused because of tunnelling of electrons through nMOS capacitor with a heavily doped n+ polysilicon gate and p type substrate. In MOS transistor, silicon oxide (SiO_2) layer at Gate terminal is a very good insulator, but the electrons can tunnel across very small thickness level of this insulation layer. The probability of this tunnelling drops off exponentially with oxide thickness. This Gate oxide tunnelling current I_{ox} [10] flows from the gate terminal through the oxide insulation to the p substrate.

III. LEAKAGE CURRENT IN BASIC NAND GATE

A graph is prepared by nodes and links, which represented by transistors and their interconnection respectively. Fig.3, shows the Graphical representation of 2 input NAND gate. Here a, b are the inputs and y is the output of the given circuit. V_{DD} and GND are the power supply and ground nodes. This logic gate is used as a basic gate for implementation of every other gate for simulation. It is used CMOS logic design style. Here two input NAND logic gate is used as a basic gate for each logic and combinational circuit. Firstly NAND gate and its variants are created using CMOS design style. Secondly all the test circuits are implemented by NAND gate and analyzed by using these variants. For Simulation HSPICE is taken as a simulator tool [11,12]. It requires a spice code (Transistor level net-list) of the desired circuit for their parameters calculation. All the circuits are mapped with 45nm and 32nm BPTM technology file. This file contains every physical design details of a CMOS transistor, where 45nm is the effective length of CMOS transistor. All kind of analysis with mapping of this file is shown through the flow of HSPICE design flow. Firstly the proposed NAND gate circuit operation is explained.

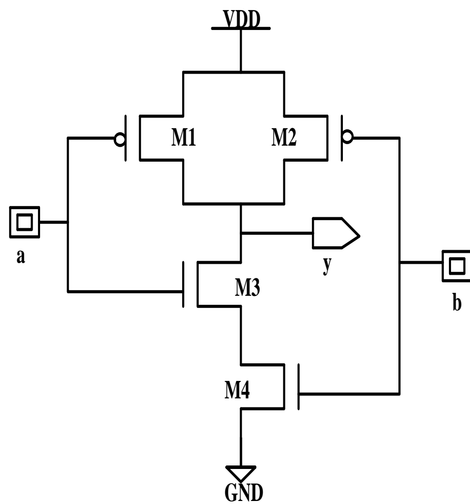


Fig.3. Graphical representation of 2input NAND gate

During operation of two input NAND gate (i.e. input vector '00'), then transistor M1 and M2 turn ON and transistor M3 and M4 turns of in which take part in leakage current. When input vector(i.e. is 01) the transistor M2 and M4 turn off and take part in leakage contribution, at input vector 10 M1 and M3 turns off and take part in leakage current contribution. When input vector is 11 maximum leakage current flows by the two M1 and M2 transistor. These parameters are Leakage Current (I_{Leak}), Static Power dissipation (P_{ST}) and Dynamic Power dissipation (P_D), Total Power (P_T), delay and PDP. Performance of CMOS circuits is depends on these parameters. For DSM circuits mainly I_{SUB} is the dominating component of power dissipation in CMOS IC [13,14].

IV. Results and Discussion

Leakage current for Proposed circuit is calculated by using Berkley Predictive Technology Module (BPTM) in HSPICE simulator using 45nm and 32nm process technology with supply voltage of 0.9V and 0.8V at 10MHz frequency and C_L=1pf. Leakage power of conventional gate is compared with Proposed technique implemented in with all the input vector combination at 25^0 C and 100^0 C temperature respectively. Transient analysis of proposed technique with Nand gate is shown in Fig.3. It is observe that output wave form provides proper logic.

Table I. Calculation of Average Power, Delay and PDP

Logic Gates	Average Power Consumption (µW)		Delay (pS)		PDP (aS)	
	45nm	32nm	45nm	32nm	45nm	32nm
NOT Gate	0.278	0.190	4.78	5.13	1.32	0.97
AND Gate	0.578	0.403	4.69	4.98	2.71	2.00
NOR Gate	0.324	0.233	5.95	6.42	1.92	1.49
NAND Gate	0.369	0.268	5.04	5.40	1.85	1.44
EXOR Gate	0.509	0.263	6.27	6.71	3.19	1.76

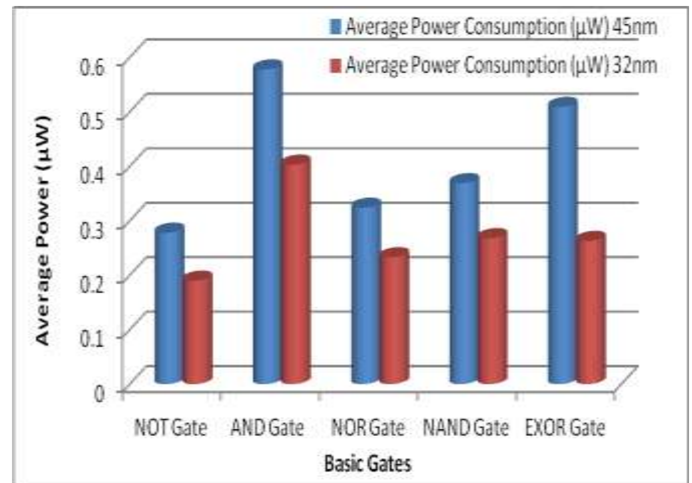


Fig.4. Average Power Consumption of Basic Gates at 45nm and 32nm.

Table.II. Leakage Power Consumption at 45nm at 25^0 C

Gates	Leakage Power Consumption at 45nm			
	00	01	10	11
NOT	21.83	75.23		
AND	60.45	109.1	76.07	172.8
NAND	31.46	149.8	103.6	150.4
NOR	43.63	83.11	72.86	111.8
EXOR	155.9	108.4	108.4	155.9

Table.III. Leakage Power Consumption at 45nm at 100^0 C

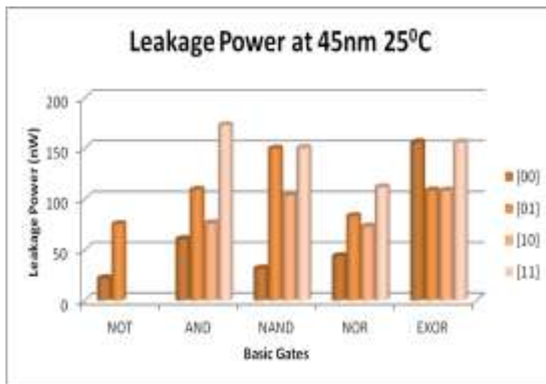
Gates	Leakage Power Consumption at 45nm			
	00	01	10	11
NOT	52.00	83.32		
AND	119.3	188.6	152.2	218.9
NAND	39.88	260.2	154.34	166.5
NOR	103.8	95.12	80.98	114.8
EXOR	176.0	166.5	166.5	176.0

Table. IV. Leakage Power Consumption at 32nm at 25^0 C

Gates	Leakage Power Consumption at 32nm			
	00	01	10	11
NOT	16.71	53.20		
AND	46.22	78.95	55.19	123.0
NAND	24.12	56.83	33.08	106.3
NOR	33.39	58.44	24.33	78.99
EXOR	109.4	78.30	78.30	109.4

Table. V. Leakage Power Consumption at 32nm at 100^0 C

Gates	Leakage Power Consumption (nW)			
	00	01	10	11
NOT	39.84	60.26		
AND	90.71	139.8	113.5	160.6
NAND	29.60	78.45	52.16	120.4
NOR	79.48	69.35	42.66	80.44
EXOR	127.0	121.8	121.8	127.0



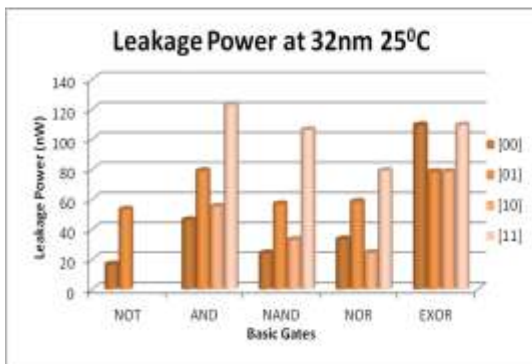


Fig. 5 Results comparison of Basic Gates at 45nm and 32nm.

One Bit FULL ADDER Circuit (1 Bit FA)

One Bit ADDER circuit implemented by two cascaded Ex-OR circuit and one NAND gate which outputs gives SUM and Carry signal respectively. The circuit of 1Bit FA is shown in Fig.6.

(i) Circuit Diagram

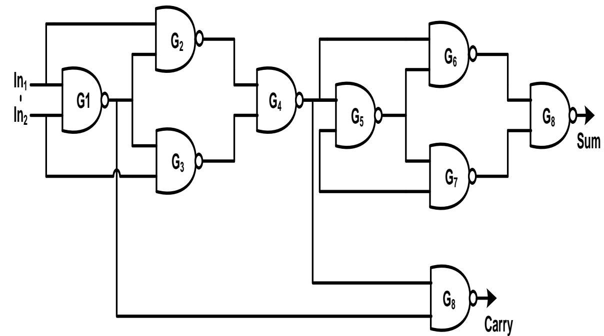


Fig.6. One Bit FULL ADDER (1 Bit FA) Circuit

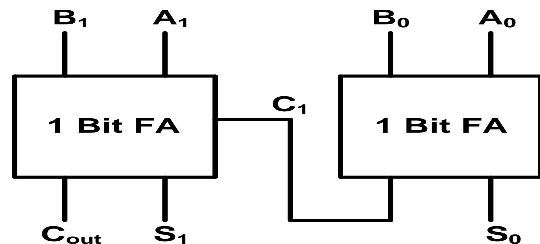


Fig .7. Two Bit FULL ADDER (2 Bit FA) Circuit

Simulation result of n1 and2 Bit FA circuit is shown in Table VI, The parameters such as P_D, P_{ST}, P_T, I_{Leak}, Delay and PDP (i.e. PDP_D, PDP_{ST}) are calculated and tabulated.

Table VI. Simulation Full Adder

Adder Circuit	Power Dissipation			I_{Leak} (nA)	PDP X(E-18)J	
	P_D (uW)	P_{ST} (nW)	P_T (uW) $=P_D+P_{ST}$		PDP_D	PDP_{ST}
1Bit Full Adder	1.66	127.00	1.79	115.4	39.84	3.048
2Bit Full Adder	3.12	239.80	3.36	218	74.88	5.7552

V. Conclusion

In nanometer scale CMOS technology, sub-threshold leakage power is compatible to dynamic power consumption, and thus handling leakage power is a great challenge. In this paper, we present a new circuit structure named "stacking with sleepy keeper Approach" to tackle the leakage problem. . It proposes a technique for reducing the leakage current during idle mode of circuit. The proposed technique can be applied on high performance, low power application, where leakage is major concern such as microprocessor, memory units and other portable devices. In future new approach of leakage reduction technique at gate level and block level are expected to give more power saving than the existing approach at CMOS circuit level design.

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