Dynamic circuits for CMOS and BICMOS low power VLSI Design

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***Abstract*—** *Today, in dynamic circuit's logic gates are used in CMOS and BICMOS technologies by using diodes, resistance and capacitors to decrease the swing in the voltage at output end. This technique improves both power dissipation and delay by using V_{dd} supply that is 1.8V.Here we discuss new BICMOS proposes and compare it wiith CMOS design. BICMOS logic has advantages such as large load drive capabilities, low static power dissipation, fast switching and high input impedance. In this paper, architecture is designed for CMOS and BICMOS logic using Cad tool and compared the results. BICMOS has better performance in terms of delay and power consumption, in compared to CMOS.*

Keywords—*CMOS,BICMOS,Low power*

I. INTRODUCTION

In latest trend of VLSI circuit design is High speed and Low power. The power saving issue is for battery applications and for thermal management for high performance systems. One method to overcome from this problem is to scale down device dimensions and another one is reduce the supply voltage, by decreasing power dissipation and maintaining the switching speeds. System and circuit designers can use many optimization methods to minimize the delays and low power consumption but the result is not up to the mark. This is valid for both CMOS and BICMOS circuits. In this paper we discuss a new approach to reduce the both power and delay in the circuit using CAD tools.

The reduction in the voltage reduces the power dissipation. The new dynamic CMOS and BICMOS are presented in this paper. Simulation results and comparisons designs are presented in this paper. All the simulation's in this paper are performed in CAD tools and compared with HSPICE models.

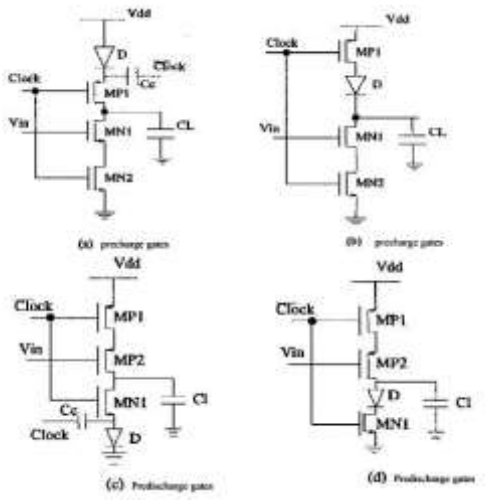
II. DYNAMIC CMOS GATE

The average Power consuption in CMOS is the average of Dynamic Power Consuption and short circuit power consuption and leakage power consuption. Static CMOS gates are used to implement the logic blocks and the transmission gates are used to transfer the output from one level to another level. Each transmission gate is controlled by clocked and the clock signal and its compliment.

The operation of CMOS dynamic logic depends upon charge storage in the parasitic input capacitances during the inactive clock cycles. In dynamic CMOS transmission gate shift register consist of CMOS inverter that is driven by a CMOS transmission gate. During the active clock phase the input voltage (V_{in}) is transferred into other input capacitance (C_x) by using transmission gate. When the resistance is low of the CMOS transmission gate results in a smaller transfer time as compared to NMOS switches. And there is no threshold voltage drop across the CMOS transmission gate. When the clock signal becomes inactive, the CMOS transmission gate turns off and the voltage level across capacitance (C_x) can be preserved until the next cycle.

In dynamic CMOS circuit we reduce the number of transistors used to implement any logic function. In circuit operation is based on the discharging of the output node capacitance and note down the output value according the input's applied. Both of the operations are scheduled by a single clock signal that drives both NMOS and PMOS transistor.

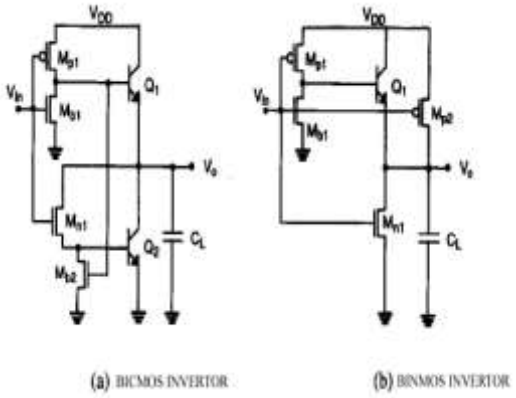
In dynamic CMOS when the clock signal is low (Precharge state), the PMOS transistor (M_p) is in conducting state. And the NMOS transistor (M_n) is off.



Dynamic CMOS in charge and Precharge states

III. DYNAMIC BICMOS GATE

When the power supply voltage is scaled down in BICMOS circuits for low power applications, the speed is reduced in many ways because the logic voltage swing is not point to point. The main feature of BICMOS circuit is to use NPN transistor from analog library in the Precharge circuit to make the output at full swing. The NPN transistor is used in Precharge state to improve the switching speed. One another way is used for this that is to cut the DC current that makes the circuit simpler. And either we use diode to limit the Precharge voltage in CMOS to increase the speed as well as power.



In this fig. BICMOS invertor and BINMOS invertor are shown.

BICMOS inverter consists of 1 PMOS and 1 NMOS and two NPN transistors. When the inputs (V_{in}) is high (V_{dd}), the NMOS transistor turns on 1 NPN conducts and other is off and PMOS is also in off condition. As a result, the ground voltage is translated to the output voltage (V_{out}). On the other hand when the input is low, one NPN transistor is on condition and PMOS is also ON, and NMOS and 1 NPN transistor is in off state, resulting to a high output level at the output side.

ADVANTAGES OF BICMOS OVER CMOS:

Low Power Consumption: In BICMOS gates perform same as the CMOS inverter when it comes to power consumption, because both gates display almost no static power consumption. The major dissipation is done by the discharging of the capacitors. When comparing BICMOS and CMOS in driving small capacitive loads, their performance are comparable, however, making BICMOS consume more power than CMOS. On the other hand, driving larger capacitive loads makes BICMOS in the advantage of consuming less power than CMOS, because the construction of CMOS inverter chains are needed to drive large capacitance loads, which is not needed in BICMOS.

High resistance to process deviations and temperature changes: The resistance to process deviations and temperature changes of the BICMOS is the reason behind the success of the development of a BiCMOS 1-Mbit DRAM. They were able to derive a set of equations that determine the DRAM's sensitivity to changes in temperature and process deviations for a 1.3 micron technology.

Need of BICMOS Technology: A BICMOS circuit consist of both BJT and MOSFET's on a single chip. The reason behind the hybridization is to combine the high speed switching and high output driving features of the BJT and the low power and the high density features of the CMOS circuit.

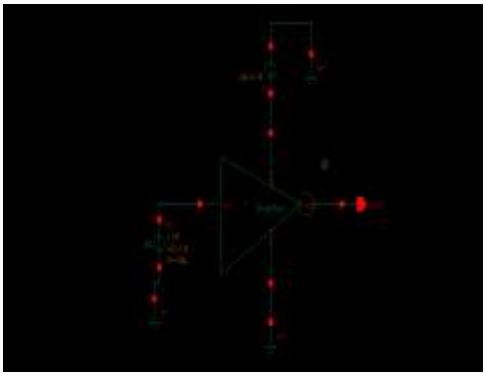
DISADVANTAGES OF BICMOS OVER CMOS:

Speed degradation in the low supply voltage region: BICMOS circuit is its speed degradation in the low supply voltage region. Since the supply voltage for CMOS technology gradually decreased from 5V to less than 2V in the past years, an optimization technique must be introduced.

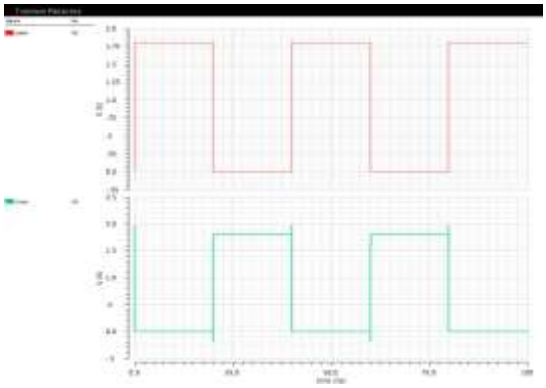
BiCMOS having greater manufacturing complexity than CMOS: The addition of NPN transistors into the CMOS process exhibits greater amounts of manufacturing complexity. This is due to the technology's viewpoint of having a better performance requirement, thus the implementation of bipolar transistors for high switching
Speed capabilities. Due to the greater complexity in developing BiCMOS circuits, strict care should be taken. Greater complexity also increases testing, verification, and database management. However, several approaches are being taken to resolve the speed degradation of a conventional BICMOS circuit without the introduction of process complexity.

IV. SIMULATION AND PERFORMANCE COMPARIOSON

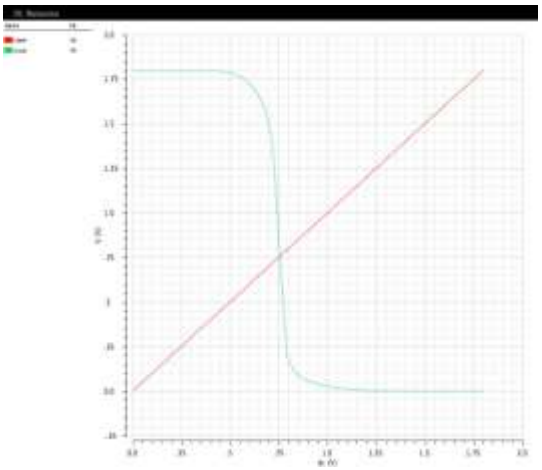
FOR CMOS INVERTER



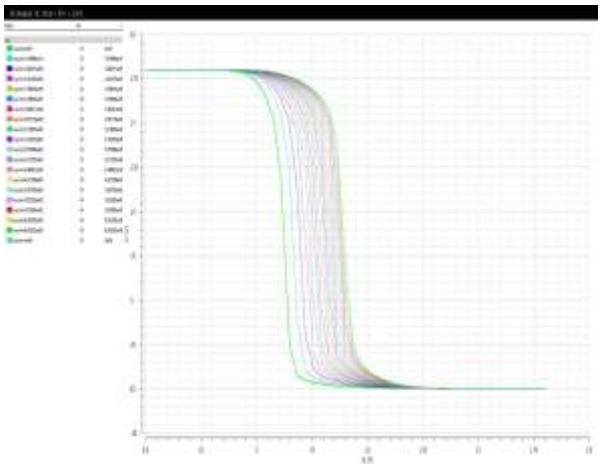
Symbol diagram of conventional CMOS inverter



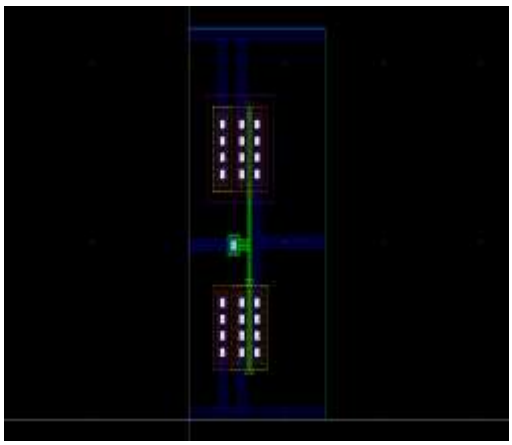
Transient Response of Dynamic CMOS Invertor



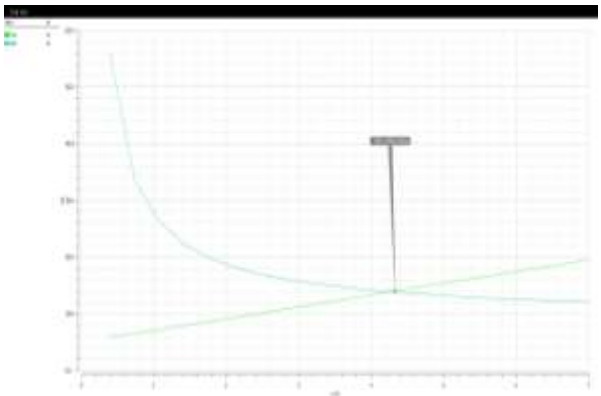
VTC characteristics of Dynamic CMOS inverter



DC analysis of Dynamic CMOS Invertor at V_1 = 0v and V_2 = 1.8 v



Layout of Dynamic CMOS Inverter



Delay in Dynamic CMOS invertor (Rise time and fall time)

Propagation Delay	Result (in sec)
High to Low(T_{PHL})	10.48 p
Low to High(T_{PLH})	22.02 p

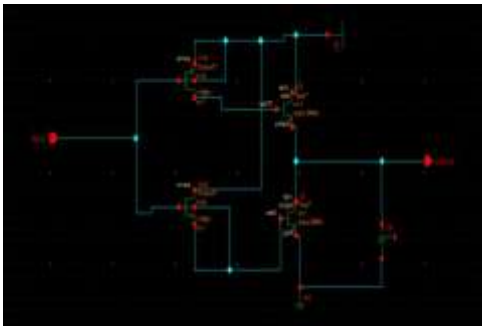
The total propagion delay is the average of T_{PHL} and T_{PLH} that is : 16.25 ps.

Parameters	Result
Power consumption	**27** nW
Area Utilization	**77** µm

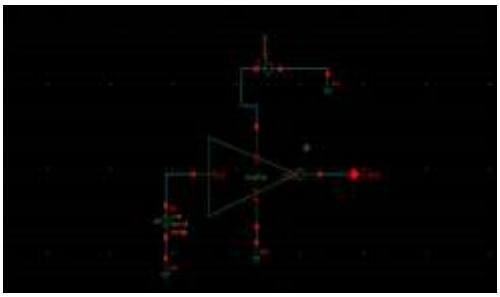
The dimensions used by PMOS and NMOS transistors in layout are:

Dimensions	Result
Width	2 µm
Channel Length	180 nm

FOR BICMOS INVERTER



Schematic diagram of conventional BiCMOS inverter:



Symbol diagram of conventional BiCMOS inverter:

BICMOS technology has a lot of features:

a) Good current drive capability because of low collector series resistance.

b) Good performance in analog and mixed application because of high precision analog components like resistirs and capactiors and very high dynamic range. Operating voltage is less than 5V.

c) Good performance in power switching: In smart applications low series resistance and low sensitivity and high junction breakdown voltage, very good performance in high currents.

On the other hand BICMOS technology has some dis-advantages compared to CMOS technology:

a) Speed degradation in low supply voltage
b) BICMOS having greater manufacturing complexity than CMOS.

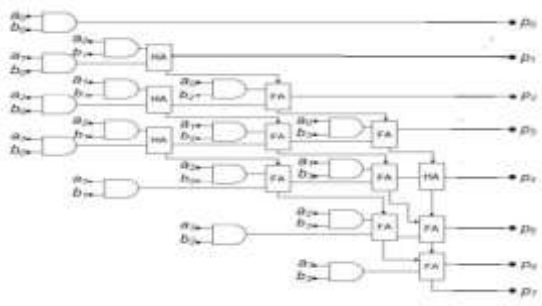


Fig.: 4*4 Array Multiplier

Delay comparison in Array Multiplier between CMOS and BICMOS:

Array Multiplier	Delay CMOS(in ns)	Delay BICMOS(in ns)
2*2	16.17	20.47
4*4	7.43	6.12

Conclusion and Future work: It is observed that BICMOS logic has better characteristics as compared to CMOS. Where ever we need much higher speed we can use BICMOS.
BICMOS technology has low power, low voltage and very high speed integrated circuit for both mixed and digital signal application. The improvement in delay of CMOS and BICMOS with V_{dd} =1.5V. more work should be needed on the layout design of BICMOS by using CAD tools to simplify their design.

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