Two Stage Operational Amplifier with a Gain Boosted, Source Follower Buffer

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Abstract- *This paper presents design and implementation of a two stage operational amplifier with gain boosted, source follower buffer. The circuit operates efficiently in a closed loop feedback system to solve many impedance issues and makes it suitable for high speed applications. Any fluctuations in supply voltage or dc input voltages can be nullified and stabilizes the operation of the circuit producing large output gain. This architecture also neutralize the effects such as ringing and overshooting in frequency response. 0.6um technology using cadence is used to implement the amplifier. The Op-amp designed here exhibits a noticeable10^4.35 DC differential gain.*

Keywords: *Operational Amplifier, Gain Band Width, Slew Rate, Common Mode Rejection Ratio.*

1. INTRODUCTION

Op-amps are very flexible and essential part in most of the integrated circuit applications. As CMOS technology scaled down to nanometers, analog circuits are increasing more significantly. So, when the transistors are manufactured there are many trade-offs occurring between higher packing density, speed and power dissipation. When compared to digital systems, analog circuits have some different trade-offs such as voltage scaling in low power circuit design. In analog integrated circuits, reducing the supply voltages does not lead to reducing the power consumption. It is basically measured by the required SNR ratio and frequency of operation.

Op-amps with medium level of DC gains, responsible bandwidth, and high dynamic range are implemented with two stages or three stage structures.Consider the following circuit shown in the figure. 1.

Differential amplifier have substantial advantage ofnoise immunityover single ended amplifier. Common Source able to provide large gain in output stage and additionally provides high output swing.

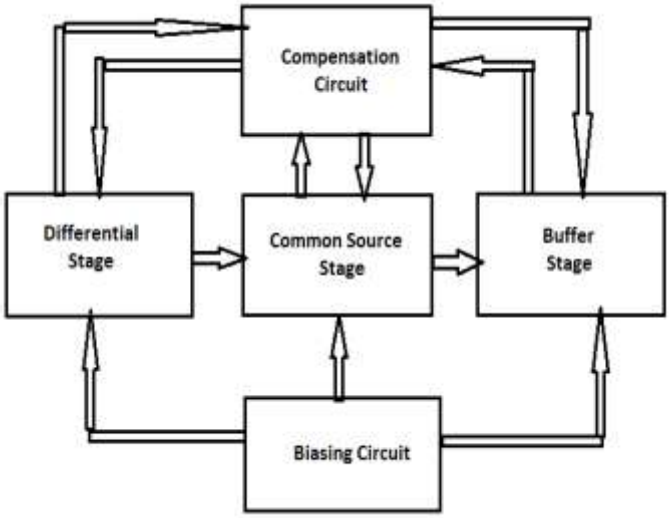

Fig. 1 shows block diagram of operational amplifier.

Differential Amplifier: Is an amplifierthat minimizes the common mode voltage/noise and supply voltage noise and provides amplification of two input difference.

Common Source: CS stage is second stage in the schematic. It is used to produce a tremendous amount of gain amplifying output from differential amplifier.

Buffer Stage: This stage is used if the Op-Amp is driving low resistance

Source follower Buffer is used for isolation. . Generally, at the Common Source Stage the output resistance is high. To reduce the output resistance and to increase the output swing than the Common Source, Source Follower is used besides it maintains the stability.

The other circuits are compensation and bias circuits which are necessary to keep Op-Amp stable when negative feedback is applied and to reduce the number of poles.Consider the following circuit shown in the figure. 2.

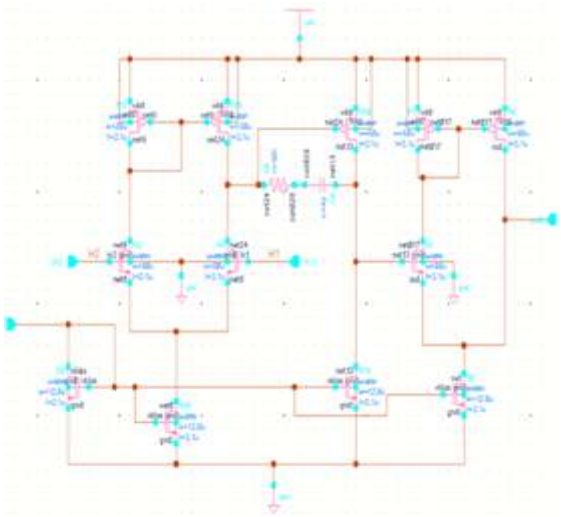

Fig 2: Schematic of two stage op-amp with gain boosted source follower buffer

Calculations for Specifications:

1. Miller Capacitance:
   CC=0.22 *CL
2. I5 Tail Current:
   SR= $I5/CC$
3. gm1,m2:
   $gm1,m2=GBW\ .CC.2\pi$
4. Design of M1 and M2:
   $(WL)m1,m2=gm1,m2/\mu n.Cox.2.ID$
   $= gm1,m2/\mu n.Cox.I5$
5. Design of M3 and M4:
   $(W/L)m3=2ID3/[\mu p.Cox.[VDD-ICMR(+)$
   $-|Vt3|max+Vt1min]$^2]
6. Design of M5:
   $(W/L)m5=\ 2ID5/\mu n.Cox.(VDSSat5)2$
7. Design of M6:
   $(W/L)6.I6=(gm6/gm4)2.(W/L)4.I4$
8. Design of M7:
   $(W/L)7/(W/L)5=I7/I5$

TABLE.I

Transistor sizes	values
$(W/L)_1=(W/L)_2$	90u/2.1u
$(W/L)_3=(W/L)_4$	30u/2.1u
$(W/L)_6=(W/L)_9$	60u/2.1u
$(W/L)_8=(W/L)_{10}$	90u/2.1u
$(W/L)_5=(W/L)_7=(W/L)_{11}$	12u/2.1u

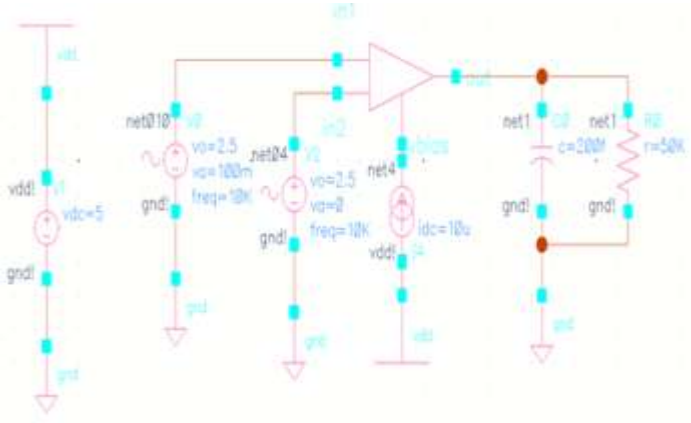

Fig 3: Symbol of two stage op-amp with gain boosted source follower buffer.

II.SIMULATION AND DISCUSSION

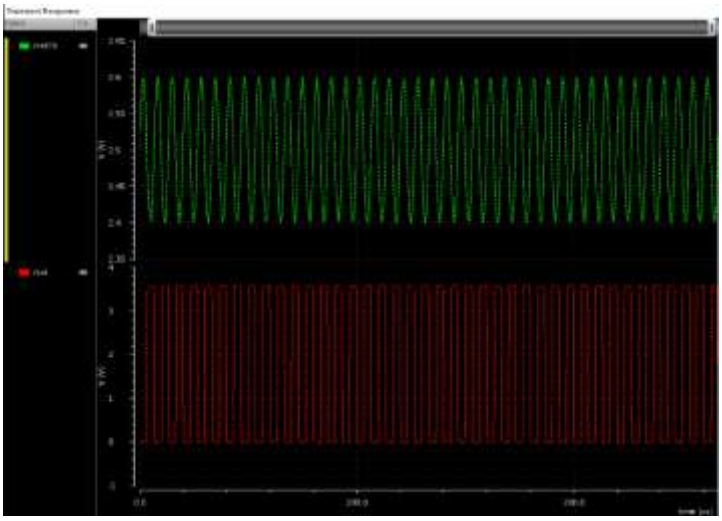

Fig 4: Transient response with voltage swing 3.6V

Performance Parameters:

Slew Rate: Change in voltage per unit time.

SR = dV/dt

Common Mode Rejection Ratio:Ratio of differential voltage gain to the common mode gain.

CMRR = Ad/Acm

Gain Bandwidth Product: The product of the open-loop voltage amplification and the frequency at which it is measured.

GBW = A1*(f) 1

Unity Gain Bandwidth:The range of frequencies within which the open-loop voltage amplification is greater that unity.

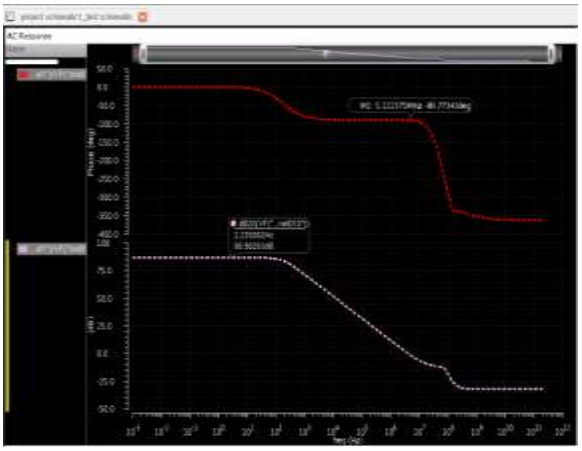

Fig 5: AC analysis of the schematic

From the plot we get the Unity gain band width of 5 MHz.

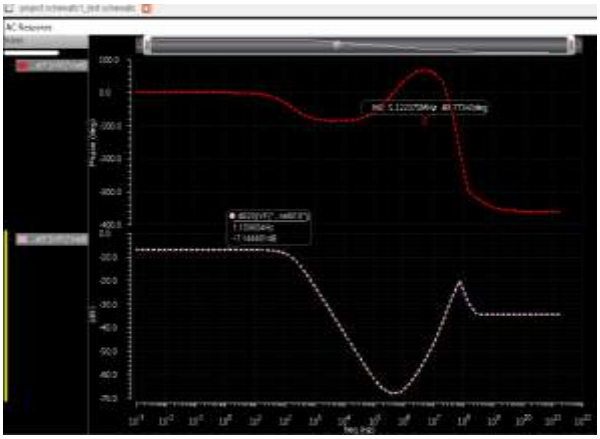

Fig 6: Common mode Gain result: 7.1dB

From the both results above
Adm = 86.98dB (104.35) and Acm = -7.1dB (10-0.35)
CMRR = Adm / Acm = 105 (99dB)

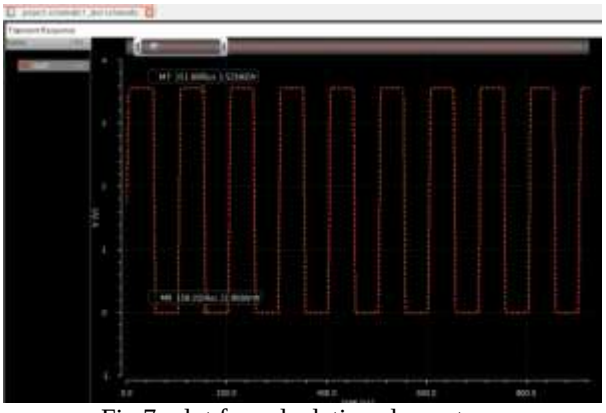

Fig 7: plot for calculating slew rate.

From the plot we have V1 = 3.525V, V2 = 22.856 mV,
T1 = 153.69us, T2 = 158.202us

We got the slew rate of 0.78V/us.

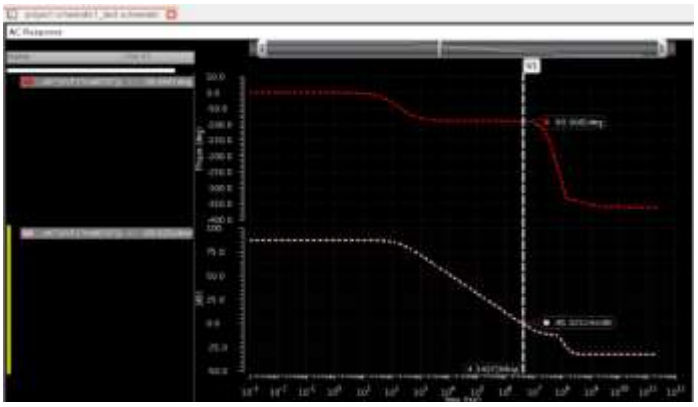

Fig 8: Plot for phase margin

From the plot the calculated phase margin is 90 degrees.

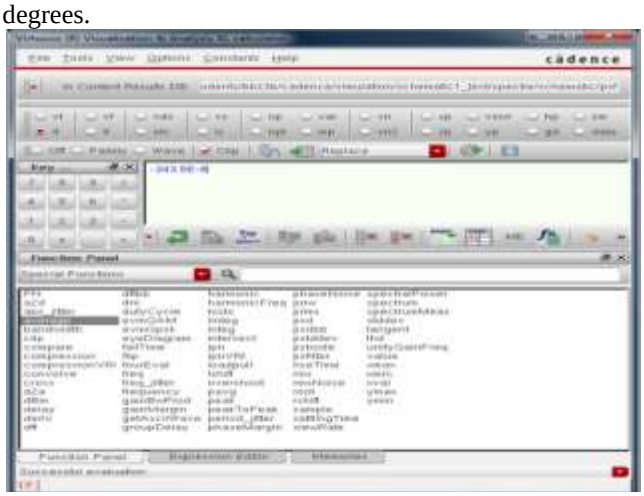

Fig 9: power consumption calculator

Calculating the power consumption from the cadence we get 343.5 uW.

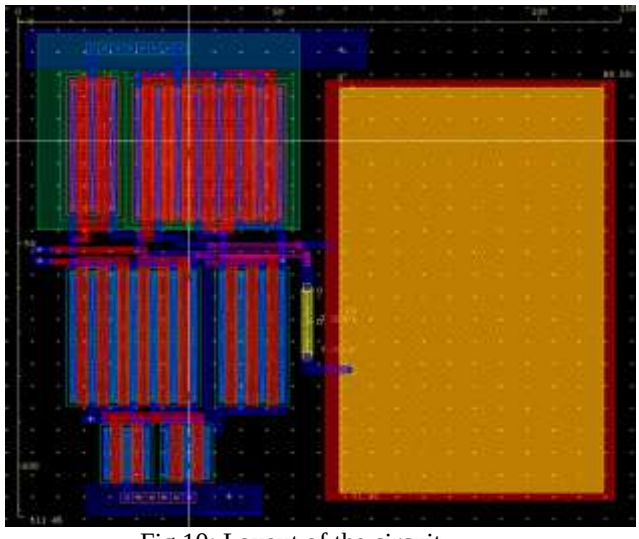

Fig 10: Layout of the circuit.

From the layout it is clear that it is in 111um*115um area.

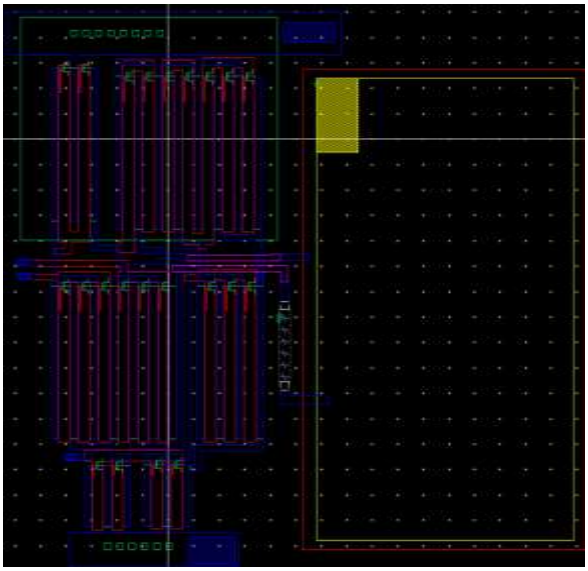

Fig 11: Extracted view from the layout

III. DESIGN SPECIFICATIONS

Process: 0.6um CMOS
Process Supply Voltage: 5V
Supply or less Supply Current: ≤ 300 uA
Quiescent Load: RL ≥ 50 K, CL ≤ 50 pF
Output Voltage Swing: ≥ +/- 2.5 V
Stages: Differential stage, High gain stage, Output buffer
Compensation: Internal Capacitance Unity Gain-Bandwidth
Frequency: ≥ 0.5 MHz
Phase Margin: ≥ 90 degrees
Differential Gain: ≥ 10^4 (preferably ≅10^5)
Common Mode Range: ≥ +/- 2.5 V
Slew Rate: ≥ 0.5 V/us overall with load capacitance
Layout: Inputs on the left, Output on the right and Rails at the top and bottom
Area: ≤ (500 um x 500 um)

IV. RESULTS

Parameters	Values Obtained
Supply Voltage	5V
Supply Current	10uA
Quiescent Load	R_L=50K,C_L=200fF
Output Voltage Swing	3.6V
Stages	3 Stages Compensation:4pF capacitance using miller compensation
Unity Gain-Bandwidth Frequency	5MHz
Phase Margin	90.23 degrees
Differential Gain	10^4.35
Slew Rate	0.78 V/us
Overall with Load Capacitance Area	111 um*115um
CMRR	90dB
Power Consumption	343.5uW

V. CONCLUSION

The design and performance of Two Stage Op-amp with a gain boosted, source follower buffer is described here. Op-amp designed here exhibits 10^4.35 DC differential gain. 5 MHz unity gain bandwidth, phase margin of 90 degrees.And0.78 V/us overall with load capacitance as slew rate. The power consumption for 5V supply voltage is 343.5uW. Excellent output differential swing of 3.6V with differential input swing 0.2V and good linear range of operation are some of the additional features of design. This type of Op Amps are mainly useful where the circuits should maintain high efficiency and distortion less signals in Digital to Analog Integrated Circuits.

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REFERENCES

[1] Rajkumar S. Parihar Anu "Design of a Fully Differential Two-Stage CMOS OpAmp for High Gain, High Bandwidth Applications".
[2] Design Procedure for Two-Stage CMOS Op-Amp withFlexible Noise-Power Balancing Scheme Jirayuth Mahattanakul, *Member, IEEE,* and Jamorn Chutichatuporn
[3] Design of Analog CMOS Integrated Circuits, Behzad Razavi
[4] Design of an Amplifier through Second Generation Current Conveyor, Nikhita Tripathi, Nikhil Saxena, Sonal Soni
[5] K. N. Leung and P. Mok, "Analysis of Multistage Amplifier-Frequency Compensation," IEEE Transactions on Circuits and Systems, vol. 48, no. 9.
[6] Analysis of two-stage CMOS Op-Amp forSingle-TransientsHenil Langalia, Sarthak Lad, Mangesh Lolge and Surendra Rathod
[7] Two-Stage High Gain Low Power OpAmp withCurrent Buffer CompensationSachin K Rajput, B K Hemant
[8] Design Procedure for Two-Stage CMOS Operational AmplifiersEmploying Current BufferJ. Mahattanakul
[9] A Two Stage and Three Stage CMOS OPAMP with Fast Settling, High DC Gain and Low Power Designed in 180nm Technology Anshu Gupta D.K. Mishra, R. Khatri U.B.S. Chandrawat Preet Jain