Area & Speed Efficient CIC Interpolator for Wireless Communination Application

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Abstract- *The aim of this paper to design and present a CIC Interpolator for SDR based wireless communication system. SDR system can provide a feasible solution which will be able to perform different function at different time on same hardware. Other requirements are high speed, improved area and low power consumption. The designing & implementation of Cascaded Integrator Comb Interpolator Filter with embedded look up tables increase speed as well as decrease the resources on FPGA's target devices. The purposed CIC filter executes SRC efficiently using only adders & subtracts building it smart for SDR system. It will greatly enhance system performance and also cost which can be accomplished by reducing the immediate storage element and increase the reliability of the system. The CIC interpolator has been designed with MATLAB2013a, simulated with ISE Simulator, synthesis is done with XST, and implement on Spartan-3E XC3s500e-4fg320 target device. The planned design can be operated at an estimated frequency of 276.060 MHz by using very less resources available on FPGAs to offer useful solution for communication systems.*

Keywords — *CIC Filter, NGN, LUTs, 5G, SRC, SDR, FPGA*

I. INTRODUCTION

Digital Signal processors are specialized device designed to implement DSP algorithms on the digitized signal. Also DSPs are widely used in wireless communication systems for performing different type of filtering; encoding, decoding and many transform function. In the field of wireless communication, which are crowd deployed such as Third Generation networks like UMTS and Wi-Fi, Wi-Max and other sensor networks like CDMA, WCDMA, GPRS, WLAN and Bluetooth. For these techniques, many efforts have done for separation of transport and service layer in the concept of NGN. Wireless network of mobile for new generation is required to fit with-in the NGN, because all things are depend on wireless application potential. Software Defined Radios is an emerging technology and profoundly changing the radio system engineering and also providing software control of a verity of modulation technique, a collection of software and hardware, technologies that enable reconfigurable system architecture for wireless network, communication security function. Also, with a large frequency range, SDR support for waveform for present and coming standard. This can also be defined in software and equivalent piece of hardware can also be use to realize special application with little modification in software. To implement the SDR, the FPGA provide the best reconfigurable solution for high speed processing modules.

In rapid development of new technologies in the field of communication (digital), FPGA has been widely applied in the field of DSP. The DSP has many benefits like reprogram ability low cost, high logic density, flexibility and high reliability. The reconfigurable and programmable features of SDR make it very attractive and it able to realize complex architecture and evolving standards. The cost factor can be enhanced by using lower and less costly FPGA resources for the system design and by the well-organized utilization of FPGA resources [1].

CIC filter are good preference for implementing interpolation or decimation because they don't use multipliers and their frequency response can decrease aliasing and imaging issues. Cascaded Integrator Comb motivated by various emerging applications, such as, high data rate filtering increase the use of polyphase filtering techniques, advances in delta-sigma converter implementations and the significant growth in wireless communication and Software Defined Radio[2].

The major difference from a user point of view between current generation and expected 5G technique must be something else than increased maximum throughput; other requirements include low battery consumption. SDR allow rapid iteration on design because it closely mirrors the functionality found in real wireless devices with the added flexibility of broader frequency coverage and reprogrammable baseband processing. Digital-up converter & Digital-down converter are very important component of wireless communication system and used to filter, up/down sample & modulate the signals from baseband to the carrier frequency. Both DUC & DDC are mostly implemented on FPGAs or on ASICs [3].

II. CIC INTERPOLATOR

CIC filters have multiplier-less structure, adders and delay elements which give great benefits when aiming at less power consumption. It is a recursive filter because its comb section has feedback. The comb stage subtracts a delayed input sample. Hongenauer introduced the CIC that presents a useful proposal for execution of such interpolation & decimations. For transmission, CIC interpolator filter must be used because it provides excellent results with low computational load. Interpolation filter implementation is commonly composed of a zero insertion phase and a low pass filter phase [4]. Basic building blocks are integrator & comb. Integrator is a single pole Infinite Impulse Response filter with a unity feedback coefficient:

$$y[ṅ] = y[ṅ - 1] + x[ṅ] \quad (1)$$

This system is also known as an accumulator. The transfer function for an integrator on the z-plane is:

$$H1(Z) = \frac{1}{1-Z^{-1}} \quad (2)$$

Integrator's power response is a LPF with -20dB/decade roll off, & need infinite gain at DC. This is due to the single pole at Z= 1; the output can rise with no bound for a bounded input. Single integrator by itself is incapable and shown in fig. 1.

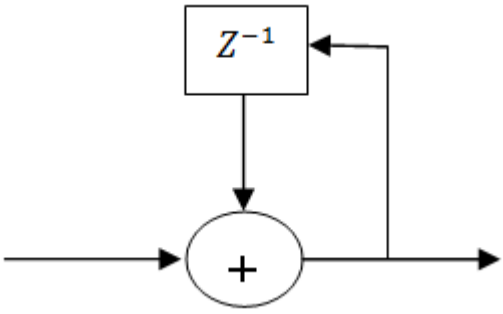

Figure 1 Integrator Structure

A comb filter running at the high sampling rate, f s, for a rate change of R is an odd symmetric Finite Impulse Response described by

$$y[ṅ] = x[ṅ] - x[ṅ - RM] \quad (3)$$

Where M is a design parameter and is called the differential delay. M can be any positive integer, but is usually limited to 1 or 2. The corresponding transfer function at f s is

$$H_c(Z) = 1 - Z^{-RM} \quad (4)$$

When interpolator factor (R) = 1 and differential delay (M) =1, the power response is a HPF function with 20dB/decade gain. When R M ≠ 1, raised cosine comes as a power response with RM cycles from 0 to 2π. The Comb structure is shown in fig. 2.

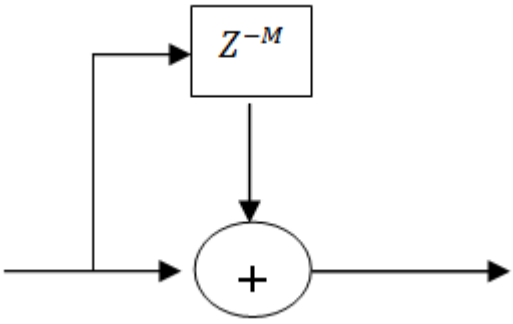

Figure 2 Comb Structure

The building of Cascaded Integrator Comb Filter, the N integrator section with N Comb section is required with a chain of input & outputs. This filter would be excellent, but can be simplified with combining it with the speed (rate) changer. Multi-rate analysis of LTI system can be done by this technique can "push" the comb section through the speed (rate) changer, & at slower sampling rate f s / R.

$$y[ṅ] = x[ṅ] - x[ṅ - M] \quad (5)$$

A Cascaded Integrator Comb interpolator filter would have number of section (N) cascaded comb stage running at f s/R, followed by a zero-stuffer, followed by N cascaded integrator stages running at f s. Cascaded Integrator Comb filter's transfer function at f s is

$$H(Z) = H_1^N(Z)H_C^N(Z) \quad (6)$$

$$H(Z) = \frac{(1-Z^{-RM})^N}{1-Z^{-1^N}} = \left(\sum_{k=0}^{RM-1} Z^{-k}\right)^N \quad (7)$$

Above equation shows that even through a Cascaded Integrator Comb has integrator, which by them has an IIR, a Cascaded Integrator Comb filter is equivalent to N Finite Impulse Response filters, each having a rectangular impulse response. All of the coefficients of these Finite Impulse Response filters are unity & symmetric, Cascaded Integrator Comb filter maintain the linear phase response & constant group delay. Filter's output shows the magnitude response as:

$$|H(f)| = \left|\frac{Sin\,\pi MF}{Sin\frac{\pi f}{R}}\right|^N \quad (8)$$

By this relations sin x ≈ x for small x and some algebra, approximation is done as for large interpolation factor (R):

$$|H(f)| = \left|RM\frac{Sin\,\pi MF}{Sin\frac{\pi f}{R}}\right|^N \; for\; 0 \le f \le \frac{1}{M} \quad (9)$$

Noticeable thing is that the output spectrum has nulls at multiples of f = 1 / M. in addition, the region around the null is where aliasing/imaging occurs. If f

c is defined to be the cutoff of the usable pass-band, aliasing / imaging regions are at:

$$(I - f_c) \le f \le (I + f_c) \quad (10)$$

For $f \le \frac{1}{2}$ and $i = 1, 2, 3 \ldots\ldots\ldots \left[\frac{R}{2}\right]$. If $f_c \le \frac{M}{2}$,

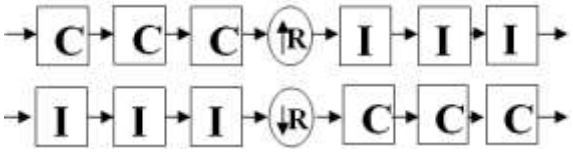

Figure 3 Three stage decimator and interpolator filters

Another noticeable thing is that pass-band attenuation is a function of the number of stages (N). As a result, while growing the number of stages (N) advance the aliasing / imaging rejection, it also growing the pass-band "droop". Also the DC gain of filter is a function of the speed (rate) changer. Cascaded Integrator Comb filter also has a constant group delay & linear phase response [5].

III. MATLAB Based Design of CIC Interpolator

In this paper, first Cascaded Integrator Comb Interpolator Filter is designed using MATLAB2013a by having design parameter interpolator factor 8, M = 2 & N = 3 whose output is shown in figure 4.

Impulse response of a system refers to reaction of any dynamic system in response to some external change and use for short duration time domain signal. This is the attributes useful for characterizing the Linear Time Invariant systems for all frequencies. It helps to predict the system output will look like in time-domain. Also it describes the reaction of any system in terms of time domain. The impulse response of proposed work is shown in fig. 5.

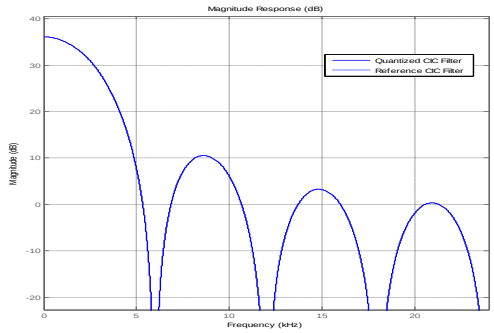

Figure 4 Cascaded Integrator Comb Interpolator Filter

Developing of m-code for CIC interpolator filter is primary step in design flow. Proposed design is implemented using 3 stages to bring about 3 effects; firstly slowdown semi of the filter & better efficiency. Comb section needs less count of delay elements. And last, comb & integrator are self-governing of speed (rate) changer block. Purposed work can be design many different CIC Interpolator Filter by keeping the same filtering structure and programmable rate changer. The pole zero response of proposed CIC Interpolator Filter is shown in fig.6.

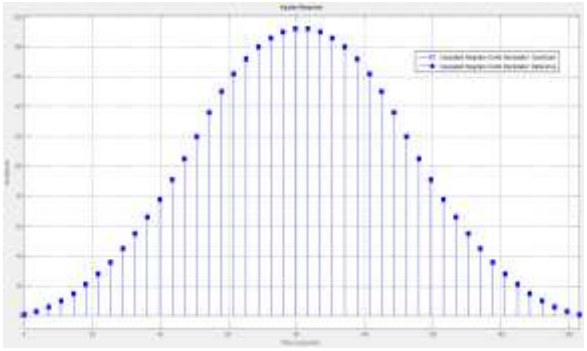

Figure 5 Impulse Response of CIC Interpolator

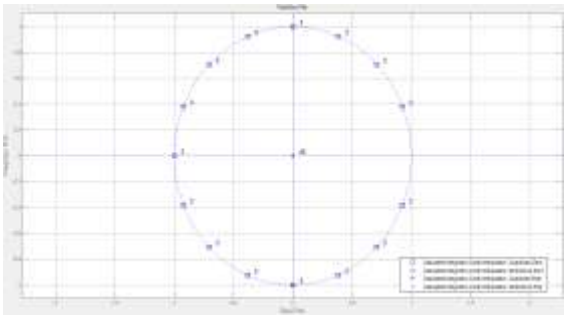

Figure 6 Pole Zero plot of CIC Interpolator Filter

IV. FPGA Implementation Result for CIC Interpolator

The structure of proposed CIC interpolator shown in figure 3 has been realized by developing the equivalent VHDL code in Xilinx ISE and then its verification and behavioral simulation is done with the help of ISE simulator. The CIC Interpolator Filter response is shown in figure 7 [6].

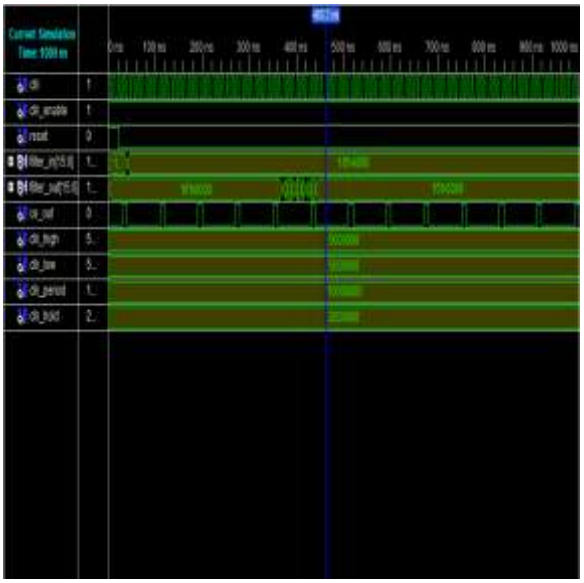

Figure 7 Device simulations in Xilinx for CIC interpolator Filter

The CIC filter is multiplier less consisting only of integrator and differentiator sections. A cascaded of 3 integrators followed by 3 Differentiators. In this paper, focus is on the speed and resource utilization of CIC Interpolator. The verification and implementation is done on two devices, Spartan-3E and Virtex 2 Pro. For the same, RTL schematic and synthesis report is generated using Xilinx synthesis tool. The purposed work is implemented on Spartan 3E based XC3s500E-4FG320 target device and Virtex 2 pro based xc2vp 30-7ff1152 target device. The timing summary for the proposed CIC interpolator with target device Spartan 3E & Virtex 2 Pro is shown in the fig. 8 and 9 respectively.

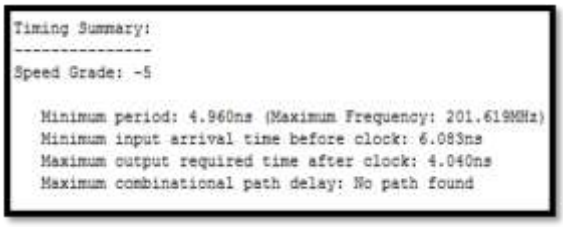

Figure 8 Timing summary of CIC interpolator with Spartan 3E

The developed design has been synthesized on Virtex 2 Pro based xc2vp20-ff1152 and Spartan 3E based xc3s500e-5fg320 target device.

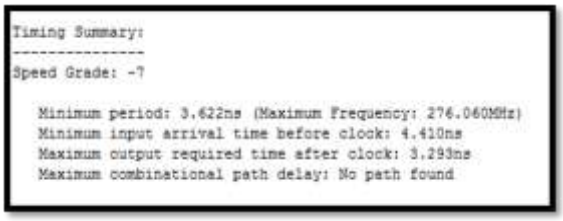

Figure 9 Timing summary of CIC interpolator with Virtex 2 Pro

The comparison table for resource utilization comparison of purposed CIC interpolator with existing work has been shown in the table 1. The optimized CIC interpolator can work on 276.060 MHz by taking 127 Flip-flops and 201.619 MHz in the case of Spartan 3E. The minimum period of developed CIC interpolator is 3.62ns. The purposed architecture can operate at an estimated frequency of 276.060 MHz as compared to existing frequency166.5 MHz in the case of CIC interpolator filter for Software Defined Radios application. In proposed CIC Interpolator Filter there is 33% reduction number of slices, 38% reduction in number of flip-flops, 41% reduction in number of LUTs used whereas 39% improvement has been achieved in maximum frequency. The table 2. Shows the resource utilization of target device Sparten 3E and Virtex 2 pro

Table 1Resource utilization Comparison

Parameter	Existing Design Spartan 3E [1] (Used/Aailable)	Spartan 3E (Used/Available)
Number of Slices	106	70
Number of Flip flop	206	127
Number of LUTs	121	71
Number of bonded IOBs	42	35

Table 2 Resource utilization of target device

Parameter	Spartan 3E (Used/Available)	Virtex 2 Pro (Used/Available)
Number of Slices	70/4656	70/13696
Number of Flip flop	127/9312	127/27392
Number of LUTs	71/9312	71/27392
Number of bonded IOBs	35/232	35/644
Speed	-5	-7

The bar chart of proposed and existing work is shown in fig.10. This comparison chart shows that the proposed work have utilize less resource as compared to existing and also give better performance of improved frequency with reduced number of slices, number of flip-flop and number of LUTs.

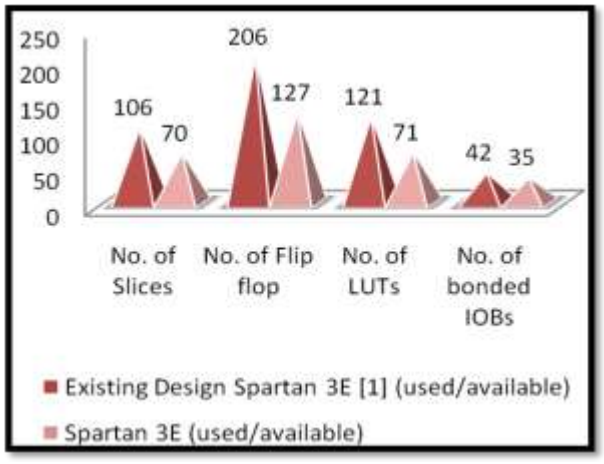

Figure 10 Bar chart of proposed CIC Interpolator Filter with existing work

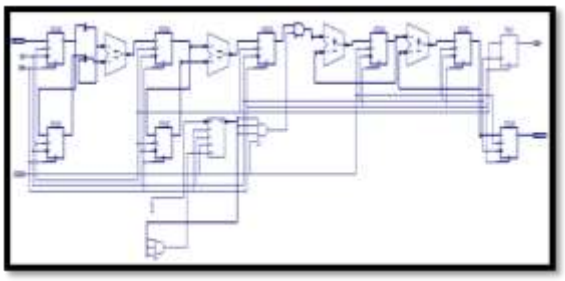

Figure 11 RTL schematic of CIC Interpolator Filter

The timing summary for the proposed CIC interpolator with target device Vertex 2 Pro is shown in the figure 7. The RTL schematic of proposed CIC Interpolator Filter is shown in fig. 11.

V. CONCLUSIONS

The This paper presents a fully pipelined multiplier less approach to design an optimized CIC Interpolator for Software Defined Radios that gives a good throughput for 5G and Wireless communication. The use of FPGA reduces the computational and hardware complexity. The design has been implemented on lower end less expensive Spartan 3E based and Virtex 2 Pro based target FPGA device. The proposed design has shown better resource utilization of slices, flip-flops and LUTs to present an outlay useful solution for Wireless Communication. The developed cascaded integrator comb interpolator filter gives 4.960 ns on Spartan 3E. Also it can operate on 276.060 MHz as compared to existing work that operate on 166.5 MHz.

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