CMOS Design and Performance Analysis of Ring Oscillator for Different Stages

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Abstract- *A ring oscillator is a circuit which consists of an odd number of inverter stages, where the output of each stage of the ring oscillator is given to the input of next stage and output of final stage is then fed to its input. Also, no external input is given to the device, only a reset pulse is provided at once and it drives the circuit. In this paper, the CMOS design and analysis of the ring oscillator have been performed for 5- stage, 7- stage and 9- stage using cadence virtuoso tool in 45nm technology. At the output of every stage of ring oscillator, a capacitor of 500aF and at the load, a capacitor of 5fF is used for different stages. The power consumption is reduced by 79% for 5-stage ring oscillator as compared to 9-stage ring oscillator.*

Keywords— *Ring oscillators, CMOS, System on Chip, frequency, power consumption, delay.*

I. INTRODUCTION

The size of electronic devices has been greatly reduced after the introduction of the integrated circuit technology. While designing any integrated chip, designers have to take care of some parameters. They are power consumption, speed, silicon area and delay. The widely used CMOS (complementary metal oxide semiconductor) technology is used for constructing these integrated circuits, as CMOS circuits provide low power consumption and smaller area. To implement any digital circuit, a complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFET) are used as in [1]. Because of the various advantages, CMOS technology is widely used in commercial applications. Reliability is another important parameter which is also needed for designing of low power circuit as in [2]. In this era, most of the digital and electronic systems show oscillatory behaviour. Oscillators have now become the most important component of all digital, optical devices and communication systems as in [3].

In a CMOS ring oscillator, the output frequency can be controlled easily and also on-chip inductors are also not required. A ring oscillator is a closed loop circuit which consists of an odd number of stages of identical inverters, forming a feedback circuit. The feedback from the output of the last stage to its input causes the desired oscillations. It needs only a power supply to operate and then oscillations start thereafter on its own. The frequency of oscillation can be further changed by either changing supply voltage or changing number of stages. Frequency scaling is another important factor for low power in cell phones and mobile computers as in [4].

Ring oscillators are fabricated using System on Chip designs as they occupy less chip area thereby improving both the cost and yield. If even number of delay cells are used, it can generate both in phase and quadrature phase outputs. But the phase-noise performance of ring oscillators is poor because of their low quality factor as in [5]. So VLSI designs are used widely because of its high-performance and emerging need for miniaturization. Hence, in nanometres scale optimizing design for trade-off between power and performance, integrated circuits is the solution. So, in order to have low power dissipation supply voltage should be low and also to maintain low propagation delay, threshold voltage should be minimized as in [6].

II. RING OSCILLATOR

The basic element in ring oscillator is an inverter cell. The cell consists of complementary pairs of pmos and nmos. The two cells are also symmetric in the way that parameters like channel length, doping are same for both the devices. Inverting operation means when input is low output gets high and vice-versa as in [7]. The inverter is now almost used in all digital designs. The behaviour of any complex circuit can be determined by estimating the results obtained for the inverters. All digital as well as analog designs can be fabricated using CMOS technology as in [8].

CMOS inverter is the combination of MOS transistors i.e. pmos and nmos, where pmos is called as pull-up network and nmos is called as pull-down network. When input is low, nmos is OFF, pmos gets ON, pulling the transistor high and when input becomes high, nmos gets ON, driving the network down and output becomes low as in [9]. It is shown in figure 1.

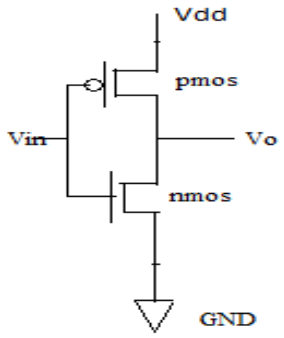

Fig. 1 CMOS inverter

In a ring oscillator, the gain stages are connected in a loop that output from the last stage is given to the input of first stage. The circuit must satisfy the Barkhausen criteria in order to provide sustained oscillation, where the circuit should provide unity voltage gain and it must have a phase shift of 2π. The DC inversion provides π phase shift and the remaining π phase shift is divided equally among the stages in ring oscillator, so each delay gives phase delay of π/N, where N is number of stages in oscillator as in [10]. A basic 3 stage ring oscillator is shown in fig 2.

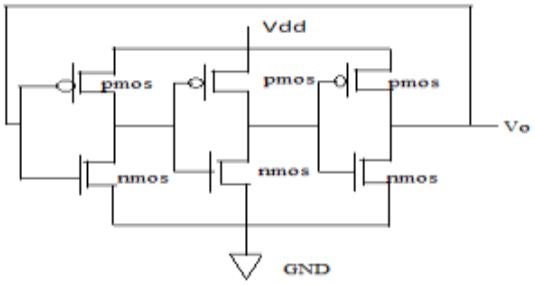

Fig. 2 A 3-stage Ring Oscillator

There are many factors that will decide the performance of any circuit. First is delay that is provided from one stage to another. Here, each inverter gives a delay between the stages, known as propagation delay (□pd). This propagation delay is the average of high to low and low to high transition delay in each stage.

$$\tau pd = (\tau phl + \tau plh)/2 \qquad (1)$$

Second factor affecting performance of ring oscillator is its frequency. For N stage, oscillator frequency is given as:

$$fosc = \frac{1}{\tau pd} = \frac{1}{2N\tau p} \qquad (2)$$

Where □p = □phl = □plh as in [11].

The frequency of the ring oscillator depends upon the □p which in turn depends on the circuit parameters. The two parameters □phl and □plh can be determined for a single stage inverter from the equations given below:

$$\tau phl = \frac{C}{gN(Vdd-Vtn)}\left\{\frac{2Vtn}{Vdd-Vtn} + \ln\left(\frac{3Vdd-4Vtn}{Vdd}\right)\right\} \qquad (3)$$

And

$$\tau plh = -\frac{C}{gP(Vdd+Vtp)}\left\{\frac{2Vtp}{Vdd+Vtp} + \ln\left(\frac{3Vdd+4Vtp}{Vdd}\right)\right\} \qquad (4)$$

Where gN and gP are trans conductance parameters, Vtn and Vtp are threshold voltages of nmos and pmos transistors respectively, Vdd is power supply and C is capacitive load as in [12].

Another factor that is of main concern is power consumption, which depends on supply voltage. When more supply is given to the circuit, it will consume more power and vice-versa. For efficient working of the device, the circuit should consume less power. The power of N stage ring oscillator is given as:

$$Pavg = \eta Vdd * Iavg = \eta NVddQmaxfosc \qquad (5)$$

Where η is the efficiency of the circuit, Iavg is average current.

Also,

$$Qmax = Ctot * Vdd \qquad (6)$$

And

$$Iavg = N * Ctot * Vdd * fosc \qquad (7)$$

Where Ctot is total capacitance of the circuit as in [13].

III. RING OSCILLATOR DESIGNS

The ring oscillators have been designed for different stages using cadence virtuoso tool in 45nm CMOS technology. Here, for 5-stage ring oscillator, 5 inverter stages are cascaded and output of one stage is fed to the input of next stage and final output is feedback to the input of first stage. Also, a sufficient supply voltage should be given and a reset input voltage is applied to the circuit at once, so that oscillations arise spontaneously. At the output of every stage, a capacitor of 500 aF and at the load, a capacitor of 5fF has been used. The schematic of 5-stage ring oscillator is shown in fig. 3.

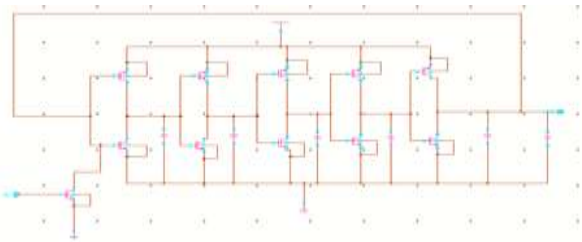

Fig. 3 Schematic Diagram of 5- Stage Ring Oscillator

Similarly, other stages of the ring oscillators have been designed, where 7- inverter stages and 9- inverter stages are used for 7 -stage and 9-stage ring oscillators respectively. The schematic diagrams of 7-stage and 9-stage ring oscillators are shown in fig. 4 and fig. 5.

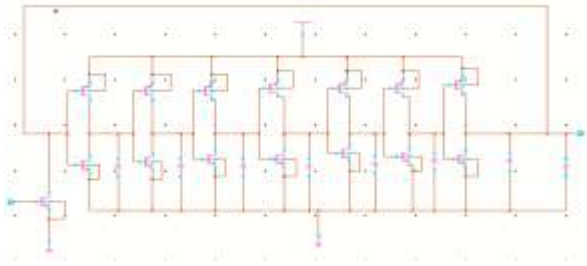

Fig. 4 Schematic Diagram of 7- Stage Ring Oscillator

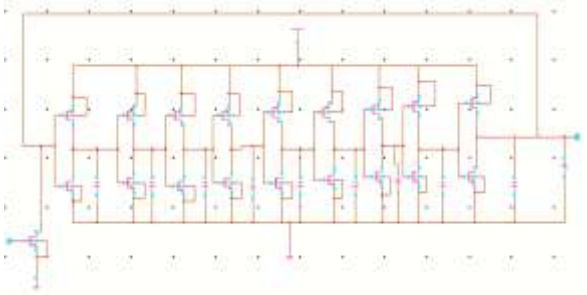

Fig. 5 Schematic Diagram of 9-Stage Ring Oscillator

IV. SIMULATION RESULTS

For a ring oscillator, a reset voltage of 0.34V is applied for a small period of time. As propagation delay is an important factor, the transient analysis for the period 0ns to 20ns is performed. The important parameters are then calculated for different stages of ring oscillator. The output of 5-stage ring oscillator is shown in fig. 6.

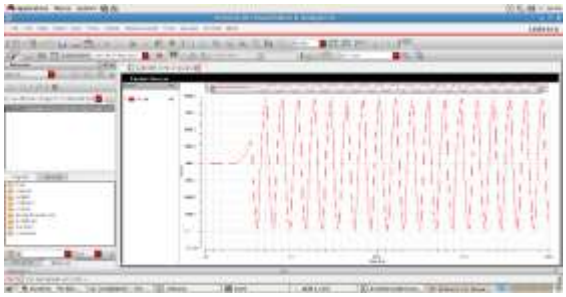

Fig. 6 Output waveform of 5- stage Ring oscillator

Here, oscillations started after a certain period of time and then oscillations are produced with some frequency. Similarly, the output waveforms for 7-stage and 9-stage ring oscillator are shown in fig.7 and fig.8 and different parameters are then calculated for both the stages of ring oscillator.

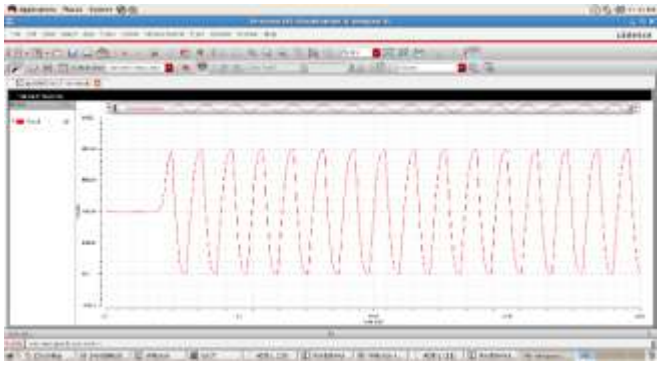

Fig. 7 Output waveform of 7- stage Ring oscillator

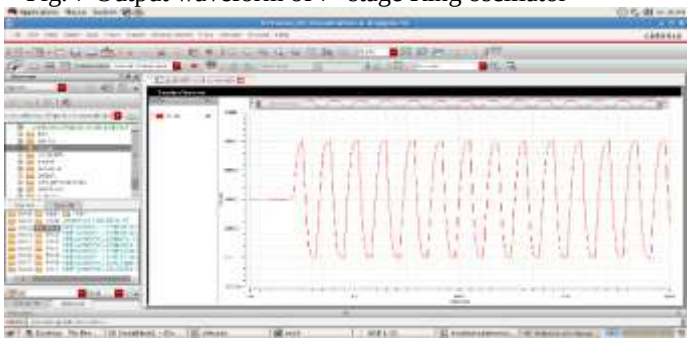

Fig. 8 Output waveform of 9- stage Ring oscillator

The following table shows the important parameters obtained for different stages of ring oscillator.

TABLE I
COMPARISON OF VARIOUS PERFORMANCE PARAMETERS FOR 5-STAGE, 7-STAGE AND 9-STAGE RING OSCILLATOR

	5-stage	**7-stage**	**9-stage**
Oscillation started	2.5ns	2.1ns	1.82ns
Power consumption	0.34µW	0.48µW	0.61µW
Average delay	10.17ps	10.23ps	11.23ps
frequency	1032MHz	831 MHz	751MHz

The following bar chart shows the power consumed by the ring oscillator for different stages.

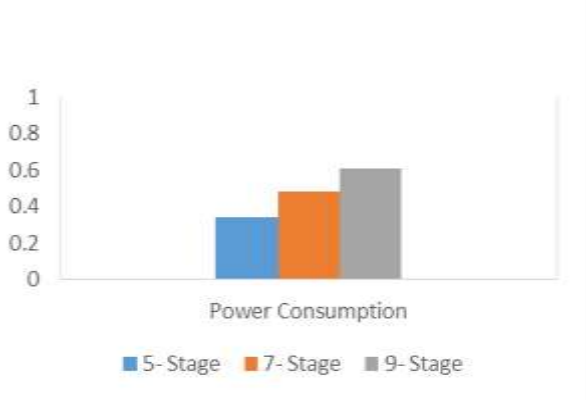

Fig. 9 Bar chart for power consumption in different stages of ring oscillator

V. CONCLUSION

The comparison of a 5-stage, 7-stage and 9-stage ring oscillator has been performed using 45nm CMOS technology and simulated in cadence virtuoso tool. Here, the important performance parameters like frequency, delay, and power consumption were measured for different stages of ring oscillator. In a ring oscillator, with increase in power supply, the frequency and power consumption were also increased and the delay was decreased. The power consumed by the 5 stage oscillator is minimum and from the table, it can be shown that power consumption is 0.34µW for 5 –stage while it is 0.61µW for 9-stage ring oscillator. Also the frequency achieved is maximum 1032 MHz for 5-stage ring oscillator.

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