Sigma-Delta Modulator Design and Analysis for Audio Application

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Abstract— *A Sigma-delta modulator is designed in 180nm CMOS process for digital Audio applications. This design is simulated on S-Edit of Tanner EDA tool. In this design continuous time sigma-delta modulator is implemented to reduce the noise problem. This sigma-delta modulator also helps to reduce power consumption of circuit. In these design two stage op-amps is used to implement modulator. Also this design uses second order continuous time modulator for increasing SNR. Circuit design an 11bit low power sigma-delta modulator for digital audio application is given, using a single bit quantizer. The power supply for this circuit is only 1.8v; the modulator achieves 72dB SNR in a 20 KHz BW, while consuming 1mW.*

Key Words—*Analog-to-digital converter (ADC), continuous time, data converter, over sampling, sigma-delta modulation.*

I. Introduction:

There is huge demand in the wired ,wireless communication market for high performance .Analog to Digital Converters (ADC) is the applications for low power dissipation, low noise, high speed, less Offset voltage are requirements for mobile and portable devices. ADC (Analog to Digital Converter) is the bridge linking the analog world and the digital world. It converts the analog signal to the digital signal, and facilitates for the storage, processing and transmission of the data [1]. The ADCs are generally classified as Nyquist rate ADCs and Oversampling ADCs. These are classified based on the rate at which the signal is sampled relative to the signal bandwidth. Digital signal processing technique replaces complex and precise analog components in oversampling converters. This gives a scope to achieve much higher resolution than the Nyquist rate converters. Sigma Delta ADC, a type of oversampling ADC is highly tolerant to analog circuit imperfections, thus making it a good choice to realize embedded ADC interfaces in modern systems-on-chip (SoCs) [2] [4]. It has been accepted as choice for modern voice band, audio and high resolution industrial measurement application. The Sigma Delta (ΣΔ) ADC is now used for much low cost, low power, high resolution applications. The method in which high-resolution signals are encoded into lower resolution signals using pulse-density modulation is called as Sigma-Delta modulation. Using DT (Discrete-Time) and CT (Continuous-Time) techniques Delta-Sigma modulator can be implemented which is one of the key building blocks. Compared to their DT counterparts, more attention have been attracted by CT Delta-Sigma modulators due to their advantages in terms of reduces the power consumption ,high speed ,low noise, high resolution and intrinsic anti-aliasing capability [3].

Sigma-delta Modulators can be categorized as*:*

1. Single-Loop versus Cascade Sigma-delta Modulators (attending to the number of quantizers employed). Sigma-delta Modulators employing only one quantizer are called single-loop topologies, whereas those employing several quantizer are often named cascade or MASH Sigma-delta Modulators.

2. Single-Bit versus Multibit Sigma-delta Modulators (attending to the number of bits in the embedded quantizer).

3. Low-Pass versus Band-Pass Sigma-delta Modulators (attending to the nature of the signals being converted).

4. Discrete-Time versus Continuous-Time Sigma-delta Modulators (attending to the nature of loop filter dynamics). The DT loop filter used in the Sigma-delta Modulators. However, CT Sigma-delta Modulators can be also implemented in practice. According to this classification criteria, hybrid CT/DT Sigma-delta Modulators take advantage of the benefits of both DT and CT implementations.

II. Background:

Depending upon the sampling rate Analog-to-Digital

Converter (ADC) can be divided in to two parts. One which samples the signal at Nyquist rate that is fN=2F, Where fN is the sampling rate and F is the bandwidth of the input signal, while the other samples the signal at a much higher sampling rate then the signal band width this type of sampling is called oversampling and the converters are called oversampling converters. These converters have an ability to achieve high resolution, high reliability, and performance ΣΔ ADC comes under the category of oversampling ADC [5]. Then Nyquist rate converters, some of the Nyquist rate converters are following.

- Flash ADC
- Ramp ADC
- Successive Approximation ADC
- Pipeline ADC

The architectural and circuit details of the modulator from the subject of the remainder of this paper, which is organized as follows. In III Section discusses the architecture of sigma-delta modulator and section IV presents design of various sub-blocks of the modulator. In section V explained experiment result and in section VI concludes the paper.

III. Architecture for modulator:

Sigma-delta ADC has two main parts one is analog modulator another is digital filter, the performance of the ΣΔ ADC is dependent on the performance of modulator, so design of modulator is very important. ΣΔ modulator has proven that they work at low frequency, high performance application. ΣΔ modulators are also known as noise shaping modulators because of their quantization noise association with various functions that shapes the noise frequency spectrum. The differential function decides (determines) the order of modulator. A higher order modulator has a higher differential function order, which further suppresses the in-band quantization noise. Differential function is the factor which makes ΣΔ modulators ADC to achieve high resolution than conventional ADCs when sampling rates are increased.

IV. Design of sub-block :

Op-amp:-

The operational amplifier (Op-amp) is the critical block of ΣΔ modulators which determine the performance of the ADC. In the electronics circuit the op-amp is most common building block. The op-amp is designed as a two-stage op-amp, with first stage using a NMOS input pair reduce power dissipation. The op-amp is miller compensated using capacitor Cc. As shown in the fig:1. The value of Cc is 1.5 pf and tail current is 20 µA. The two stage op-amp ignores the buffer stage. The differential amplifier is the first stage and most dominant pole of the system is present in this stage. The differential amplifier has ability to convert differential input in to single ended output with high gain.

The second stage contributes inferred noise due to large gain of the first stage miller compensation used to facilitate pole splitting in order.

A two stage design is more effective in reducing the in-band noise arising from op-amp non linearity when compared with a single stage op-amp.

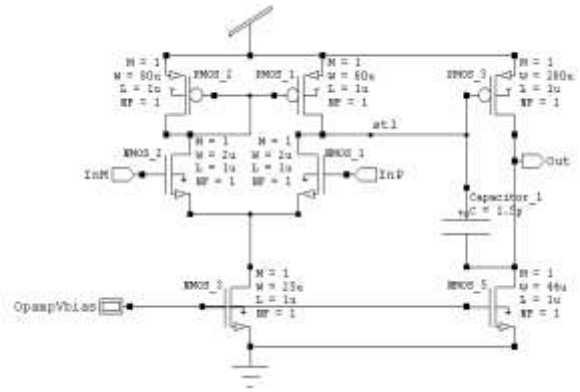

Fig.1: Schematic diagram of Op-amp

Integrator:-

Continuous time integrator have their advantage the amplifier setting requirement are generally more relaxed than in switched-capacitor circuits, a very high oversampling ratio is available .The oversampling ratio in SC integrator is limited by the achievable BW of the op-amp .This makes CT ΣΔ modulators very appealing for high speed application. The integrator is a circuit using op-amp that performs the mathematical operation of integration .The integrator acts like a storage element that "produces a voltage output which is proportional to the integral of its input voltage with respect to time". In other words the magnitude of the output signal is determined by the length of time a voltage is present at its input as the current through the

feedback loop charges or discharges the capacitor as the required negative feedback occurs through the capacitor.

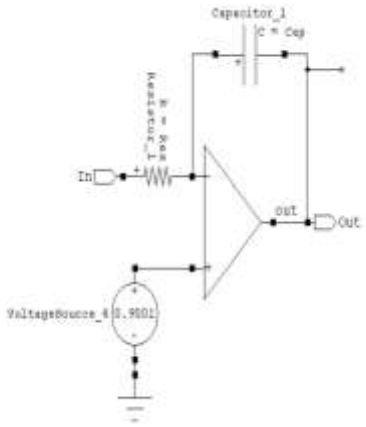

Fig.2: Schematic diagram of Integrator

Adder:-

The Summing Amplifiers a very flexible circuit based upon the standard Inverting Operational Amplifier configuration. In the Inverting Amplifier if we add another input resistor equal in value to the original input resistor, R in we end up with another operational amplifier circuit called a Summing Amplifier, "Summing Inverter" or even a "Voltage Adder" circuit as shown below.

The output voltage, (Vout) becomes proportional to the sum of the input voltages, P1, P2, etc. So, the original equation for the non-inverting amplifier can be modified to take account of these.

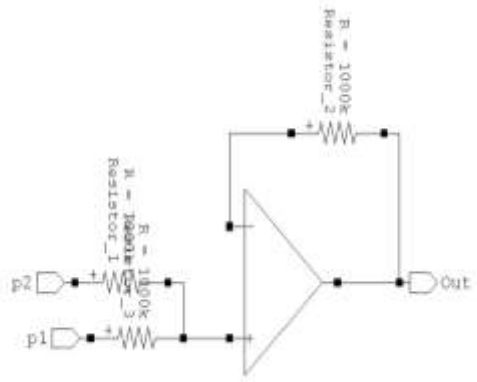

Fig.3: Schematic diagram of Adder

One bit DAC and Comparator:-

Comparator or quantizer is one of the core components of any analog-to-digital converter (ADC).Inverter is used as 1 bit comparator. If we increase size of inverter it acts like a comparator. Here we use logic chain due to which work fast as compared to other and also gain is multiplied. A 1 bit DAC convertor converts the 1 bit digital output of positive .comparator to the analog signal. Since, it is only 1bit the corresponding analog output will also have two levels and is almost similar to the digital input. The DAC has two reference levels +Vref and –Vref . If the digital input is "1" then the DAC output will be –Vref. A 1 bit DAC can be designed using a simple multiplexer circuit, which selects between the +Vref and –Vref signals depending on the "1"bit digital input signal. Fig.4: shows the circuit diagram of a "1" bit comparator.

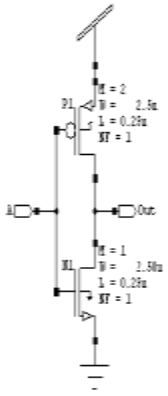

Fig.4: Schematic diagram of Comparator

V. Result:-

The second order continuous-time sigma-delta modulator was implemented using Tanner. Fig.5.shows the output waveform of modulator frequency Vs voltage in which SNR are calculated 72dB with a1.8v supply voltage. Also Table .1. shows the Measurement Results of Sigma-Delta Modulator. The SNR in the table is defined as

$SNR=10\log_{10}$ (Power signal/Power noise)

$SNR=10\log_{10}(S/N)$

Where the proposed modulator achieves the highest SNR while maintaining good FoM.

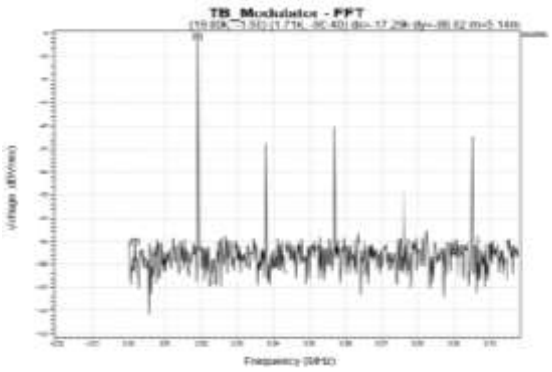

Fig.5: Simulation result of second order ΣΔ Modulator

Table.1.Measurement Results of Sigma-Delta Modulator

parameter	Value
Technology	180nm
Power Supply	1.8v
Signal Bandwidth	20KHz
Power Consumption	1mW
SNR	72.39
ENoB	11

VI. Conclusion:-

We present the design an 11 bit low power continuous time sigma-delta modulator for digital audio application, using a single bit quantizer. The proposed continuous time second order sigma-delta modulator circuit was simulated by T-spice. The power supply for this circuit is only 1.8v was chosen, the modulator achieves 72dB SNR in a20KHz BW, while consuming 1mW power.

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