Sigma-Delta Modulator Design and Analysis for Audio Application

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Abstract- *Analog to Digital converters fined different usage in various receiver design architectures. Analog modules appear to be precise and quite resistant to a variety of sources of noise and interference. Most of the highly precise A/D converters involve the use of sigma-delta modulation which is associated with oversampling and noise shaping. These converters use the least parasitic capacitances and small feature sizes characteristic of scaled VLSI technology by trading speed for resolution. Second order 11 bit power optimized continuous time ∑-Δ modulator has been presented in the paper. 1.8 V supply is used to operate this modulator. This paper compares the continuous-time second-order modulator to several alternative modulator architectures available in the audio frequency domain.*

Keywords — *Analog-to-digital converter, delta-sigma modulator, low power, low voltage, over sampling.*

I. Introduction:

There is huge demand in the wired, wireless communication in day to day life for larger bandwidths and operating at high performance .Analog to Digital Converters (ADC) is the applications for low power dissipation, very high speed, low noise, less Offset voltage are requirements for mobile and portable devices. ADC (Analog to Digital Converter) is the bridge linking the analog world and the digital world. It converts the analog signal to the digital signal, and facilitates for the storage, processing and transmission of the data [1]. The ADCs are generally categorized as Nyquist rate ADCs and Oversampling ADCs. These are classified based on the rate at which the signal is sampled relative to the signal bandwidth. Complex and precise analog components are replaced by digital signal processing techniques in oversampling converters. A scope to achieve much higher resolution is provided by this than Nyquist rate converters. Sigma Delta ADC, a oversampling type ADC is highly tolerant to analog circuit imperfections, thus providing it a one of the best choice to realize embedded ADC interfaces in modern systems-on-chip (SoCs) [2] [4]. It has been accepted as choice for audio and video processing system, medical imaging, modern voice band and high resolution industrial measurement application. The Sigma Delta (ΣΔ) ADC is now used for noise shaping, very low power, high resolution applications. The method in which high-resolution signals are encoded into lower resolution signals using pulse-density modulation is called as Sigma-Delta modulation. Using DT (Discrete-Time) and CT (Continuous-Time) techniques Delta-Sigma modulator can be implemented which is one of the key building blocks. Compared to their DT counter parts, much attention have been attracted by CT Delta-Sigma modulators due to their advantages in terms of high resolution, operate at higher sampling rate, reduces the power consumption ,low noise, high speed and intrinsic anti-aliasing capability [3].

Sigma-delta Modulators can be distinguished as:

1. Single-Loop versus Cascade Sigma-delta Modulators (attending to the number of quantizers employed). Sigma-delta Modulators employing only one quantizer are called single-loop topologies, whereas those using several quantizers are often named cascade or MASH Sigma-delta Modulators.

2. Single-Bit versus Multibit Sigma-delta Modulators (attending to the number of bits in the embedded quantizer).

3. Low-Pass versus Band-Pass Sigma-delta Modulators (attending to the nature of the signals being converted).

4. Discrete-Time versus Continuous-Time Sigma-delta Modulators (attending to the nature of loop filter dynamics). In Sigma-delta Modulators the DT loop filter used . However, in practice CT Sigma-

delta Modulators can also be implemented. According to this classification criteria another type of sigma-delta modulators, known as hybrid CT/DT Sigma-delta Modulators take advantage of the benefits of both DT and CT implementations.

II. Background:

Depending upon the sampling rate Analog-to-Digital Converter (ADC) can be distinguished in to two parts. One which samples the signal at Nyquist rate that is fN=2F, Where fN is the sampling rate and F is the bandwidth of the input signal, while the other samples the signal at a higher sampling rate then the signal band width this type of sampling is called oversampling and the converters are called oversampling converters. These converters have an ability to achieve high reliability, high resolution and performance and they simplify the requirement placed on the AAF. ΣΔ ADC comes under the category of oversampling ADC [5]. Then Nyquist rate converters, some of the Nyquist rate converters are following.

- Flash ADC
- Ramp ADC
- Successive Approximation ADC
- Pipeline ADC

III. Literature review:

Shanthi Pavan [4] present design consideration for low power continuous-time sigma-delta convertor (CTSDMs) showing design details and measurements result for 15 bit audio modulator. It proves that a multibit quantizer with a proper choice of NTF can result in a modulator performance that is relatively immune to loop-filter time constant variations, clock jitter, and comparator offset. A third order active-RC loop filter, an efficient excess-delay compensation scheme, and a very low power 4-bit flash quantizer to reduce power dissipation. Fig.1.(a) shows conventional ways of combating excess delay using direct path around the quantizer using a second DAC. Fig.1. (b) shows the circuit to complete the same task using a feed-in capacitor Cx. Fig. 2. shows the output waveform.

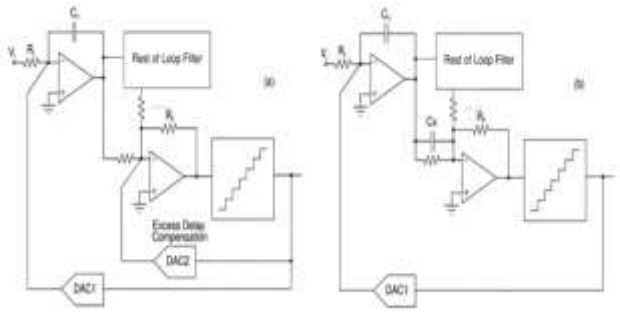

Fig.1.Excessdelaycompensation(a)Conventional (b)Proposed

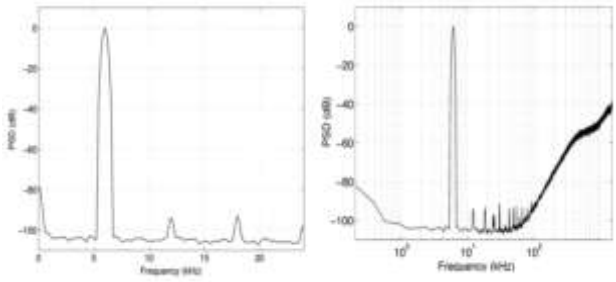

Fig.2. Complete spectrum for a 6 kHz input

Keith A.O'Donoghue [5] This paper discusses about a digitally corrected 5-mW 2-MS/s SC ΔΣ ADC in 0.25-μm CMOS with 94-dB SFDR, 75-dB SNDR, and 90 -dB THD. First, high bias currents were used in the op-amps of the front-end integrators I_1 and I_2 to achieve good fourth-order performance without correction. Then, those bias currents were reduced, and the output was digitally corrected using coefficients found by a parallel second-order structure. This resulted in a 38% power savings after correction. Peak SFDR and THD were improved by over 25 dB and the peak SNDR was improved by 9 dB after correction. A competitive FoM of 0.85 pJ/conv was achieved before correction due to power savings from the feed-forward architecture and passive capacitive summing at the quantizer inputs. The power dissipation before correction is limited by the need to avoid distortion that would arise from insufficient slew rate. The savings in power dissipation measured after correction came entirely from the correction, allowing a reduced FoM =0.56 pJ/conv to be achieved; similarly the active area is 0.39 mm^2 in 0.25-μm CMOS. Below fig .3. Shows that feed-forward paths significantly reduces the input components in the integrator outputs. The other advantage is that it only requires single feedback path

instead of feedback to the inputs of both integrators. Fig.4. shows the output.

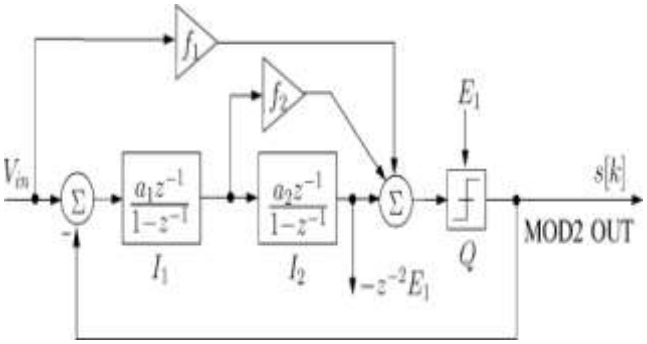

Fig.3. Block diagram of the second-order ΔΣ modulator with feed forward paths f_1 and f_2.

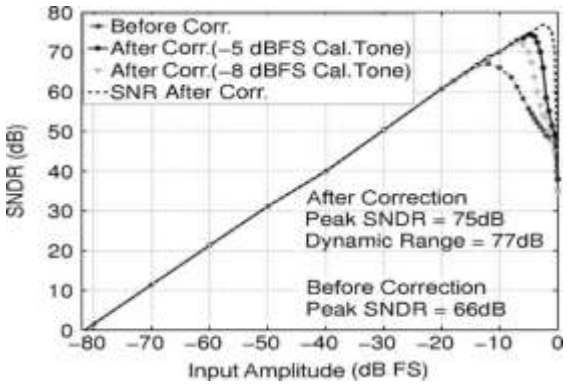

Fig.4. SNDR versus input signal amplitude

In this paper **Liyuan Liu [6]** design the 15-bit,1-V supply ΣΔADC for audio application. The second order CIFB ΣΔ modulator with a 3-bit internal quantizer is adopted. The NTF is optimized so that the performance of the modulator is very tolerant to the linear gain as well as coefficients variations. A single-capacitor analog summing is suggested to avoid signal attenuation problem. For the digital decimation filter design, low hardware cost implementation method is used. Fabricated in 0.18µm CMOS, the overall ADC achieves 9103dB peak SNDR and 93 dB DR with 16kH$_z$ bandwidth. The analog modulator occupies 0.3mm^2.The total power dissipation is 190µW for the modulator and 170 µW for the decimation filter. Below Fig.5. Shows architecture for above sigma delta ADC & Fig.6 shows Measured output spectrum of the ΣΔADC

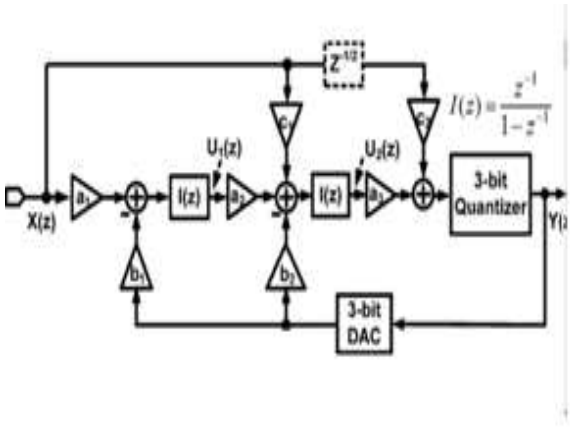

Fig.5. Architecture of Sigma delta modulator

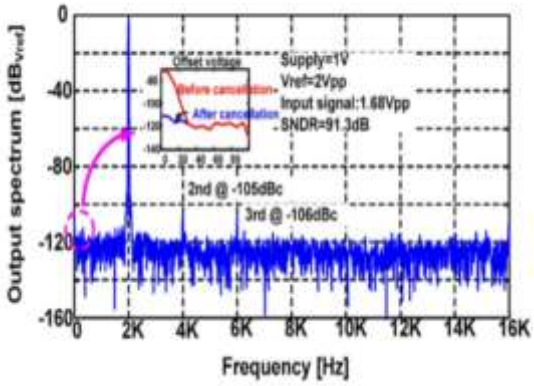

Fig.6.Measured output spectrum of the ΣΔADC

In this paper **Alireza Nilchi [7]** has presented, a low power switched capacitor integrator based on a capacitive charge-pump (CP),and its practical effects are discussed. The CP integrator is used as the first stage of sigma delta ADC. The 10kHz BW of CP ADC achieves 87.8 dB SNDR, while consuming 148uW,The conventional ADC has similar performance but dissipates 241uW.The energy required per conversion step for the CP based ADC is almost 40% lower than that of the conventional ADC. As Compared to conventional ADC ,the CP based modulator achieves the suited for sensory or wireless system with small inputs ,where it can significantly reduce the power consumption of dominant front end circuits. Below Fig.7.(a) shows conventional SC integrators & Fig.7. (b) shows proposed CP integrators used in sigma delta modulators. Fig.8. shows measured SNR and SNDR for the CP and conventional sigma delta modulators.

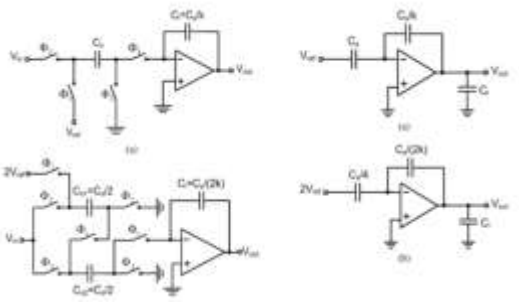

Fig.7. (a) conventional SC integrator,(b)proposed CP integrator

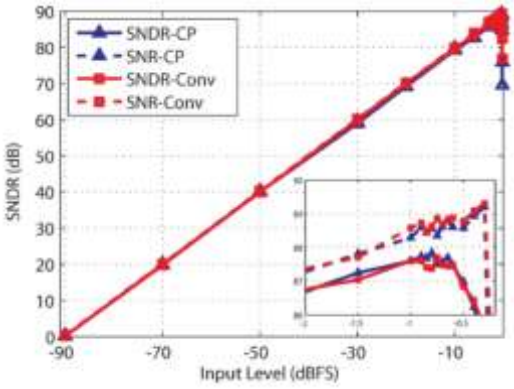

Fig.8.Measured SNR &SNDR versus i/p signal level for the CP and conventional ΣΔ modulators

IV. Proposed work:

The modulator is the analog part of sigma delta ADC, the resolution of the converter depends upon the order of the modulator order of the modulator is set by the sampling ratio.

By balancing three major design aspects the resolution of the sigma delta ADC can be increased they are the over sampling ratio, quantizer resolution and order of modulator. The use of a higher order modulator reduces the superimposed noise in the bit stream. The in band quantization noise can be reduced by doubling there sampling frequency. The input analog signal can directly be sampled using an input over sample clock as it uses the ***process*** of oversampling this also eliminates the use of anti-aliasing filter due to oversampling ***process***.

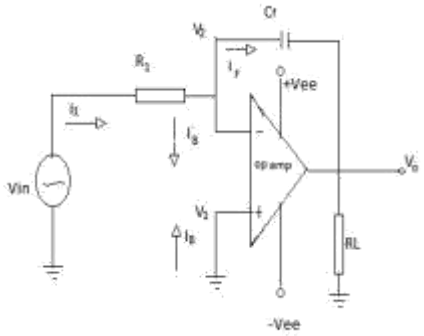

Fig.9. Block dia. of sigma-delta modulator

The modulator consists of an Integrator, Difference Amplifier, 1 bit latched Comparator (ADC) and a 1bit DAC. Fig .9.shows the basic structure of a modulator. Here we use continuous time second order single loop sigma delta modulator. By increasing the order of the loop filter "n" ideally and noise shaping, the SNR of the convertor (modulator) can be increases.

Implementing above modulator first step is to design a op-amp. The op-amp is a fundamental building block in analog integrated circuit design. We use two stage CMOS op-amp. We can use the op-amp, with buffer or without buffer at the output. Without buffer at the output configuration is used for the comparator, integrator where the load is fully capacitive. The load capacitance C_L is used in estimating the op-amp compensation. Fig.10.shows the basic block diagram of op-amp.

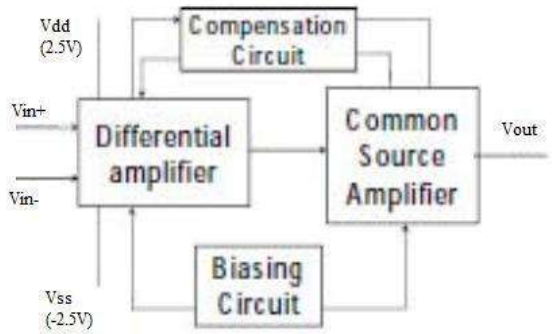

Fig.10.Block Diagram of Op-amp

The op-amp Integrator is an essential circuit component in any analog circuit that performs mathematical operation of Integration mainly in solving differential equation. The integrator also used as a storage element in analog computing. Following Fig.11. shows the integrator

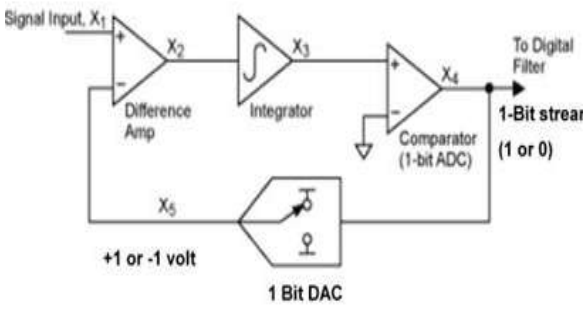

Fig.11.Circuit Diagram of Integrator

The summing amplifier is a very flexible circuit based on the standard operational amplifier, which can be used for combining multiple inputs. it has a single input voltage applied to the inverting input terminal. If more resistors are added to the input equal to the input resistor, we end up with another operational amplifier called as summing amplifier. Fig.12. shows the circuit of a summing amplifier.

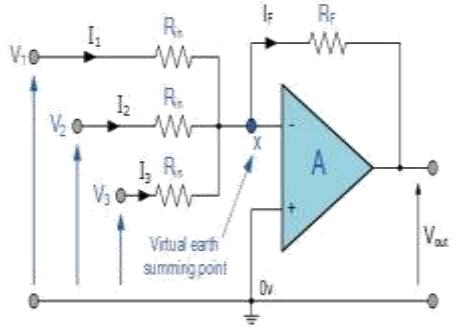

Fig.12. Basic circuit of Summing amplifier

It is a device for converting a digital usually binary code to analog signal (current, voltage or charges).The DAC acts as an interface between digital world and analog real world. The DAC inputs a digital signal and outputs an analog signal in form of current, voltages or charges.Fig.13.shows the basic symbol for a DAC.

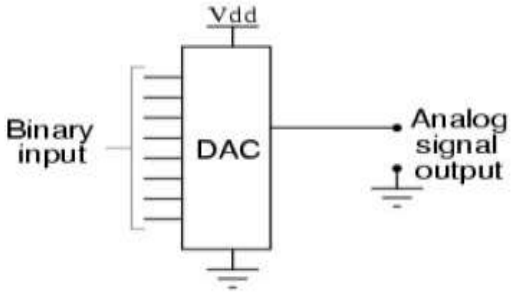

Fig.13.Block Diagram of DAC

The above all the basic blocks like integrator ,summing amplifier, comparator and the DAC are integrated together to design the Sigma Delta ADC architecture ,Which is being given by a input analog signal and results in a series of discrete digital pulse stream of data.

V. Conclusion:

Sigma delta modulators are widely used in wired & wireless applications. This paper incorporates Second-order modulators efficiently exchange the high speeds of CMOS VLSI technology for high analog resolution ,low power and audio application without sacrificing modulator stability or placing severe constraints on the precision of the analog circuits. Besides requiring more complex and precise anti-aliasing filter, architectures that allow the use of lower over-sampling ratios generally depend on precise component matching or better analog circuit presentation.

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