Comparator Design Analysis using Efficient Low Power Full Adder

Meena Aggarwal[1], Rajesh Mehra[2]

[1]*ME student (ECE)* , [2]*Associate Professor*

National Institute Of Technical Teachers Training And Research, Chandigarh, India

Abstract- *In today's electronic industry, low power has emerged as principle theme. This reduction in power consumption and also in form of area, it makes the devices more reliable and efficient. So, CMOS technology has been developed which become best known for low power consumption and miniaturization in chip sizes. In a large-scale digital systems design, Comparator is a eminent to be the useful unit of digital systems and signal processors. In this paper , 32-bit comparator has been designed.. The above said designs are prepared by combining two different design approaches: Gate Diffusion Input (GDI) and PTL. These two techniques are hybridized in a way such that it takes the advantage of both the approaches in order to obtain the good quality performance of the circuit. The performance of this proposed 32-bit comparator by hybridizing the two design styles has been compared in terms of transistor count and power and also shows the effect of voltage variations on the power consumed by the circuit. The transistor level schematic are designed and simulated for its behavior using DSCH-3.1.The layout of simulated circuits are created using Verilog based netlist file which is then simulated in Microwind 3.1 to analyze the performance of comparators at 180 nm CMOS technology. The results shows that with the decrease in voltage, the power consumption also decreases but low voltage level results in increase delay.*

Keywords- *ALU, Full Adder , Comparators, CMOS style, Digital Arithmetic, Full, GDI technique, Hybrid, PTL logic, Power Efficient.*

I. INTRODUCTION

Now a day for every 2 years, it is challenged for semiconductor industries are challenged to scale down CMOS technology which leads to high integration, high speed and low cost chips because of small areas of dies. As CMOS technology is scale down, there is also reduction in supply voltage which results in low power consumption for integrated circuits. So, CMOS technology has important contribution in the majority of commercial applications. In comparator circuit design, the CMOS technology has a central position in modern designing methodology. Comparator is one of the fundamental units which have extensive application areas in VLSI systems such as CPU, decoding of microprocessor instructions The comparator has very useful component in many areas such as multi-

access memories, parallel computing and multiprocessing [1]. So, in order to have efficient processing, it is required to design high speed, low power and area efficient comparator circuits. The basic function of the comparator is to compare two n-bit numbers and find the output that depends on the results of comparison. It can be either of the three possible outcomes i.e., whether and which number is greater then, equal to or less then. It is required to have 2n inputs & 2^{2n} entries in the truth Table if two n-bit numbers have to be compared [2].

These are designed from basic logic gates i.e., AND, NOR and NOT which compare the binary signals present at their input terminals and gives the output based on the signals applied at the input terminal. Generally, there are two types of comparator circuit:
a) Equality comparator
b) Magnitude comparator

a) Equality Comparator: This comparator is a simplest multi-bit logic comparator that is used to compare the two numbers bit by bit and give the result at the output that whether these numbers are equal or not. In electronic lock system and also in security providing devices in which password consists of binary numbers of multiple bit which act as a input to the comparator and has to be compared with another preset word, these types of comparator has significant importance

b) Magnitude Comparator: This comparator also performs the same function of comparison but it provides two more outputs along with equality. The output depicts whether a number is greater than, less than or equal to the other number. For example, when we add and subtract binary numbers, we have to compare those numbers and find whether the value of first input is greater than, smaller than or equal to the value of second input [3].The basic diagram of 1-bit comparator is shown in Fig. 1.
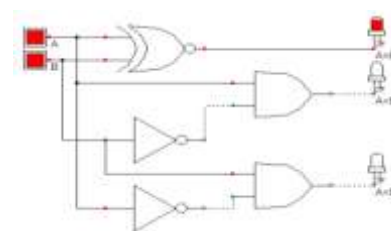

Fig. 1: Single-Bit magnitude Comparator [3]

II. VLSI SCALING

In order to achieve the growth or to raise the success of VLSI industry, the scaling of devices has significant role that results in dense and faster integration of the device by utilizing small area. As the technology moving towards the very large submicron region, the processing capacity per chip and operating frequency increases rapidly which in turn results in increased power dissipation and leakage current and circuit reliability become the key issue [4]. Hence the overall performance of the circuit is affected. Reliability is also an important issue which points to the need for low power design. So, VLSI designers have to make the balance in performance of the circuits and power dissipation with the scaling in technology. The MOS transistors are the basic element of integrated circuits. By performing the scaling on MOS characteristics, it will improve its size, cost and performance. There are various scaling methods by which scaling can be done on VLSI circuits. By varying the one parameter, it will affect the performance of another. The various methods of scaling are:

i) **Voltage Scaling:** With the reduction in supply voltage, the power dissipation of the circuit can be reduced at a constant clock frequency but on the other hand the propagation delay increases. This is shown by the relation given as:

$$T = C_L V_{DD}/l \qquad (1)$$

The drawback of voltage scaling is that some circuit styles cannot function at low supply voltage [4].

ii) **Load Scaling:** It is another method to improve the performance of the circuit by reducing the power dissipation. If load capacitance is large, it draws more power supply hence increases dynamic power dissipation. So, scaling is to be done in terms of load capacitance [5], [6].

iii) **Technology Scaling:** To optimize the high performance of the circuit, CMOS technology has to be scale down continuously. With the new technology generation, overall lateral and vertical dimensions of the transistor are scaled down by a factor. And also if there will be certain limit after which if further scaling in technology will be there then number of limitation factor arises like sub-threshold conduction, body effect, short channel effect etc.

iv) **Transistor Sizing (Width Scaling):** It is also called channel width scaling. As the width of the transistor reduces, the power dissipation gets reduced and also there will be reduction in area of the circuit. On the other side, the propagation delay decreases if there will be increase in transistor width.

III. HYBRID FULL ADDER MODULE

The full adder circuit is basically designed by using X-OR gate and 2:1 MUX. By enhancing the performance of the XOR gate, the performance of the full adder can be improved [7]. Several filtering have been made in its structure in terms of transistors in order to increase the performance of full adder [8]. There are lot of designs have been implemented in past in order to optimize the design which utilizes the eight transistors or six transistors that are conventionally used. The main objective is to reduce the transistor count so as to reduce the size of XOR gate so that large number of devices can be configured on a single silicon chip. Hence increases the circuit performance in terms of area and power. The full adder is designed by hybridizing PTL and GDI logic which has been implemented by using only 9 transistors shown in Fig.2.
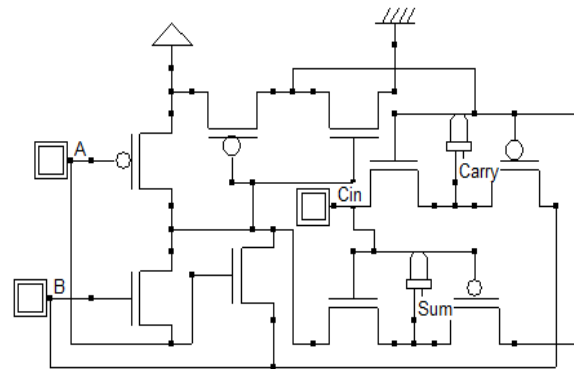

Fig. 2: Hybridized Full Adder Module

This full adder design consists five transistors in module1 i.e. XOR-XNOR which has been implemented using PTL logic and module 2and 3 has been implemented by using 2T GDI cell to provide the Sum output and Carry respectively.

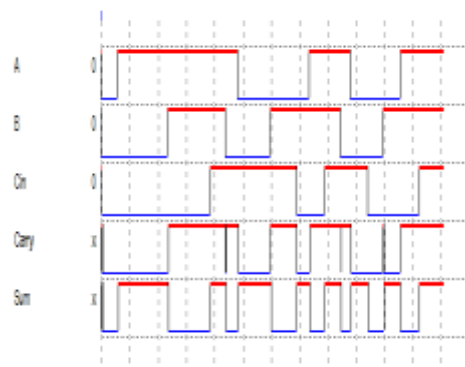The timing waveform shown in Fig. 3 is the result of logic level simulation at DSCH.

Fig. 3: Timing Waveform of full adder module

The layout of a full adder designed by hybridized approach in Microwind3.1 and simulation is performed using LEVEL-3 model.
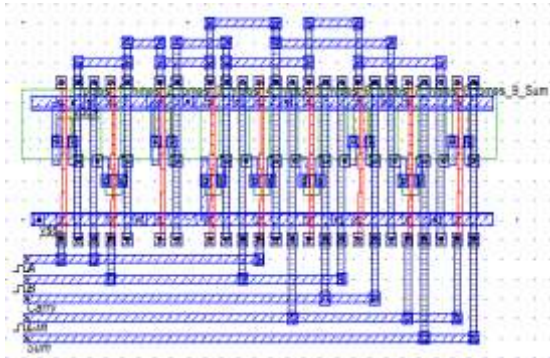

Fig. 4: Layout of GDI-PTL based full adder

A. Schematic Design of XOR-XNOR module

The XOR-XNOR which plays important role in designing the full adder is shown in Fig.5 has been designed by the PTL logic and consist only 5 transistors which is least as compared to all previous discussed designs [9].
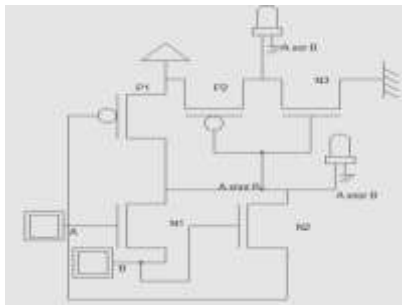

Fig. 5: PTL based XOR-XNOR Module

It consists of 3 NMOS and 2 PMOS transistors which provide an area efficient design as compared to previous discussed designs. The MOS logic states is shown in Table 1 for both XOR and XNOR output is obtained by applying four different input combinations,.

Table 1 Analysis of XOR-XNOR Module

Inputs		MOS Logic State					Outputs	
A	B	N1	N2	N3	P1	P2	A $\oplus$ B	A $\odot$ B
0	0	OFF	OFF	ON	ON	OFF	0	1
0	1	OFF	ON	OFF	ON	ON	1	0
1	0	ON	OFF	OFF	OFF	ON	1	0
1	1	ON	ON	ON	OFF	OFF	0	1

B. Schematic of GDI based 2:1 MUX used in full adder

The XOR-XNOR outputs become the inputs for the 2T GDI based cell. Finally the Sum and Carry output of the module 2 and module 3 can be expressed as [10] :

$$SUM = C(A \ominus B) + C'(A \oplus B) \qquad (1.2)$$

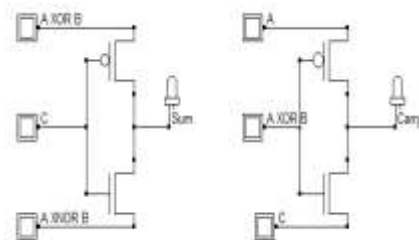$$CARRY \, C(A \oplus B) + A(A \ominus B) \qquad (1.3)$$

Fig. 6: GDI cell based Module 2 and Module3

IV. PROPOSED COMPARATOR

In Fig.7, the 2-bit magnitude comparator is designed which provide the three output i.e. whether first number is less than, equal to or greater than the third number. In this 9T hybrid full adder block is used whose schematic is shown in Fig.2. This 2-bit comparator which is designed by hybridizing approach of PTL and GDI provide good performance by reducing transistor count as well as power because PTL logic helps in reducing the transistor count and GDI logic gives good result in terms of power consumption also maintain low complexity of the circuit [11]-[15]. So, to improve the performance for both parameters in one circuit, both techniques are hybridized [12].
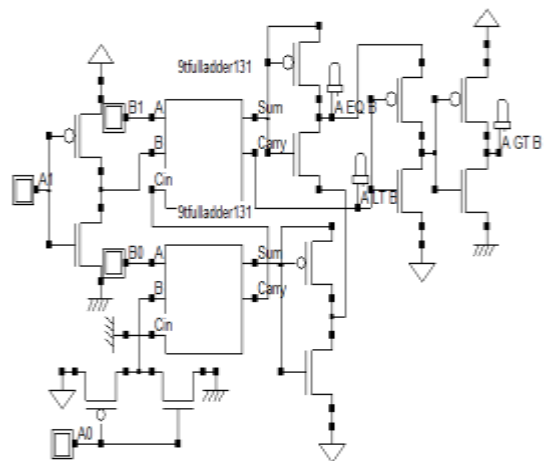

Fig. 7: 2-bit Hybridized comparator

By cascading the above designed comparator, 32-bit implementation of comparator is done which is shown in Fig.8. This circuit is designed in DSCH3.1. It is obtained by cascading sixteen 2-bit comparator circuit and finally the three outputs which is the result of comparison of all the 32-bits of each input A and B. Firstly, the most significant bit is compared if it is equal then next bit is compared and so on. In this way all the bits from MSB to LSB are compared and provide the final result at the output.
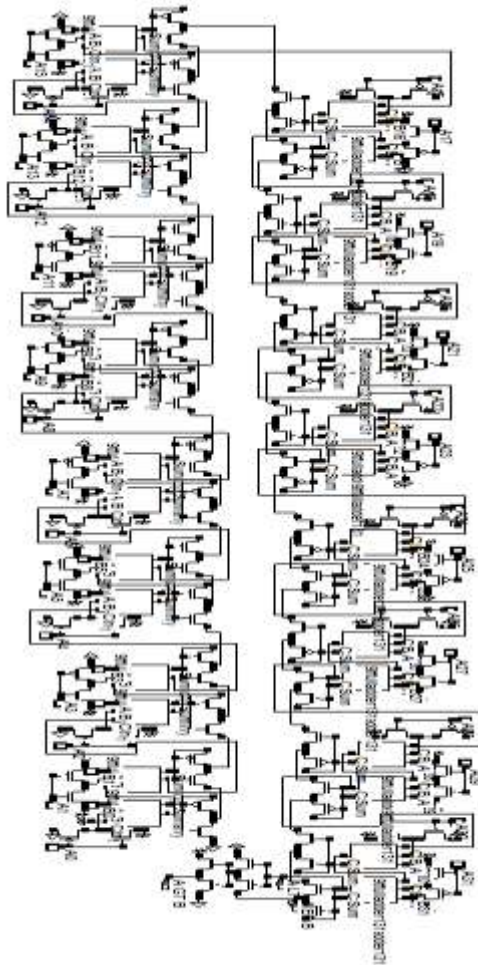

Fig. 8: Schematic of Proposed 32-bit comparator

V. LAYOUT ANALYSIS

As it is not easy to design the layout of any complex circuit manually, so automatic layout generation tool is an efficient method to build it. The proposed design of 32-bit comparator has been designed in DSCH3.1 and then its verilog file that is generated using DSCH is compiled in Microwind3.1 to generatethe layout [16]. After this the analog simulation has been done which is obtained at different voltage values in order to observe the effect different voltages on the power consumed by the circuit. with 27^0C temperature for Level-3

model.Table 2 shows the power consumption of various techniques based 32-bit comparator results for different supply voltages. It is also observed that power dissipation goes on increasing as the voltage increases. When we compare these three circuits in terms of transistor count, it is found that PTL design consume 564 transistors, GDI takes 596 and proposed design uses only 420 transistors which is very less in number as compare to other. So, it is also advantageous in terms of transistor count. Both the techniques have their own advantages [17].

Table 2 Comparison of Power for different voltages

Parameter	Power Dissipation (mW)		
Supply Voltage	PTL [9]	GDI [10]	Proposed
1V	0.233	0.113	0.076
1.2V	0.399	0.177	0.122
1.4V	0.615	0.269	0.213
1.6V	0.942	0.407	0.337
1.8V	1.396	0.597	0.519

Fig.9 shows the variation of power supply with respect to various voltage value of different techniques based comparator using LEVEL-3 model.
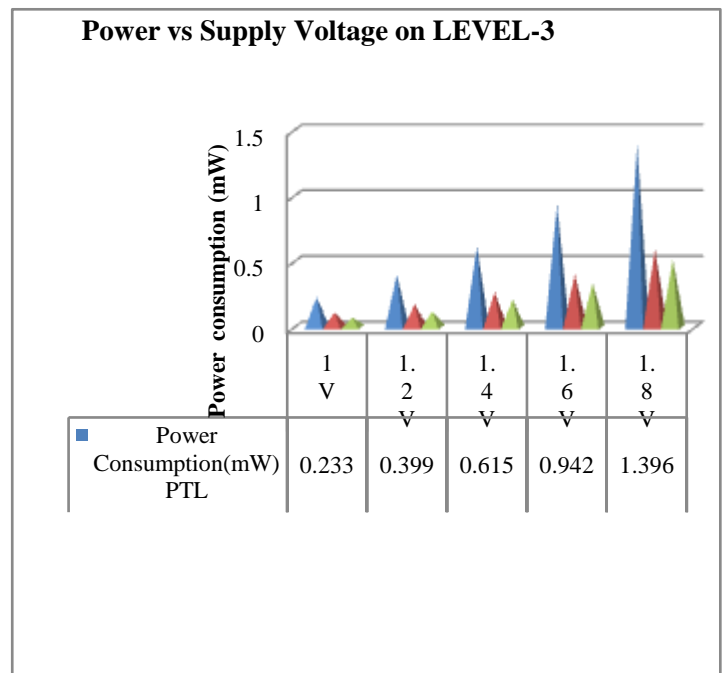

Fig. 9: Power vs Supply voltage plot

VI. CONCLUSION

By analyzing the simulation results of proposed design of 32-bit comparator that implanting the design using PTL and GDI logic techniques, the final results obtained in terms of transistor count and power of the device shows that both PTL and GDI logic helps in reducing the transistor count. As the GDI technique is low power technique also helps in reducing the power consumption caused by designing on a gate level. This improves the circuit performance. So, it provides area efficient and power efficient design integrating number of stages into one stage. The simulation results have been obtained which shows that proposed design have good performance at different voltages .

REFRENCES

[1] Suman Deb and S. Chaudhary, "High-Speed Comparator Architectures for Fast Binary   Comparison", *IEEE International Conference on Emerging Applications of Information Technology*, pp. 454-457, 2012.

[2] Anjuli and Satyajit Anand, "2-Bit Magnitude Comparator design using different logic styles," *International Journal of Engineering Science Invention*, Vol. 2, No. 1, pp.13-24, 2013.

[3] Anjali Sharma, Richa Singh, Rajesh Mehra, Member, IEEE, "Low Power TG Full Adder Design Using CMOS Nano Technology," *IEEE International Conference on Parallel, Distributed and Grid Computing*, pp. 210-213.

[4] Vijay Kumar Sharma, Manisha Pattanaik, *"VLSI Scaling methods and Low Power CMOS Buffer Circuit"*, *International Journal of Semiconductors*, Vol. 34, No. 9, pp. 1-8, 2013.

[5] Dinesh Sharma and Rajesh Mehra, "Low power Delay Optimized Buffer Design using 70nm CMOS Technology," *International Journal of Computer Applications*, Vol.22, No. 3, pp.13-18, 2011.

[6] P. Saini and R. Mehra, "A Novel Technique for Glitch and Leakage Power Reduction in CMOS VLSI Circuits*," International Journal of Advanced Computer Science and Application*, Vol.3, No.10, pp.161-168, 2012.

[7] Vandana Choudhary and Rajesh Mehra, "2-bit Comparator using Different Logic Style of Full Adder*," International Journal of Soft Computing and Engineering*, Vol. 3, No.2, pp.277-279, 2013.

[8] Manoj Kumar, Sandeep K. Arya1, and Sujata Pandey, " Single bit full adder design using 8 transistors with novel 3 transistors XNOR   gate", *International Journal of VLSI design & Communication Systems*, Vol. 2, No. 4, pp. 47-59, 2011.

[9] Meena Aggarwal, Rajesh Mehra, " Hybridized Power Efficient 32-bit Comparator using Less Transistor count", *International Journal of Advanced Research in Electronics and Communication Engineering*, Vol. 4, No. 7, pp. 2012-2018, 2015.

[10] Subodh Wairya, Himanshu Pandey, Rajendra Kumar Nagaria, Sudarshan Tiwari, "Ultra Low Voltage High Speed 1-bit CMOS Adder," *International Conference on Power Control And Embedded System*, Vol.3, No.2, pp. 221-242, 2010.

[11] Morgenshtein, A., Fish A., Wagner, I.A., "Gate- diffusion input (GDI): A Power Efficient Method for Digital Combinational circuits," *IEEE Transaction on Very Large Scale Integration (VLSI) Systems*, Vol. 10 , No. 5 , pp. 566 - 581 , 2002.

[12] Chiou-Kou Tung, Yu-Cherng Hung, Shao-Hui Shieh, Guo-Shing Huang, "A Low -Power High-speed Hybrid CMOS Full Adder For Embedded System," *IEEE Transaction on Design and Diagnostics of Electronic Circuits and Systems*, Vol.13, No.6, pp.1- 4, 2007.

[13] Po-Ming Lee, Chia-Hao Hsu, Yun-Hsiun Hung, "   Novel 10-T full adders realized by GDI structure*," Components, Circuits, Devices & Systems, Engineered Materials, Dielectrics & Plasmas*, pp. 115 - 118 , 2007.

[14] A. Morgenshtein, A. Fish., A. Wagner, "Gate- Diffusion Input (GDI)-A novel power efficient method for digital circuits: *A Design Methodology," IEEE International Conference*, pp. 39 – 43, 2001.

[15] Shahid Jaman, Nahian Chawdhury, Aasim Ullah, Muhammad Foyazur Raham, " A New High Speed-Low Power 12 Transistor Full Adder Design With GDI Technique*," International Journal of Science & Engineering Research*, Vol.3, No.7, 2012.

[16] Microwind and DSCH version 3.1, User's Manual, Copyright 1997-2007, *Microwind INSA France*.

[17] N.Weste and D.Harris, CMOS VLSI Design: *A Circuits and System Perspective, 3rd ed. Reading*, MA, USA: Addison-Wesley May 2004.