Various Reduction Techniques for Parallel FIR Digital Filter Using Parallel Architecture

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Abstract: *The FIR filter is a most widely used tools in digital signal processing and image processing applications. The aim is to design efficient Fast Finite-Impulse Response (FIR) Algorithms (FFAs) for parallel FIR filter structure with the constraint that the filter tap must be a multiple of 2. In our work we have briefly discussed for L = 4 parallel implementation. The parallel FIR filter structure based on proposed FFA technique has been implemented based on carry save and ripple carry adder for further optimization. The reduction in silicon area complexity is achieved by eliminating the bulky multiplier with an adder namely ripple carry and carry save adder. Overall the new parallel FIR structures can lead to significant hardware savings for symmetric convolutions from existing FFA parallel FIR filter especially when the length of the filter is large.*

Keywords: *Digital signal processing (DSP) , Fast Finite Impulse Response (FIR) Algorithm (FFA) , Parallel FIR filter; FFA structure.*

1. Introduction:

Along with time, the need for digital signal applications which have high speed and consumes less power is increasing. The finite impulse response (FIR) digital filter is a very basic tool that is usually used in most of the signal processing and image processing applications. Also the use of FIR filter helps to achieve a narrow transition band characteristics. Moreover the two techniques of parallel and pipelining processing available in DSP applications, can both be well utilized to reduce the power consumption . The parallel processing is a more convenient technique as it reduces the power consumption of FIR filter while increasing the throughput of the filter. The method of parallel processing helps to increase the rate of sampling by hardware replication and thus multiple inputs can be processed in parallel so that multiple outputs are generated at the same time. But with the increase in size of the parallel processing block, the cost as well as the complexity of the hardware goes on increasing. Hence the practical implementation of this filter is restricted. The Fast FIR algorithms (FFAs) makes use of sub filter blocks to implement a parallel FIR filter. The problem of area complexity is thus minimized by reducing the number of bulky multipliers when using the FFA technique. The FIR digital filter is one of the most widely used fundamental devices performed in DSP systems, ranging from wireless communications to video and image processing. Some applications need the FIR filter to operate at high frequencies such as video processing, whereas some other applications request high throughput with a low-power circuit such as multiple-input– multiple-output systems used in cellular wireless communication. Furthermore, when narrow transition band characteristics are required, the much higher order in the FIR filter is unavoidable. In this brief, parallel processing in the digital FIR filter will be discussed. Due to its linear increase in the hardware implementation cost brought by the increase in the block size L, the parallel processing technique loses its advantage to be employed in practice.

An efficient FFA filter structure that will save a large amount of hardware cost involved , especially when the length of the FIR filter is large enough can be obtained by the Iterated Short Convolution (ISC) based linear convolution structure. The longer convolutions are decomposed into several smaller convolutions which leads to significant saving in the cost and complexity of the hardware.

2. Fast FIR Algorithm (FFA)

Let us consider an N-tap FIR filter that can be expressed in the general form as

$Y(n) = \sum_{i=0}^{N-1} h(i)x(n-1),\ n=0,1,2,.....,\infty$ ……..(1)

where {x(n)} is an input sequence of infinite-length and {h(i)} are the length-N FIR filter coefficients. Then, the traditional L-parallel FIR filter can be derived using polyphase decomposition as

$$\sum_{p=0}^{L-1} Yp(z^L)z^{-p} = \sum_{p=0}^{L-1} Xp(z^L)z^{-p} \sum_{r=0}^{L-1} Hr(z^L)z^{-r}$$

...……(2)

Where Xq=

$$= \sum_{k=0}^{\left(\frac{N}{L}\right)-1} z^{-k}x(Lk+q), Hr = \sum_{k=0}^{\left(\frac{N}{L}\right)-1} z^{-k}x(Lk+r), Yp = \sum_{k=0}^{\infty} z^{-k}x(Lk+p),$$

for p , q , r =0,1,2.....L-1. The equation of FIR filter shows that the usual FIR filter requires sub filter blocks of length N/L to implement L_2 FIR filter.

2.1 The 2x2 FFA technique (L=2*parallel*)

According to equation (2), a two-parallel FIR filter can be expressed in the following form

Y0+Z-1Y1 = (H0+Z-1H1) (X0+Z-1X1)
=H0X0+Z-1(H0X1+H1X0)+Z-2H1X1
…….(3)

Implying that
Y0=H0X0+Z-2H1X1
Y1=H0X1+H1X0 …….. (4)

Equation (4) shows the traditional structure of a two-parallel filter, that requires four FIR sub filter blocks of length-N/2, two adders for post processing, and a total of 2N multipliers and (2N-2) adders. The equation (4) can also be expressed as

Y0=H0X0+Z-2H1X1
Y1= (H0+H1)(X0+X1)-H0X0-H1X1 ……..(5)

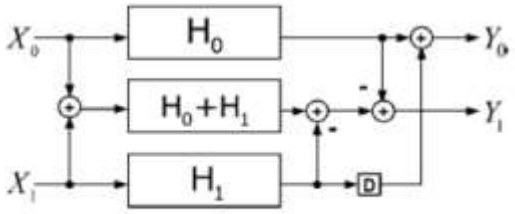

Fig. 1: Existing FFA for Two-parallel FIR filter implementation

2.2 The 3x3 FFA technique (L=3*parallel*)

A three-parallel FIR filter using FFA can be expressed in the same manner as that of two-parallel FIR filter.
Y0=H0X0-Z-3H2X2+Z-3x[(H1+H2)(X1+X2)-H1X1]

Y1 = [(H0+H1)(X0+X1)-H1X1]-(H0X0-Z-3H2X2)
Y2=[(H0+H1+H2)(X0+X1+X2)][(H0+H1)(X0+X1)-H1X1]- [(H1+H2)(X1+X2)-H1X1] …….. (6)

To implement equation 6,six length-N/3 FIR sub filter blocks, three preprocessing and seven post processing adders, and three N multipliers and 2N+4 adders are required. This method reduced the hardware cost over the traditional method.

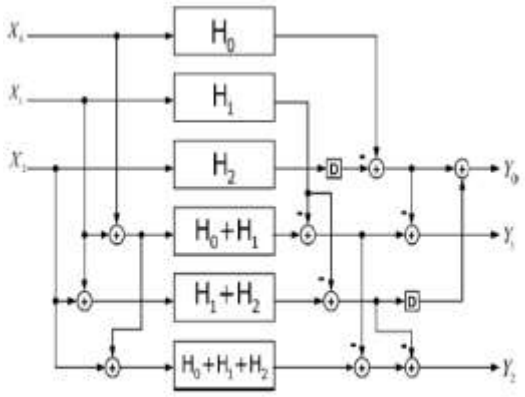

Fig. 2: Three-parallel FIR filter implementation using Existing FFA

3. FFA structures based on Symmetric convolutions

A two-parallel FIR filter can be expressed as follows
Y0 = {1/2[(H0+H1)(X0+X1)+(H0-H1)(X0-X1)]-H1X1}+Z-2H1X1,
Y1 = 1/2[(H0+H1)(X0+X1)-(H0-H1)(X0-X1)]
…….(7)

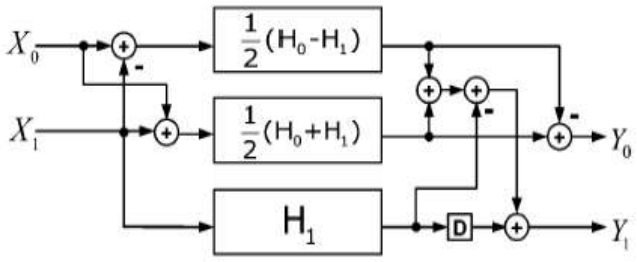

Fig. 3. Symmetric convolution based FFA two-parallel FIR filter

For even symmetric coefficients expressed in equation 7, there is an availability of one

more block of sub filter than equation 5.

3.1 FFA structures based on Symmetric convolutions for L=3

A three-parallel FIR filter as expressed in equation 6 can also be written as in equation9.

Y0= 1/2[(H0+H1)(X0+X1)+(H0-H1)(X0-X1)]-H1X1+
Z-3{(H2+H0+H1)+(X0+X1+X2)-(H0+H2)(X0+X2)-1/2[(H0+H1)(X0+X1)-((H0-H1)(X0-X1)]-H1X1}
Y1=1/2[(H0+H1)(X0+X1)-(H0-H1)(X0-X1)]+
Z-3{1/2[(H0+H2)(X0+X2)+(H0-H2)(X0-X2)]-1/2[(H0+H1)(X0+X1)+(H0-H1)(X0-X1)]+H1X1}
Y2=1/2[(H0+H2)(X0+X2)-(H0_H2)(X0-X2)]+H1X1
……...(9)

The Fig. 4 shows the implementation of proposed three-parallel FIR filter. If the symmetric coefficient N is a multiple of 3, then the three-parallel FIR filter structure given by equation 9 enables four blocks of sub filters with symmetric coefficients in the total, although the existing FFA parallel FIR filter has only two. Figure 5 shows shadow blocks stand for sub filter blocks consisting of symmetric coefficients. Hence the structure based on symmetric convolution saves N/3 multipliers as compared to the existing FFA structure. The three-parallel FIR structure brings as overhead, in preprocessing and post processing blocks, of additional seven adders.

4. Cascaded FFA structures based on Symmetric convolutions

The parallel FIR structure helps us to reuse the multipliers in sub blocks and it also adds to the adder cost in preprocessing and post processing blocks. When the cascaded FFA parallel FIR structure is implemented the number of adders goes on incrementing substantially. Hence instead of using the FFA FIR filter structure for all the sub filters in the process of decomposition, the FFA structures that provide less number of preprocessing and post-processing blocks are used for sub filters with no symmetric coefficients, whereas the FIR filter structures are used for all other sub filters. The length of the resulting final set of filter will be Nl.

The number of multipliers and the number of adders are necessary to be considered and kept track of. To calculate the number of required multipliers the equation 14 is used.

$$M = \frac{N \; r}{\Pi^{r}_{i=0} Li} \; \pi \; M_i \qquad \text{……(10)}$$

where r is the number of FFAs used, Li is the block size of FFA , Mi gives the number of filters that results from the application of i^{th} FFA filter and N is the order of filter. The adders required can also be calculated on the basis of a formulae as

$$A = A_1 \prod_{i=2}^{r} L_i + \sum_{i=2}^{r} [A_i (\prod_{j=i+1}^{r} L_j)(\prod_{k=1}^{i-1} M_k) + [\prod_{i=1}^{r} M_i][\frac{N}{\prod_{i-1}^{r} L_i} - 1], \qquad \text{……(11)}$$

Where Ai gives the number of adders.

If we consider an example of 2 FFAs arranged in cascaded form, the result which is a 4 parallel filter will require (N/4 -1) adders and 9N/4 multipliers. The 4 parallel filter thus implemented have a reduced hardware complexity of at least 45% as compared to traditional multipliers.

The four-parallel FIR filter (L=4) in cascading form is as shown in figure blow:

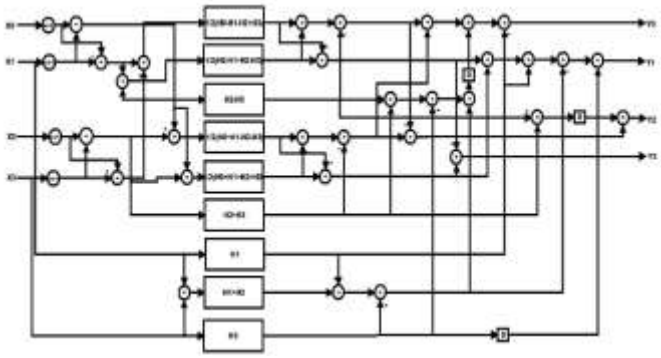

Fig. Four Parallel Proposed FFA Algorithm

5. Analysis of Hardware complexity and their comparison

When we compare an existing FFA structure and the proposed structure for symmetric even coefficients of different lengths the difference can be seen with respect to number of adders, multipliers and sub filter blocks.

(1) For L = 2 Parallel FIR Filter:

Length		24-tap	36-tap	81-tap	512-tap	1024-tap
Multipliers	Existing FFA	36	54	122	768	1536
	Proposed FFA	30	45	102	640	1305
	Reduced	6	9	20	128	231
Adders	Existing FFA	4	4	4	4	4
	Proposed FFA	6	6	6	6	6
	Increased	2	2	2	2	2
Sub-Filters Block Adders		33	51	118	765	1533

(2) For L = 3 Parallel FIR Filter:

Length		24-tap	36-tap	81-tap	512-tap	1024-tap
Multipliers	Existing FFA	48	72	162	1024	2048
	Proposed FFA	40	60	135	854	1707
	Reduced	8	12	27	170	341
Adders	Existing FFA	10	10	10	10	10
	Proposed FFA	17	17	17	17	17
	Increased	7	7	7	7	7
Sub-Filters Block Adders		42	66	156	507	2042

(3) For L = 4 Parallel FIR Filter:

Length		24-tap	36-tap	81-tap	512-tap	1024-tap
Multipliers	Existing FFA	54	81	182	1152	2304
	Proposed FFA	44	66	149	940	1880
	Reduced	10	15	33	212	42
Adders	Existing FFA	20	20	20	20	20
	Proposed FFA	31	31	31	31	31
	Increased	11	11	11	11	11
Sub-Filters Block Adders		45	72	173	1143	2295

(4) For L = 6 Parallel FIR Filter:

Length		24-tap	36-tap	81-tap	512-tap	1024-tap
Multipliers	Existing FFA	72	108	243	1536	3072
	Proposed FFA	60	90	203	1286	2566
	Reduced	12	18	40	253	506
Adders	Existing FFA	42	42	42	42	42
	Proposed FFA	74	74	74	74	74
	Increased	32	32	32	32	32
Sub-Filters Block Adders		5	4	90	225	1518

6. Conclusion:

Thus we can make an inference that the parallel filter structure proposed here proves to be advantageous for convolutions of symmetric type. For hardware implementation of parallel FIR filter. The new proposed FIR structure reduces the number of multipliers thus reducing the additional cost involved in utilizing additional pre-processing and post-processing adders.

7. References:

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