Novel 5 Level Cascaded H-Bridge Multilevel Inverter Topology

AbhishekThakur[1], RejoRoy[2], T.V.Dixit[3]
M. Tech Scholar[1], Assistant Professor[2], Assistant Professor[3]
Rungta College of Engineering, Bhilai, Chhattisgarh India[12]
Sarguja university, Ambkapur, Chhattisgarh India[3]

***Abstract*:-**This paper represents Novel 5 level cascade H-bridge multilevel inverter using only 6 switches and two DC power source. The main aim of this paper is to increase number of levels with Reduced Number of Switches and Sources at the output without adding any complication to the power circuit. The main aim of the novel topology is to decrease the lower whole harmonic distortion and high output voltage. In this paper pulse width modulation technique is used to implement this topology which can minimize the total harmonic distortion and enhances the output voltages. The hardware of multilevel Inverter circuits has been done using Proteus-7.8 software. An AVR (ATmega16) microcontroller is used to generate pulses for controlling the multilevel inverter circuit and result are show in DSO (digital Storage Oscilloscope).

Index Terms:-Cascaded H- bridge multilevel inverter, phase pulse width modulation, Proteus7.8/Simulink software, reduced switches and sources.

I. INTRODUCTION

Basically Inverter is a device that converts DC power to AC power at desired output voltage and frequency. Disadvantages of inverter are a reduced amount of efficiency, high cost, and high switching losses. To overcome these drawbacks, we are going to multilevel inverter. The period Multilevel began with the three-level converter. The model of multilevel converters has been introduced since 1975. [1].

Now a day, the multilevel inverters have expected much attention because of their major advantages such as high power quality; lower harmonic components, enhanced electromagnetic consistence, lower dv/dt, and switching losses reduce .There are three main types of multilevel inverters: diode clamp multilevel inverter, cascaded multilevel inverter, and flying capacitor multilevel inverter. The cascaded multilevel inverters have expected special devotion due to the modularity and smoothness of control. The cascaded multilevel inverters are fundamentally classified intotwo groups [9].:

- Symmetric, with equal magnitude for the dc voltage sources; and
- Asymmetric, with different values of the dc voltage sources.

A multilevel converter was offered in which the two separate DC sources were the secondaries of two transformers coupled to the utility AC power. In difference, in this paper, only one source is used without the usage of transformers. The importance here is interfacing a single DC power source with a cascade multilevel inverter where the other DC sources are capacitors. At present, every phase of a cascade multilevel inverter requirement N DC sources for 2N+1 level in applications that comprise real power transfer. In this work, a preparation is future that permits the use of a single DC power source (e.g., fuel cell stack, or battery) with the remaining N-1 DC sources being capacitors. It is shown that one can instantaneously sustain the DC voltage level of the capacitors and select a fundamental frequency switching configuration to create a almost sinusoidal output. The multilevel inverters also find applications in several areas viz. Medium voltage variable drives, static VAR compensation, harmonic filtering, and HVDC back-to-back inter-tie.[2].

II. MULTILEVEL INVERTER ARCHITECTURE

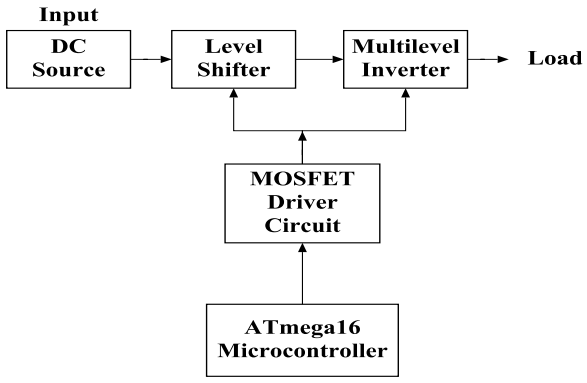

Fig 1:- Block diagram of Multilevel inverter

In these proposed work we design and implement the three and five level cascaded H-Bridge multilevel inverter. The real time proteous 7.8 and hardware result of single phase multilevel inverter circuits has been shown in below Fig no.1& 2. [5]:

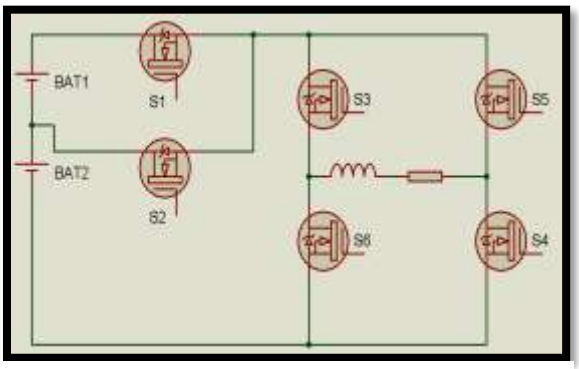

Fig 2:- Proteus Model of Single Phase 5-level Inverter

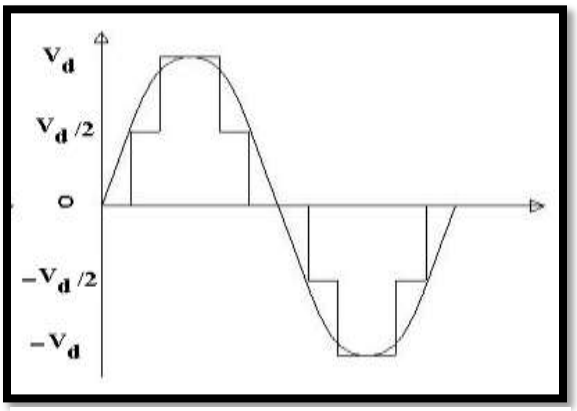

Fig 3:- Output Waveform of Five Level Multilevel Inverter

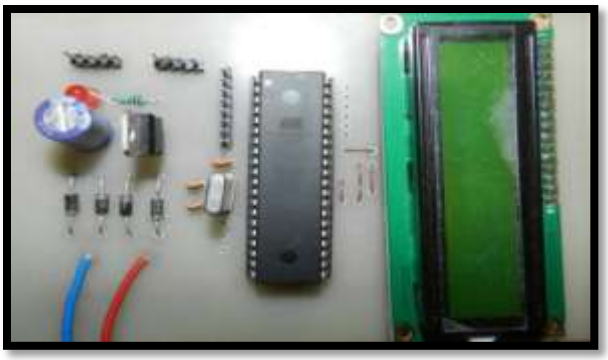

Fig 4:- Firing Control Card Circuit

1:- ATmega16 Microcontroller

The ATmega16 is a low-power CMOS 8-bit microcontroller based on the AVR improved RISC architecture. By implementing powerful instructions in a single clock cycle, the ATmega16 accomplishes throughputs future 1 MIPS per MHz permitting the system designed to improve power consumption versus processing speed.

2:- Firing control card

This circuit is Firing control card , driver circuit is dirve a MOSFET through this card. firing control card send a pulse to the MOSFET driver and This Driver send High –Low voltge pulse to the MOSFET Gate terminal and also check a signal form voltage sensor and current sensor.

3:- MOSFET Driver circuit

The purpose of a low cost drive circuit is to switch a power semiconductor device from 'OFF'-state to the 'ON'-state and vice versa. To reduce instantaneous power dissipation during switching, the turn-on and turn-o must be minimized. So, that power device spends little time in the active region. In the on-state the drive circuit must provide adequate drive power (gate source voltage in case of MOSFET) to keep the power switch in the on state where the conduction losses are low. The drive circuit is needs to provide reverse bias to the gate to minimize turn o times and to ensure that the device remains in the o state and is not triggered on by stray transient signals generated by the switching of other power devices. The features of properly designed gate-driver circuits are as follows [6]:

- It interfaces between the control circuit and the power switch.
- It amplifies the control signals to the levels required to drive the power switch.
- It also provides electrical isolation between power and control circuits.
- The gate drive circuit required to provide protection to the power device from over-current or short circuit conditions.

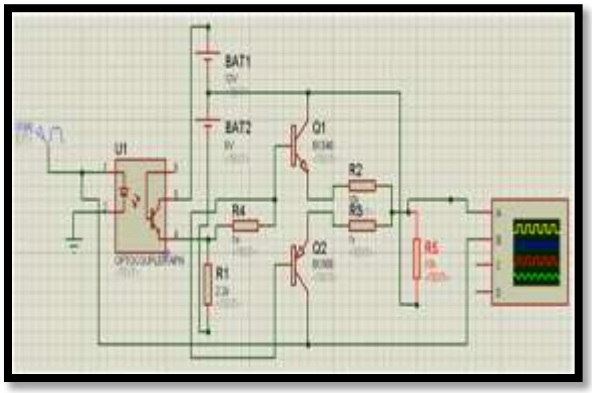

Fig5:- Driver circuit of power MOSFET device

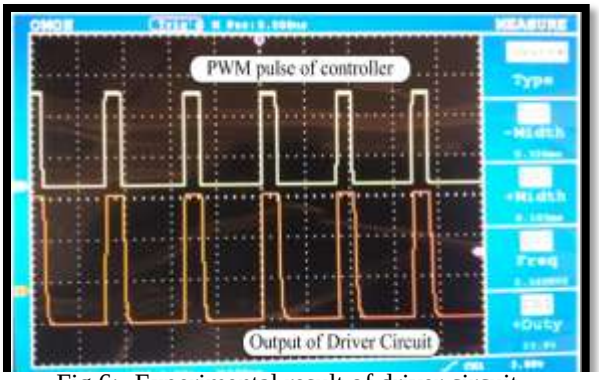

Fig 6:- Experimental result of driver circuit

III. CASCADED MULTILEVEL INVERTER TOPOLOGY

A cascaded multilevel inverter prepared up of from series connected single phase full bridge inverter, each with their individual isolated dc bus. This multilevel inverter can producenearly sinusoidal waveform voltage from several separate dc sources, which may be acquired from solar cells, ultra capacitors, fuel cells,batteries, etc. Thisvariety of converter does not requirement any transformer or flying capacitors or clamping diodes [5].Each level can producefive different voltage outputs $+V_{dc}$, $+V_{dc}/2$, 0 - $V_{dc}/2$ and $-v_{dc}$ by connecting the dc sources to the ac output side by different combinations of the four switches.

TABLE NO. 1:- Switching State of Five Level Cascade H-Bridge Multilevel Inverter Inverter.

Output Voltage	S1	S2	S3	S4	S5	S6
V_{dc}	1	0	1	1	0	0
$V_{dc}/2$	0	1	1	1	0	0
0	0	0	0	0	0	0
- $V_{dc}/2$	0	1	0	0	1	1
V_{dc}	1	0	0	0	1	1

By closing the proper switches, each H-bridge inverter can produce five different voltages:

- When a switch S_1, S_3 and S_4 H-bridge inverter are closed, the output voltage is $+V_{dc}$.
- When a switch S_2, S_3 and S_4 are closed, the output voltage is $+V_{dc}/2$.
- When all switches are closed, the output voltage is 0.
- When a switch S_2, S_5 and S_6 are closed, the output voltage is $-V_{dc}/2$.
- When a switch S_1, S_5 and S_6 of one particular H-bridge inverter are closed, the output voltage is -Vdc.

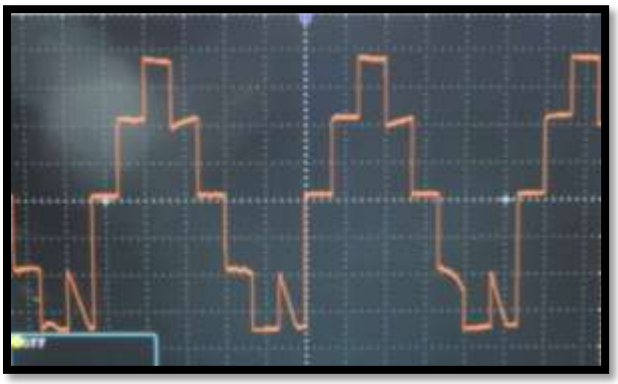
Fig 7:- Experimental result of Five level inverter output

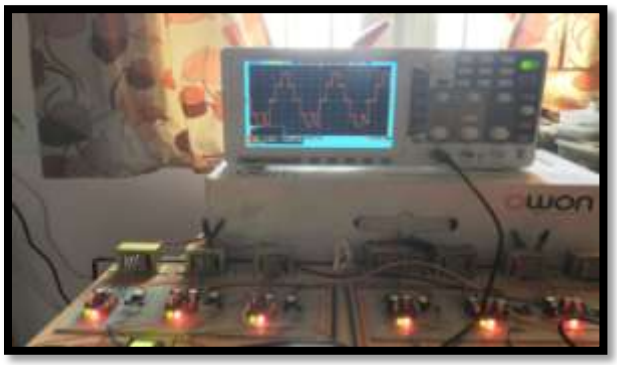
Fig 8:- Experimental Setup to multilevel Inverter

IV. CONCLUSION

Prototype of the 5-level involves of a single phase H-bridge multilevel inverters that it uses isolated dc power sources. pulse width modulation modulated technique are used to to control signal for power electronics switches.Increase level of the Inverter using this technique. The modified PID algorithm can be incorporated to improve the performance of this system. In this paper hardware prototype model results are associated.

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