Low Power Layout Design of Priority Encoder Using 65nm Technology

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Abstract— **this paper provides comparative performance analysis of power and area of 4 bit priority encoder using 65nm technology. Two priority encoder approaches are presented, one with semi custom and the other with full custom. The main objective is to compare semi custom and full custom designed layout on the basis of two parameters which is power and area. Both the semi custom circuit simulation and full custom has been done by manually layout created. Creation of layout in both types of method is done at 65nm CMOS technology. The simulation results show that priority encoder using full custom design has improved power efficiency by 0.86 µW and effective area by 12.40 µm^2.**

Keywords— **Priority Encoder, Low power, CMOS, 65nm.**

I. INTRODUCTION

Nowadays, priority encoder has been widely utilized in high-performance critical applications which persistently impose special design constraints in terms of high-frequency, low power consumption, and minimal area [1]. In the growth of the integrated circuit towards large integration density with high operating frequency the concern issues are power, delay and smaller silicon area with higher speed [2].The tremendous growth in portable electronics systems, the designers prime research are in low power nano-electronics technology to achieve a good-drivability, noise-robustness and low-energy operations for deep-sub micrometer and to extend the battery life of the system [3]. As VLSI technology enters nanometre regime, placement has become a critical step in VLSI design flow. The two major causes are both related to the increasing dominance of interconnect in nanometre-scale VLSI technologies [4]. Priority encoders are used in a number of computer systems as well as other applications. When several process, modules, or unit's request a single hardware (or software) resource, a decision has to be made to allow a single request to use such a resource. The priority encoder implements a fixed selection function where the resource is granted to the request with the highest priority [5]. The development of digital integrated circuits is challenged by higher power consumption [6]. As the computer systems become more compact the area of the PE becomes a key parameter in the design of the system. And at the same time, the overwhelming demand for portable electronics encourages the development of a power optimized PE structure [7]. This paper discusses comparison between 4 bit priority encoder design between Semi custom layout using static CMOS logic and full-custom layout using static CMOS logic at 65nm

technology. Industrial 65nm processes have been introduced by Toshiba in 2002, Fujitsu, NEC and STMicroelectronics in 2003 and by Intel in 2004. With transistor channels ranging from 30nm to 50nm in size (30 to 50 billionth of a meter), comparable to smallest microorganisms this technology is truly nanotechnology [8]. Here Microwind3 is used to draw the layout of the CMOS circuit [9]. In digital electronic an encoder is the logic device that converts 2N input signals to N-bit coded outputs. The output of a priority encoder is the binary representation of the ordinal number starting from zero of the most significant input bit. If two or more inputs are given at the same time, the input having the highest priority will take precedence.

II. PRIORITY ENCODER DESIGN

This 4 bit priority encoder circuit is designed to control interrupt requests by acting on highest priority request with output produced by the desired bit. The truth table of priority encoder is given in Table1. The X are don't care condition that designate the fact that the binary values represent either 0 or 1.Input D3 has highest priority, so regardless of the value of other inputs, when the input is 1, the output Y1, Y2 is 11. D2 has the priority level. The output is 10 if D2 =1 and D3 = 0, irrespective of the values of the other two lower priority inputs, the outputs for D3 is generated only if higher priority inputs are 0, and so on down the priority level. A valid output indicator V is set to 1 only when one or more of the inputs are equal to 1. If all the inputs are equal to 0, V is equal to 0, and the other two outputs (Y1 and Y0) of the circuit are not used [10].

TABLE I
TRUTH TABLE FOR PRIORITY ENCODER

Truth Table for 4 bit Priority Encoder						
Inputs				Outputs		
D0	D1	D2	D3	Y1	Y0	V
0	0	0	0	X	X	0
1	0	0	1	0	0	1
X	1	0	0	0	1	1
X	X	1	0	1	0	1
X	X	X	1	1	1	1

Fig.1.Shows the logic diagram of 4 bit priority encoder which consists two 2 input OR gates, one 4 inputs OR gate, one 2 input AND gate and one inverter.
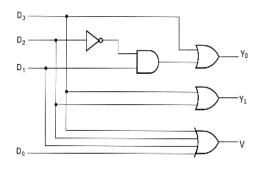

Fig. 1 Logic level priority encoder

Now replacing the basic logic gates used in above logic level diagram by their static CMOS logic using DSCH represented in fig. 2. The DSCH program is a logic editor and simulator. DSCH is used to validate the architecture of logic circuit before microelectronics design is started [11]. Fig. 2 shows the CMOS implemented 4 bit priority encoder on DSCH3.CMOS semiconductors have both PMOS and NMOS transistors and only one of them is on at any instant of time
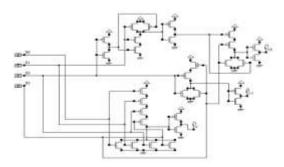

Fig. 2 CMOS equivalent on DSCH3

Fig.3.shows the output simulation of CMOS equivalent of 4 bit priority encoder on DSCH.
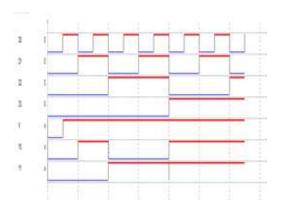

Fig.3 Simulation result of equivalent CMOS logic

The DSCH program is a logic editor and simulation. It provides user-friendly and fast simulation [12].

III. PRIORITY ENCODER LAYOUT SIMULATION

This section consist two design layout simulation mainly semi custom layout and full custom layout. Semi custom layout has been developed on Microwind3.1. It gives an idea about interconnections between two different metal layers polysilicon layer and metal layers got connected. It also gives an idea about lambda rule to design our desired logic circuit. Fig 4 Shows the Semi custom layout generated on Microwind3.1 of 4 bit priority encoder when we use static CMOS logic gates. So this is the gate level implementation of our desired logic level circuit.
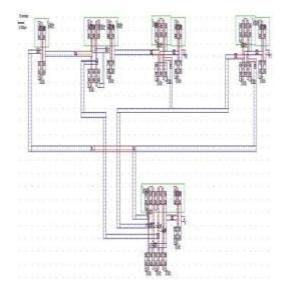

Fig.4 Semi custom layout using static CMOS logic
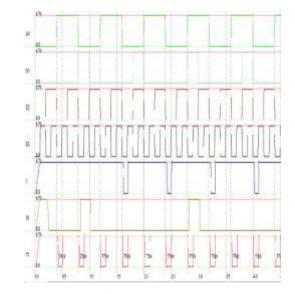
The simulation result is shown in fig 5

Fig. 5 Simulation result of Semi custom layout

Fig.6. shows the full custom design layout using static CMOS logic using Microwind3.1 on 65nm technology.

Fig. 6 Full-Custom layout using static CMOS logic

Fig. 7.Shows the simulation result of full-custom layout

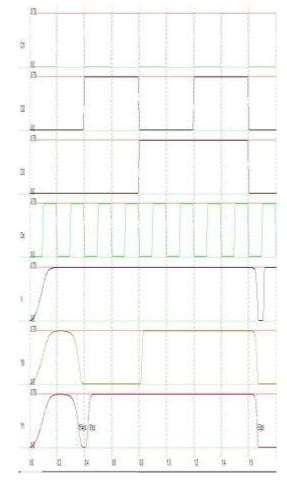Fig.7.Simulation result of full-custom layout

IV. RESULT ANALYSIS

Comparative analysis between semi custom layout and full custom design layout of 4 bit priority encoder is shown in table.2. Comparison is based on the factor responsible for factors affecting performance of priority encoder are power dissipation and surface area used. Comparison shows that full-custom design based 4 bit priority encoder is better than semi custom layout in terms of power consumption and efficient area. This improvement is done because of flexibility of placement and routing in full custom design than semi custom. Both design techniques are used foundry 65nm technology

TABLE II
COMPARATIVE PERFORMANCE ANALYSIS

Parameters	Semi Custom Layout Design	Full Custom Design
Power (µW)	5.56	4.69
Area (µm²)	95.6	83.2

Fig 8 and fig 9 represents the comparison on Column chart for power and area respectively.
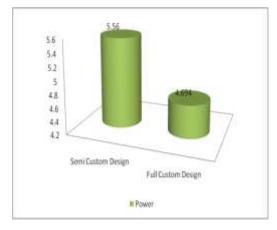

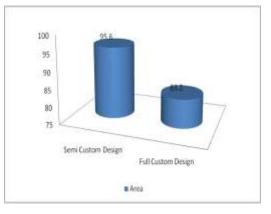Fig.8 Power Graph for semi custom and full custom design (unit in µW)

Fig.8 Area Graph for semi custom and full custom design (unit in µm²)

V. CONCLUSIONS

From the above analysis it can be concluded that full custom is more useful technique to reduce power consumption and surface area. Thus as shown in table II power consumption is reduced by 15.57% and area is reduced by 12.97% for full custom.

In the future work full custom design for priority encoder for more number of bits by using techniques like domino CMOS logic can be design.   .

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