

Performance Enhancement of VLSI Circuits using CNTFETs

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Abstract— In the world of integrated circuits, CMOS has lost its credential during scaling beyond 32nm. The main drawbacks of using CMOS transistors are high power consumption and high leakage current. Scaling causes severe Short Channel Effects (SCE) which are difficult to suppress. As technology is scaled down, the importance of leakage current and power analysis for VLSI design is increasing since short-channel effects cause an exponential increase in the leakage current and power dissipation. CNT-FET technologies mitigate these limitations by providing a stronger control over a thin silicon body. Enormous progress has been made to scale transistors to even smaller dimensions to obtain switching transistors that are fast and reduce the overall power consumption. However although the device characteristics are improved the problem of high active leakage still remain a problem. CNT-FET has become the most promising substitute to bulk CMOS technology because of reducing short channel effect and the similarity of the fabrication steps to the existing standard CMOS technology. CNT-FET device has a higher controllability, resulting relatively high *I_{on}/I_{off}* ratio. CNT-FET devices can be used to increase the performance by reducing the leakage current and power dissipation. The research work has, characteristics of CNT-FET, inverter & basic gates like NAND Gate, and are modelled in HSPICE software using CMOS structures and CNT-FET structure are analysed and their performances like power consumption and speed are compared. The values for Sub-Threshold slope of CNT-FET and MOSFETs are calculated

Keywords— Short channel effects, CNTFET.

I. INTRODUCTION

Silicon-based integrated circuit technology is approaching its physical limit as the device dimensions scale to the nanometer regime [1]. In the post silicon era, carbon nanotube field effect transistor (CNTFET) is a promising candidate for future integrated circuits because of its excellent properties like near ballistic transport [2], high carrier mobility (10^3 – 10^4 cm²/V.s) in semiconducting carbon nanotube (CNTs) [3, 4], and easy integration of high-k dielectric material resulting in better gate electrostatics. CNTs are basically hollow cylinders of rolled-up graphene sheet composed of one or more concentric layers of carbon atoms in a honeycomb lattice arrangement. Depending on the direction in which the nanotubes are rolled (chirality), they can be either metallic or semiconducting [5]. In a nanotube, low bias transport can be nearly ballistic across distances of several hundred nanometer and it is attractive for nanoelectronic applications due to its excellent electrical properties. The carbon nanotube field-effect transistor thus

already achieved widespread attention as possible alternative to nanoscale MOS transistor. Due to the similar *I-V* characteristics of CNTFET as that of MOS devices, qualitatively most of the CMOS circuit can be implemented using CNTFET [6-7]. Carbon Nano Tube field-effect transistors (FETs) overcome these problems because of tighter control of the channel potential by using gate-all-around CNTFETs, gates wrapped around the body. Amongst FETs, CNTFETs have emerged as the best candidate structures from a fabrication perspective. In this work we used the compact HSPICE compatible model for CNTFET using Verilog of Stanford Model. The VLSI circuits like Inverter and NAND Gate, logic levels are represented in terms of voltage value for computation. The work emphasis on *I-V* characteristics of CNTFET. The CNTFET model is implemented in Verilog and simulated in Hspice for the circuit simulation of inverter and NAND Gate and the performances are evaluated. The simulation results show excellent performance on power and speed of operation.

II. V-I CHARACTERISTICS OF CNTFET

The circuit compatible model of CNTFET has been successfully implemented in Verilog. At first the n-type and p-type CNTFETs are modelled and simulated in SPICE. The series of *I-V* characteristics of both types of CNTFET (Figure. 2 & 3 (a) & (b)) are obtained for 1.2 nm diameter CNT with $R_{SD} = 3.3k\Omega$ at room temperature (298K). In order to demonstrate the versatility of this model, we employed it to design basic logic gates. This CNTFETs behaviour is very similar to the conventional MOSFET. The p-type characteristics are obtained when the polarity-gate voltage is set to -0.2V and the n-type characteristics are obtained when the polarity-gate voltage is set to +0.2V. These CNTFETs are used to design circuits replacing the traditional MOS transistors. To perform the simulation of these circuits we arbitrarily decided to use 900 mV power supply and supposed that the flatband voltages are equal to +450 mV and -450 mV for n-type and p-type CNTFETs. The n-type and p-type characteristics curves shown in Figure.2 & 3 validate the developed model in Verilog.

III. TYPES OF CNTFET

Carbon Nanotube FETs (CNTFETs): The Carbon nanotube field effect transistor (CNTFET) is one of the most promising

candidates for next generation electronics and sensors. The first carbon nanotube field-effect transistors were reported in 1998. These were simple devices fabricated by depositing singlewall CNTs (synthesized by laser ablation) from solution onto oxidized Si wafers which had been treated with gold or platinum electrodes. The electrodes served as source and drain, connected via the nanotube channel, and the doped Si substrate served as the gate [8]. CNTFET so far can be classified into: Back-gated CNTFET's, Top-gated CNTFET's, Wraparound gate CNTFET's, Suspended CNTFET's, Multi-Wall CNTFET, and Vertical CNTFET. One device fabricated with CNTs that has been highly examined is the carbon nanotube field effect transistor (CNTFET), comprised of single-wall CNTs (SWCNTs) as the active element between two metal source and drain contacts. Even though there are many advantages to the CNTFET, such as size, high sub-threshold slope, and low power consumption. There are two main methods for CNT creation: CVD Growth & CNT Solution Deposition [9].

Single-Wall CNTFETs There are a few types of architecture of Single-wall Carbon Nanotube FET - (SWNTFET): Back-gated CNTFET's, Top-gated CNTFET's, Wrap-around gate CNTFET's, Suspended CNTFET's, Vertical CNTFET, Local-gated single-walled CNTFET. Single device architecture cannot be suitable for all applications. Hereinafter is an overview of single-wall nanotube devices depending on their architecture.

Multi-Wall CNTFET: The multiwall carbon nanotubes structure is complex. So they are not studied in detail. Each multiwall carbon nanotube can be metal or semiconductor with different chirality [8]

IV. CNTFET MATERIAL CONSIDERATIONS

There are general decisions one must make when considering what materials to use when fabricating a CNTFET. Semiconducting single-walled carbon nanotubes are preferred over metallic single-walled and metallic multi-walled tubes since they are able to be fully switched off, at least for low source/drain biases. A lot of work has been put into finding a suitable contact material for semiconducting CNTs; the best material used is Palladium. This is because the work function of Palladium matches closely with that of nanotubes and it remains to the CNTs very well.[12]

V. PROJECT IMPLEMENTED BY USING WRAP-AROUND GATE CNTFETs:

Wrap-around gate CNTFETs as shown in figure.1(f), also known as gate-all-around CNTFETs were developed [10] and are a further improvement upon the top-gate device geometry. In this device, instead of gating just the part of the CNT that is closer to the metal gate contact, the entire circumference of the nanotube is gated. This should ideally improve the electrical performance of the CNTFET, reducing leakage current and improving the device on/off ratio.

Device fabrication begins by first wrapping CNTs in a gate dielectric and gate contact via atomic layer deposition.[11]. These wrapped nanotubes are then solution-deposited on an substrate that is insulating, where the

wrappings are etched off partially, thus exposing the ends of the nanotube. The contacts (Source, Drain and Gate) are then deposited onto the ends of the CNT and the metallic outer gate wrapping.

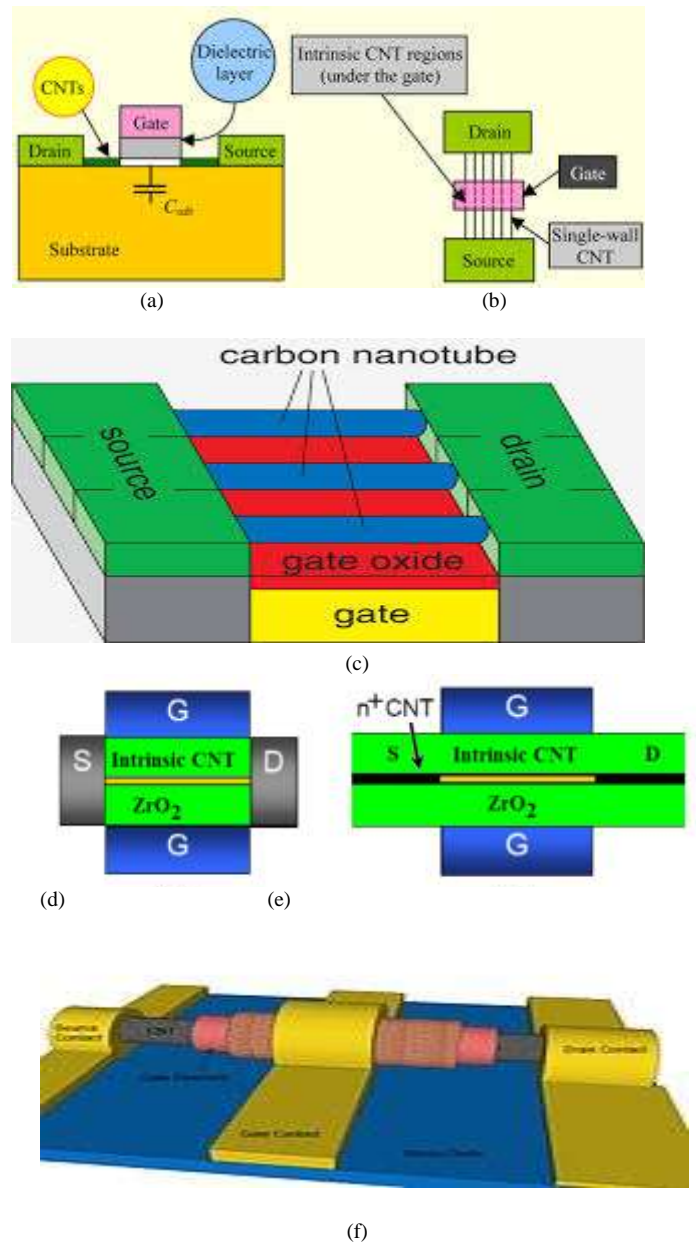


Figure.1. Schematic of a CNTFET structures

VI. COMPARISON TO MOSFETS

CNTFETs show different characteristics compared to MOSFETs in terms of overall performance. The p-CNTFET in a planar gate structure produces ~1500 A/m of the on-current per unit width at a gate overdrive of 0.6 V while p-MOSFET produces ~500 A/m at the same gate voltage[14]. This on-current advantage comes from the high gate capacitance and enhanced channel transport. As the

effective gate capacitance of CNTFET (per unit width) is about double compared to that of the p-MOSFET. It's compatibility with high- k gate dielectrics is a distinct advantage for CNTFETs[13]. About twice higher carrier velocity of CNTFETs than MOSFETs comes from the increased mobility and its band structure. In addition to this CNTFETs have about four times higher transconductance.

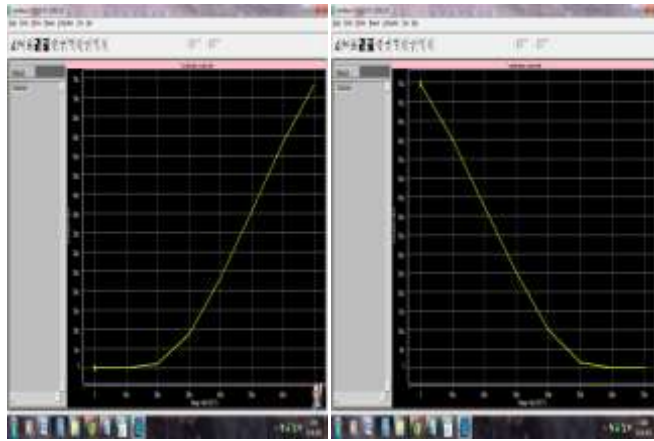


Figure.2. Transfer characteristics of CNTFET:a) N type b) P type

In spite of his double gate structure, the CNTFET is closed to its root, the conventional MOSFET in layout and fabrication. The Wrap-All Around gate Stanford CNTFET model used for simulation purpose & its specification is as follows[15]: Model files are for a Wrap-All Around gate CNTFET device with

1. Gate length= $L_g = 10e-9$ from (0:inf)
2. Contact length= $L_c = 11e-9$ from (0:inf)
3. Source/drain extension length= $L_{ext} = 3e-9$ from (0:inf)
4. Device width= $W = 1000e-9$ from (0:inf)
5. Gate height= $H_g = 15e-9$ from (0:inf)
6. Gate oxide thickness= $t_{ox} = 3e-9$ from (0:inf)
7. Gate oxide dielectric constant= $k_{ox} = 23$ from [1:inf)
8. Dielectric constant of the channel material= $k_{ch} = 1$ from [1:inf)
9. Dielectric constant of the spacer= $k_{spa} = 3.9$ from [1:inf)
10. Dielectric constant of the substrate= $k_{sub} = 3.9$ from [1:inf)
11. CNT diameter= $d = 1.2e-9$ from (0:inf)
12. CNT spacing= $s = 1000e-9$ from (0:inf)
13. Fermi level to the band edge at source/drain (eV)= $E_{fsd} = 0.258$ from (-0.2:0.5)
14. Flat band voltage= $V_{fb} = 0$;
15. Device structure= $Geomod = 1$ from [1:3]1:gate-all-around; 2:top-gate w/ screening; 3: top-gate w/o screening
16. $R_{cmod} = 0$ from [0:2]; // 0: user-defined series resistance, R_{s0} ; 1: d-dependent R_c ; 2: d-independent contact resistance

17. $R_{s0} = 3.3e3$ from [0: inf); // user-defined series resistance (Ohm). Activated only when $R_{cmod} = 0$.
18. $SDTmod = 1$ from [0:2]; // 0: SDT off; 1: SDT on; 2: SDT w/o inter-band tunnelling
19. $BTBTmod = 1$ from [0:1]; // 0: BTBT off; 1: BTBT on

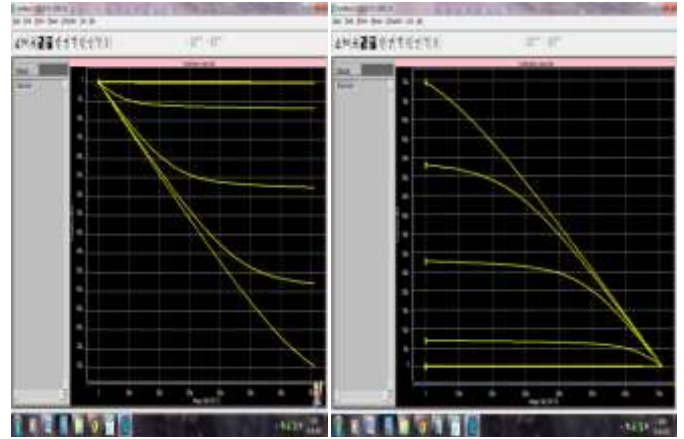


Figure.3 Output characteristics of CNTFET:a) N type b) P type

Figure.2 Tell us there is no current flowing up to threshold voltage but after this voltage current start over drain current increasing. This is ideal condition. In practical situation current flow before threshold voltage reaching.

Figure.3. Indicate increasing drain current with increasing drain voltage this condition is true up to pinch off voltage then there is no effect of drain voltage.

VII. SUB-THRESHOLD SLOPE

In MOSFET model, it was assumed that current only flows through the MOSFET channel when $V_{GS} > V_{TH}$. In reality, current flows even when V_{GS} is below the threshold voltage, V_T however it is weaker than currents lying in strong inversion. Inversion layer which is observed in strong inversion is barely seen here, and this can also be identified as weak inversion. Under weak inversion, the relation between current and gate-source voltage becomes exponential. S is defined to be the inverse slope of the $\log(I_D)$ vs. V_{GS} characteristic in the sub threshold region. The subthreshold slope S is an important parameter for switches because it defines how much is the ratio between the on and off currents. In order to get high on/off current ratios, we would like to have low subthreshold slopes so that the same difference in V_{GS} can decrease the drain current by more decades. For $V_T \sim 26$ mV (room temperature) and the ideal case of $n=1$, the ideal subthreshold slope for MOSFETs is ~ 60 mV/decade. on the other hand, the practicable slopes are around 70~80 mV/decade. Furthermore, as temperature increases, so does V_T and the subthreshold slope. If you plot $\log(I_{ds})$ against V_{gs} at a constant V_{ds} voltage, for $V_{gs} < V_{th}$ region the line would be somewhat linear. The slope of this line is also identified as

the subthreshold slope. It represents the rate at which the value of I_{ds} ramps up for an increase in the value of V_{gs} . Steep slope also means that the device gets away from the subthreshold region faster or in other words has lower V_{th} and therefore conduct better. It is usually given as $kT/q \cdot \log(1 + C_d/C_i)$. Where C_d is the depletion layer capacitance and C_i is the gate oxide capacitance. Note that $S \geq 60$ mV/dec at room temperature. Typical value is 70mV/decade. Different processes have different slopes. We have found the subthreshold slope of CNTFET which is mentioned below.

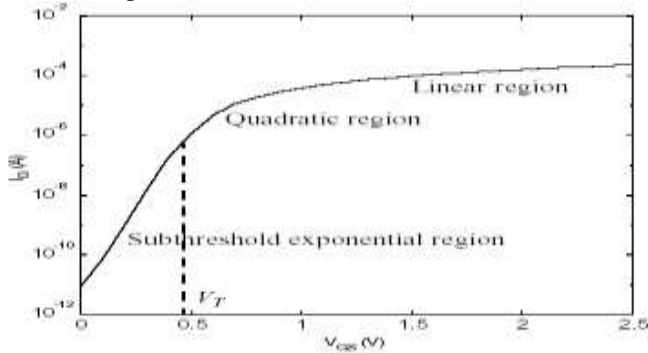


Figure.4: Sub-Threshold Characteristics

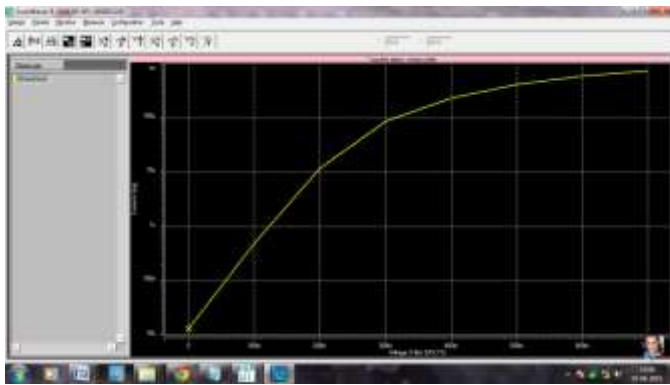


Figure.5: Subthreshold slope of CNTFET in Hspice

The calculated subthreshold slope of CNTFET using Hspice is 77mV/decade and that CMOS model is 122mV/decade.

VIII. INVERTER USING CNTFET & CMOS:

Below are the figures of CMOS inverter & Inverter using CNTFET Wrap-All Around gate type.

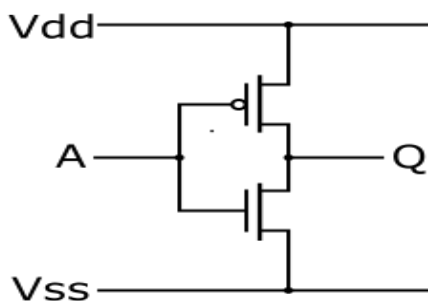


Figure.6.Static CMOS inverter

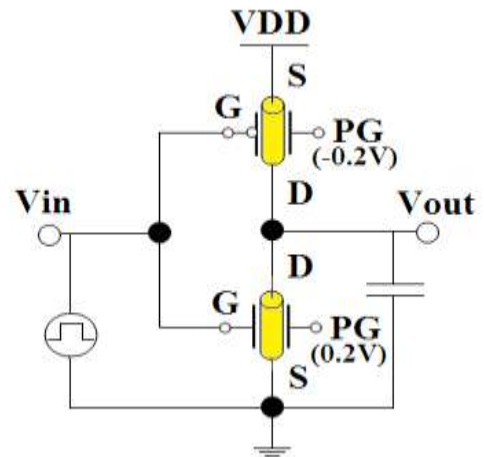


Figure.7. Inverter using CNTFETs

CMOS inverters (Complementary MOSFET Inverters) are some of the most widely used and adaptable MOSFET inverters used in chip design. They operate with very little power loss and at relatively high speed. Else furthermore, the CMOS inverter has good logic buffer characteristics, in that, its noise margins in both low and high states are large. A CMOS inverter contains a PMOS and a NMOS transistor connected at the drain and gate terminals, a supply voltage VDD at the source terminal, and a ground at the NMOS source terminal, where as VIN is connected to the gate terminals and VOUT is connected to the drain terminals.(See figure 6). It is important to notice that the CMOS does not contain any resistors, this makes it more efficient in terms of power consumption than a regular resistor-MOSFET inverter. As the voltage at the input of the CMOS device varies in the range 0 and 5 volts, the state of the NMOS and PMOS transistors varies accordingly. If we model each transistor as a simple switch which gets activated by the voltage at VIN, the inverter's operations can be deciphered very easily: The CMOS inverter is an important circuit device that provides quick transition time, high buffer margins, and low power dissipation: all three of these are desired qualities in inverters for most circuit design. It is quite clear why this inverter has become as popular as it is. Figure.7. illustrates the structure of an Inverter using CNTFETs. The inverters performance in terms of average power dissipation and speed (less time delay) is somewhat better as compared to the CMOS inverter.

IX. LOGIC GATES:

A logic gate is an elementary building block of a digital circuit. Most logic gates have two inputs and one output. At any given moment, every terminal is in one of the two binary conditions *low* (0) or *high* (1), represented by different voltage levels. The logic state of a terminal can, and generally does, change often, as the circuit processes data. In most logic gates, the low state is approximately zero volts (0 V), while the high state is approximately five volts positive (+5 V). There are seven basic logic gates: AND, OR, XOR, NOT, NAND, NOR, and XNOR.[16][17].

NAND GATE USING CNTFETs:

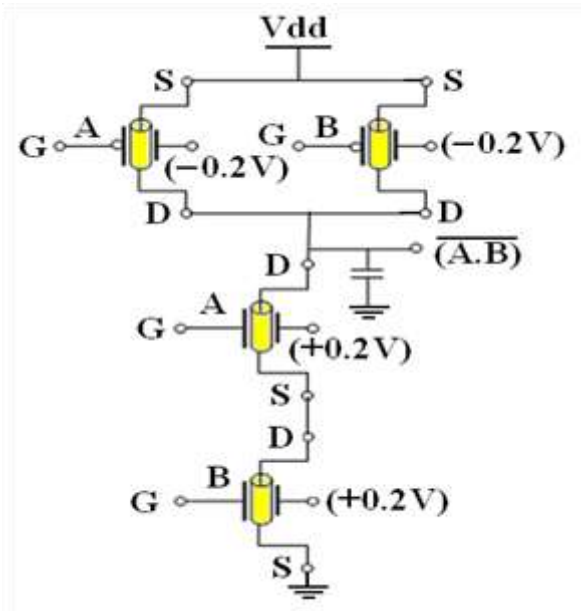


Figure.8. NAND Gate using CNTFETs



Figure.9. NAND Gate symbol

TABLE 1: TRUTH TABLE OF NAND GATE

Input A	Input B	Output Q
0	0	1
0	1	1
1	0	1
1	1	0

NAND Gate: The NAND Gate represents the complement of the AND operation. The symbol for the NAND gate consists of an AND symbol with a bubble on the output, denoting that a complement operation is performed on the output of the AND gate. The truth table and the graphic symbol of NAND gate is shown in the figure above. [16][17]

Universal Gates: NAND and NOR Gates are called Universal Gates because all the other gates can be created by using these gates. A universal gate is a gate which can implement any Boolean function without need to use any other gate type. The NAND and NOR gates are universal gates. In practice, this is advantageous since NAND and NOR gates are economical and easier to fabricate and are the basic gates used in all

ICdigital logic families. In fact, an AND gate is typically implemented as a NAND gate followed by an inverter not the other way around. Likewise, an OR gate is typically implemented as a NOR gate followed by an inverter not the other way around.[16][17].

Below are the simulated waveform results for Inverter and NAND Gate using CNTFETs (Figure.10 & Figure.11).The first simulated results are for Inverter using CNTFET .First waveform of it is signal input & second waveform is signal output signal. Third waveform is of power dissipation. The second simulated results are the waveforms for a NAND Gate using CNTFET. The first waveform is input signal A and second is input signal B. Third waveform is the output signal. Fourth waveform is of Power Dissipation. The waveforms below in figure.10 are shown for Inverter using CNTFET. The table no.2.below shows comparison of performance of Inverter using CNTFET and CMOS model in terms of power dissipation & speed. The power dissipation of the circuit in case of CNTFET is least & hence preferred over other CMOS model. Also the time taken is less which means speed is also improved using CNTFETs.The table no.3below shows comparison of performanceof a NAND Gate using CNTFET and CMOS model in terms of power dissipation & speed. The power dissipation of the circuit in case of CNTFET is least & hence preferred over other CMOS model. Also the time taken is less which means speed is also improved using CNTFETs.

X. RESULTS: GRAPHS & TABLES

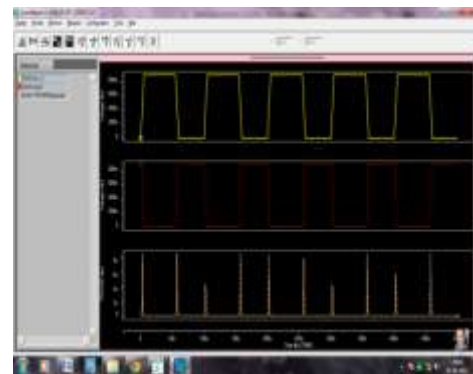


Figure.10: Inverter using CNTFET

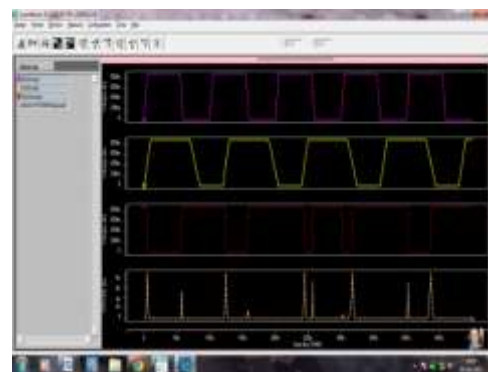


Figure.11: NAND Gate using CNTFET

TABLE.2: NAME OF CIRCUIT: INVERTER USING CNTFET and CMOS MODELS

	Average Power dissipation (watts)(J/s)	Time Delay (sec)	PDP(J)
CNTFET	1.620e-07	1.832e-11	2.96784e-16
IBM	2.117e-07	5.021e-10	10.6295e-17

TABLE.3: NAME OF CIRCUIT: NAND GATE USING DIFFERENT MODELS

	Average Power dissipation (watts)(J/s)	Time Delay (sec)	PDP(J)
CNTFET	2.825e-07	1.299e-09	3.6696e-16
IBM	7.151e-05	1.759e-09	12.5786e-14

XI. KEY ADVANTAGES

- Better control over channel formation
- Better threshold voltage
- Better subthreshold slope
- High electron mobility
- High current density
- High transconductance

XII. APPLICATION:

- High-speed transistors,
- Optoelectronics devices,
- Bio-sensors

XIII. CONCLUSIONS

We have seen in the above simulated waveforms & tables that by using CNTFETs in VLSI circuits power dissipation can be reduced and speed can be improved. Using CNTFETs total power dissipation & time delay are least compared to other CMOS model. Hence use of CNTFETs in VLSI circuits is essential.

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