A High Resolution All Digital Duty Cycle Corrector Using Reversible Multiplexer Logic

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***Abstract*— In low power design and high speed applications, a high resolution all digital duty cycle corrector (HR-ADDCC) is proposed. It is used to correct the duty cycle error and to achieve an exact 50% output duty cycle. A reversible multiplexer logic is used to obtain a glitch free circuit, which is more feasible compared to conventional logic gates. In addition, a reversible multiplexer based DCC (Duty Cycle Corrector) is proposed to achieve an exact 50% output duty cycle with low power area and high resolution duty cycle correction. It is suitable for wide operating frequency range in nanometer CMOS technology process.**

Keywords— **Duty Cycle Corrector (DCC), Delay Locked Loop (DLL), All-Digital Duty Cycle Corrector (ADDCC),Digitally Controlled Delay Line (DCDL).**

I. INTRODUCTION

In high-speed devices, such as double data rate (DDR) memory or double sampling analog-to-digital converter (ADC), the positive edge and the negative edge of the clock are utilized for sampling the input data. Thus, these systems require an exact 50% duty-cycle of input clock. Several approaches have been available to adjust the duty cycle error. Digital duty cycle corrector is one of the techniques to correct the error.

The two major types in the digital approach are as follows

1) Synchronous Mirror Delay (SMD).
2) Time-to-Digital Converter (TDC).

The SMD-based DCC consist of a half cycle delay line (HCDL) that can induce a delay mismatch problem in a nanometer CMOS technology. Hence, the operating frequency range and the duty cycle error are limited in this system. The TDC-based DCC quantizes CLK_IN period information into a digital code, and then this digital code is divided by two to control the delay line for generating the half-cycle delay time. The TDC-based DCC has a short locking time but it is not suitable for wide operating frequency range.

In this paper, a reversible multiplexer based duty cycle corrector is proposed. As compared with the SMD-based and TDC-based ADDCC, the proposed architecture can obtain a high resolution duty cycle correction.

The rest of the paper is organized as follows. The related works can be done in Section II. Section III explains the proposed system architecture. The simulation result is shown in Section IV. Finally, the conclusion is given in Section V.

II. RELATED WORKS

In conventional Pulse Width Control Loop PWCL [1], the ring oscillator is used to produce a 50% duty cycle reference source, has a large leakage power and its locking time is very long, while the operating frequency is low. The low voltage PWCL [2], needs an exact 50% duty cycle of the clock signal. It can operate in low voltage with fast locking and cannot generate other output duty cycle after design. In fast locking PWCL [3], is used to achieve a fast locked and pre-settable output duty cycle.

To obtain fast locking, a voltage-difference-to-digital converter (VDDC) is used. It may cost large chip area and power consumption. The mutual correlated PWCL [4], generate a complementary clock, and reduce jitter and to correct the duty cycle error by using single-to-complementary (STC) circuits. However, it can produce a fixed duty cycle and has a narrow operating frequency range. In single path PWCL [5], is used to achieve phase-locked and pre-settable output duty cycles. The phase lock of the DLL locking time would be very long to correct the operation.

The NAND based DCDL (Digitally Controlled Delay Line) is used to correct the duty cycle error, and to achieve an exact 50% duty cycle for input clock with low power leakage. But, the data loss is present in this system. To avoid, these problem a reversible multiplexer DCC is proposed.

III. ARCHITECTURE OF PROPOSED DCC

A. Reversible Multiplexer

Reversible multiplexer means a number of inputs are equal to the number of outputs. In conventional logic gates, the output is differing for each operation as a result the loss of information takes place hence the power dissipation is there. But in reversible gate, there is a specific output for specific input.

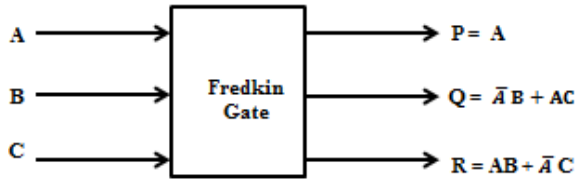


Fig1. Block Diagram of Fredkin Gate

Fig.1 shows the block diagram of fredkin gate. Fredkin gate is used for developing the reversible multiplexer. It consists of three inputs and three outputs. The inputs are A, B, C and the outputs are P, Q and R. The truth table shows the operation, of the fredkin gate. The truth table of the fredkin gate is given in table-1.

Table-1 Truth table of Fredkin Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	0
1	1	1	1	1	1

Unutilized output from a gate is called garbage output. P is called as a garbage output, which is needed in the circuit to equalize the number of inputs and outputs condition. Q and R are called as a quantum output and it can produce the average weight of the output. Depending upon the selection line either Q or R will be produced.

B. Reversible Mux Based Dcc

Fig.2 shows the circuit diagram of the proposed reversible multiplexer DCC. In this structure, it consists of two blocks such as DCC (Duty Cycle Corrector) and DLL (Delay Locked Loop). The DCC is used to correct the duty cycle error and the DLL is used to align the phase of the clock signal.

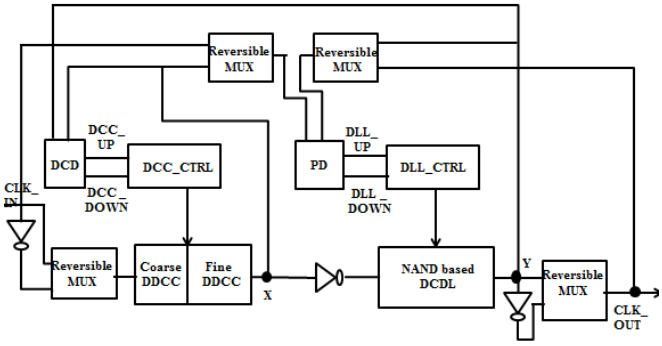


Fig.2 Block diagram of proposed system

Initially, the input clock input signal is given to the DCC circuit, and it can produce the output as X signal. Then the inverted X signal is passed to the DLL. The Y is the output signal, which is generated from DLL circuit.

Both the output signals such as X and Y are given to the reversible multiplexer block. Depending on the selection line of the reversible multiplexer, the operation has to be performed. In Fig.2 the inputs of the reversible multiplexer are X and Y signal and the selection signal is given as S. When S=0, the output becomes Q= $\bar{S}X+SY$. Similarly, if the S=1, then the output produced by the reversible multiplexer as R= $SX+\bar{S}Y$.

Depending upon the output, the phase detector detects the phase error between the signals X and Y. The DLL_CTRL is used to adjust the pulse width of the clock signal. If the phase error is eliminated, then the DLL get locked. After the DLL is locked, the DCC start to correct the duty cycle error. If the error between the two signals (DLL_CLK and CLK_IN) is corrected, then the DCC get locked.

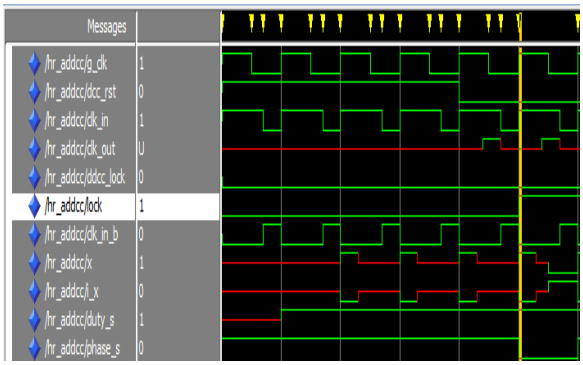
IV. RESULTS AND DISCUSSIONS

The simulation output waveform can be coded by using Model Sim software. With the help of Xilinx software, the total power consumption, area and delay are calculated.

TABLE-2

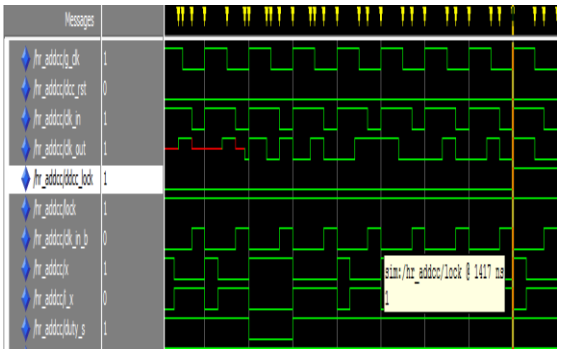
Parameters	Reversible MUX based DCC	NAND based DCDL	MUX based DCC
Total power consumption	34	37	39
Area	189MB	192MB	220MB
Delay	2.636 ns	5.747ns	8.941ns

Table-2 compares the technique, which is to be used to correct the duty cycle error. It can compare the parameters such as power, area and delay. The reversible multiplexer based DCC is more feasible than the other two techniques as shown in Table-2.



3(a)

Fig.3 shows the simulation results of the proposed HR-ADDCC in DLL and DCC locked condition. If the positive phase of the clock signal gets aligned, then the DLL get under locking condition as shown in Fig.3 (a).



3(b)

Fig.3 Simulation waveform of the proposed HR-ADDCC.

The DCC starts to correct the duty cycle error. If the error is corrected, then the output clock signal produced an exact 50% duty cycle as shown in Fig.3 (b).

V. CONCLUSION

In this paper, a reversible logic based duty cycle corrector is proposed. It can be designed for power reduction in multiplexers. By using this technique the data loss could be avoided and the resolution of the duty cycle is improved with low power and low cost area. Experimental results show that the frequency range of the proposed ADDC is 250-1 MHz with DCC resolution is 5-3 ns. So, it is suitable for system on chip application (SoC).

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