Area Reduction of Test Pattern Generation Used in BIST Schemes

[1] Nandini Priya.M

[1] PG Scholar, VLSI Design, Dept of Electrical and Communication Engineering,

Avinashilingam Institute for Home Science and Higher Education for Women-University,

Faculty of Engineering, Coimbatore.

Abstract-This paper proposes a test pattern generator (TPG) for built-in-self-test. This method generates Multiple Single Input Change Vector (MSIC), which in turn are applied to the scan chain. The existing methodology uses Johnson counter, xor gate and LFSR for generating Multiple Single Input Change Vector. But the drawback of the previous technique was more Area consumption. Hence in order to reduce the area Multiple Single Input Change Vectors are generated using Johnson counter and Accumulator. This test pattern generation technique for BIST schemes is coded using VHDL and simulated using ModelSim 10.0b. The gate count and power required for test pattern generation is analyzed using Xilinx ISE 9.1 software.

Keywords-Built-in-self-test (BIST), Multiple Single Input Change Vector (MSIC), Test Pattern Generator (TPG).

I. INTRODUCTION

Built-in-self-test (BIST) technique is used in order to test the VLSI circuits. It reduces difficulty and complexity in VLSI testing. BIST technique has an on chip test hardware, on the circuit under test. The conventional BIST architecture, the LFSR is commonly used to generate the test pattern. The major drawback of this architecture is that the pseudorandom Patterns generated have high switching activity in the CUT [1], this lead to excessive power dissipation.

The first class is energy reduction TPGs. Girard et al. analyzed the impact of an LFSR's polynomial and seed selection on the circuits switching activity.

The second class is low power TPGs. Wang and Gupta used two LFSRs of different speeds to reduce the frequency of transition at the circuit inputs, leading to reduction in switching activity during test application [5]. Corno et al. provided a low power TPG based on cellular automata to reduce test power in combinational circuits [6]. The scheme in [7] is the approach focusing on modifying LFSR. Modified clock schemes reduce the power in the CUT. In [8], a low power BIST for data path architecture is proposed, which is circuit dependent. Bonhomme et al. [9] used a gating technique where two non overlapping clocks control the odd and even scan cells of the scan chain so that the shift power dissipation is reduced by the factor two. The ring generator [10] can generate a single input change (SIC) sequence. This method compares to the corresponding already known TPGs with respect to the fault coverage obtained by the test sequence of same length.

The third approach aims to reduce the dynamic power dissipation during scan shift through. Bhunia et al. [11] inserted blocking logic into the stimulus path of the scan flip-flops. The need for transistors insertion makes difficult to use with standard cell libraries that do not have powered gate

cells. In [12] reducing the dynamic power dissipation during scan-based testing is proposed. Partial gating technique has been proposed to reduce the dynamic power dissipation.

II.EXISTING METHODOLOGY

The existing methodology develops a test pattern generation scheme that converts SIC vector for multiple scan chains. Initially the SIC vectors are converted to its multiple code words. Then the code words generated are XORed with the seed vector. The multiple single input change vector generated are applied to the scan chain.

A. Test Pattern Generation Method

Test patterns are generated by Johnson counter bit-XOR with seed vector. Let us assume there are m primary inputs, M scan chain and l scan cells.

Let us assume there are m primary inputs and M scan chains in a full scan design, and each scan chain has l scan cells. Fig. 1 shows symbolic simulation for one generated pattern. The vector generated by an m-bit LFSR with the primitive polynomial can be expressed as S(t)=S0(t) S1(t) S2(t),….Sm-1(t), and the vector generated by an l-bit Johnson counter can be expressed as J(t)= J0(t) J1(t) J2(t),…, Jl-1(t). During the first clock cycle, J= J0J1J2,…, Jl-1 will bit-XOR with S=S0S1S2,…SM-1, and the results X1Xl+1X2l+1….,X(M-1)l+1 will be shifted into M scan chains. During second clock cycle J= Jl-1 J0J1J2,…, Jl-2,will in turn bit xor with the seed vector S=S0S1S2,…SM-1. The resulting X2Xl+2X2l+2….,X(M-1)l+2 will be shifted into each scan chain will be fully loaded with unique Johnson code word, and seed S0S1S2,…SM-1 will be applied to m PIs. Since the circular Johnson counter l unique Johnson code words through circular shifting a Johnson counter and xor gates constituting a linear sequential decompressor.

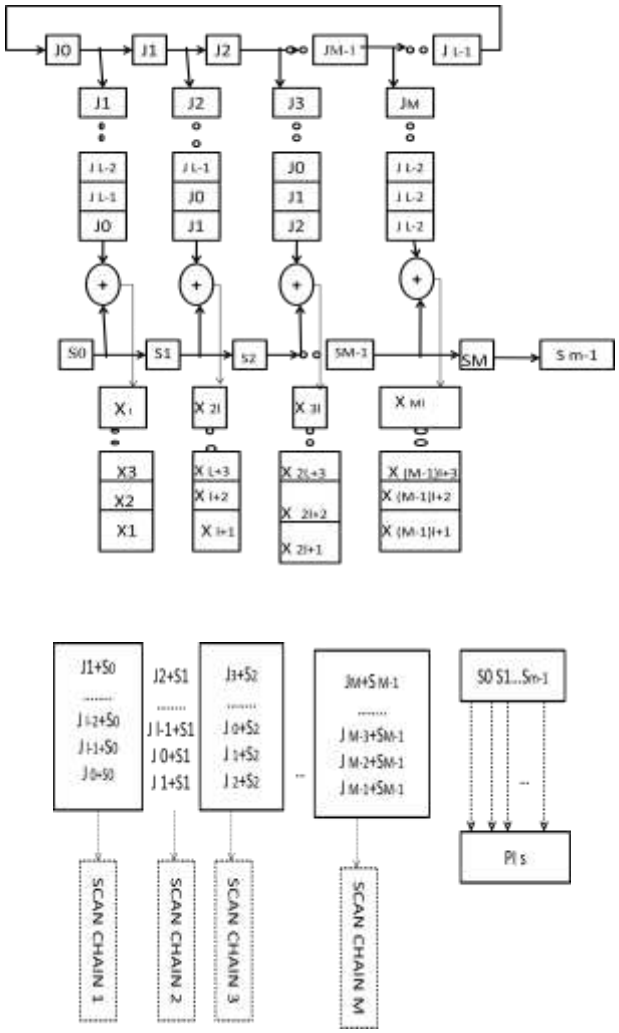

Fig.1 symbolic representation of an MSIC pattern generate

B. Reconfigurable Johnson Counter

According to the scenarios of the scan length either reconfigurable Johnson counter or scalable SIC counter is used to generate Johnson vector and Johnson keyword. There are three modes of operation.

1) Initialization:

During initialization process RJ_MODE is set to 1 and INIT is set to logic 0. So that reconfigurable Johnson counter is initialized to all zero states by clocking CLK 2 more than l times.

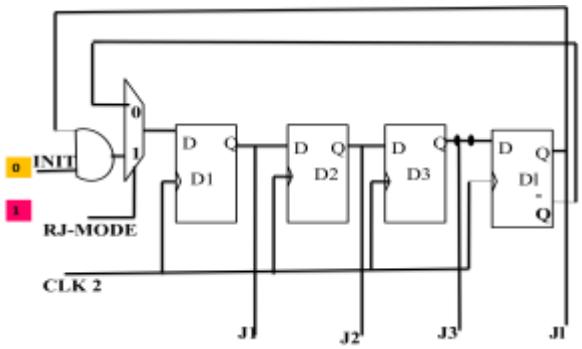

Fig.2 Initialization mode

2) Circular shift register mode:

During circular shift register mode RJ_MODE and INIT are set to logic 1 Johnson counter will output a Johnson codeword by clocking CLK2 *l* times.

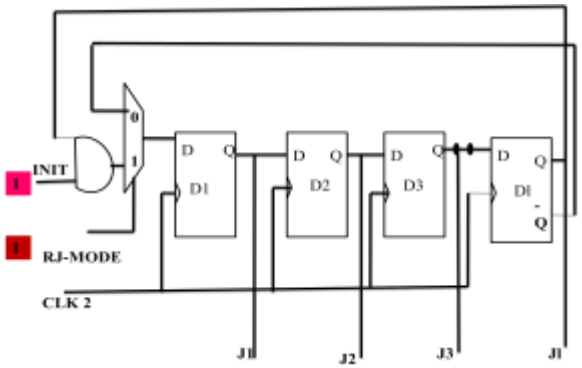

Fig.3 Circular shift mode

3) Normal mode:

During Normal mode RJ_MODE is set to logic 0

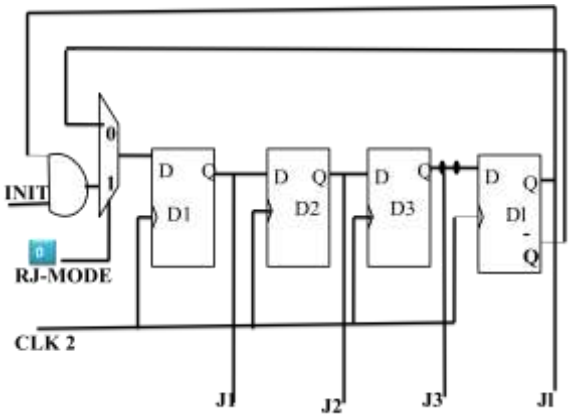

Fig.4 Normal mode

C. *Scalable SIC Counter*

For a maximal scan chain length l is much larger than the scan chain number M, scalable SIC counter is developed. Fig 1 shows the scalable SIC counter; it contains k-bit adder clocked by the rising SE signal, a k-bit subtractor clocked by test clock CLK2, an M-bit shift register clocked by CLK2 and k multipliers. It can operate in three modes of operation.

1) If SE=0, the count from the adder is stored to the k-bit subtractor. When SE=1, the contents of k-bit subtractor will be decreased from the stored count to all zeros gradually.
2) If SE=1 and the contents of the k-bit are not all zeros, M_Johnson will be kept at logic 1(0).
3) Otherwise, it will be kept at logic 0(1). Thus, the needed 1s(0s) will be shifted into the M-bit shift register by clocking CLK2 l times, and unique Johnson code words will be applied into different scan chains.

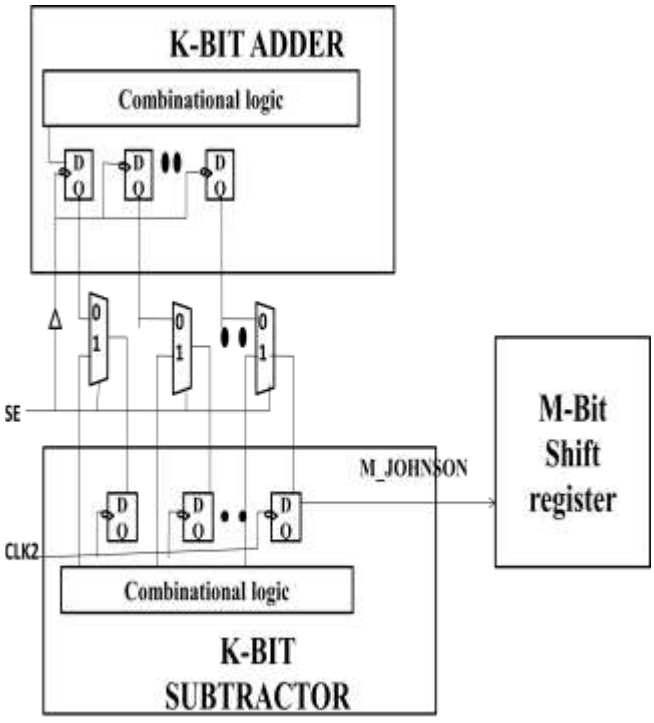

Fig.5 Scalable SIC Counter

D. MSIC-TPGs for Test-per-clock-schemes

The CUT's are arranged as n x m SRAM like grid Johnson counter. Each grid has two-input XOR gate whose inputs are tapped from a seed output and an output of the Johnson counter.

The outputs of the xor gates are applied to the CUT's PI's. A seed generator is an m-stage conventional LFSR, and operates at lower frequency CLK1. The procedure is as follows.

1) The seed generator generates a new seed by clocking CLK1 one time.
2) The Johnson counter generates a new vector by clocking CLK2 one time
3) Repeat 2 until 2l Johnson vectors are generated.
4) Repeat 1-3 until the expected fault coverage or test length is achieved.

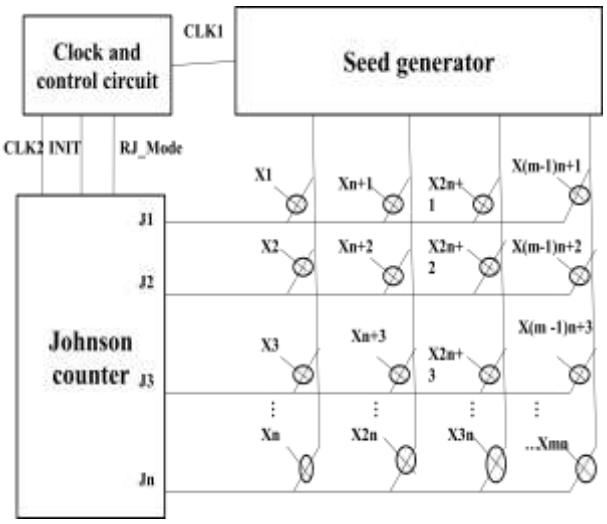

Fig.6 Test-per-clock-schemes

E. MSIC-TPGs for Test-per-scan-schemes

The MSIC-TPG for test-per-scan schemes is illustrated in Fig.7. The input of the xor comes from seed generator and the SIC counter, and their outputs are applied to M scan chains. The outputs of the seed generator and xor gates are applied to the CUT's PI respectively. The test procedure is as follows.

1) The seed circuit generates a new seed by clocking CLK1 one time.
2) RJ_MODE is set to "0". The reconfigurable Johnson counter will operate in the Johnson counter mode and generate a Johnson vector by clocking CLK2 one time.
3) After a new Johnson vector is generated, RJ_MODE and Init are set to 1. The reconfigurable Johnson counter will operates as a circular shift register, and generates l code words by clocking CLK2 l times.
4) Repeat 2-3 until 2l Johnson vectors are generated.
5) Repeat 1-4 until the expected fault coverage or test length is achieved.

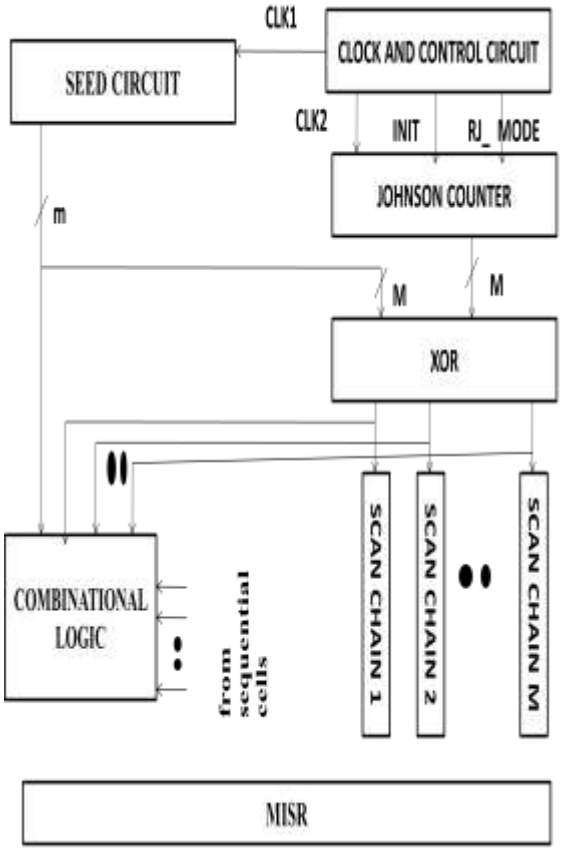

Fig.7 Test-per-scan-schemes

III. PROPOSED METHODOLOGY

This method proposes a test pattern generator for the BIST schemes. It generates a multiple single input change (MSIC) vectors in a pattern. These patterns generated are applied to the scan chains. This method is suitable for detecting faults in a combinational circuit. A Reconfigurable Johnson counter has been developed. This method generates SIC sequences, and converts them to low transition sequences for each scan chain. This can decrease the switching activity in scan cells during scan-in shifting. Existing methodology consumes more area. The proposed methodology has an advantage of reduced area. The proposed MSIC-TPG consists of Johnson counter, Adder and Registers. The proposed methodology has an advantage of reduced area. The proposed MSIC-TPG consists of Johnson counter, Adder and Registers.

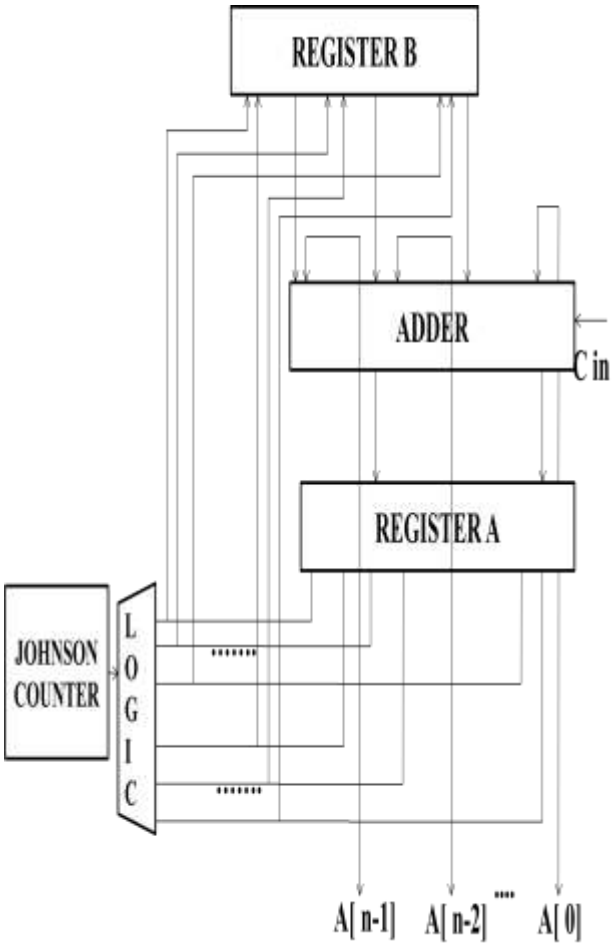

Fig.8 MSIC pattern Generation using accumulator architecture

IV. SIMULATION RESULTS AND ANALYSIS

The simulation results of testing 4 bit multiplier by applying MSIC vector generated using Johnson counter and Seed block has been shown in the Fig. 9. When the vectors of ref_out and test_out are equal, then the circuit is fault free circuit otherwise the circuit is faulty circuit.

The simulation results of testing with MSIC vector using accumulator architecture is shown in the Fig. 10. The area required for generating single input change vector by existing method is more. Total Equivalent Gate Count for Design for existing method is 7205. The total equivalent gate count for design for proposed approach is 3509. The area required for generating single input change vector for proposed accumulator architecture along with Johnson counter is comparatively smaller than Existing method. The area result for implementing existing method and proposed method is determined using Xilinx ISE 9.1 software is shown in the Fig.11&12. Area Report has been obtained between Existing and Proposed method as shown in Fig.13.

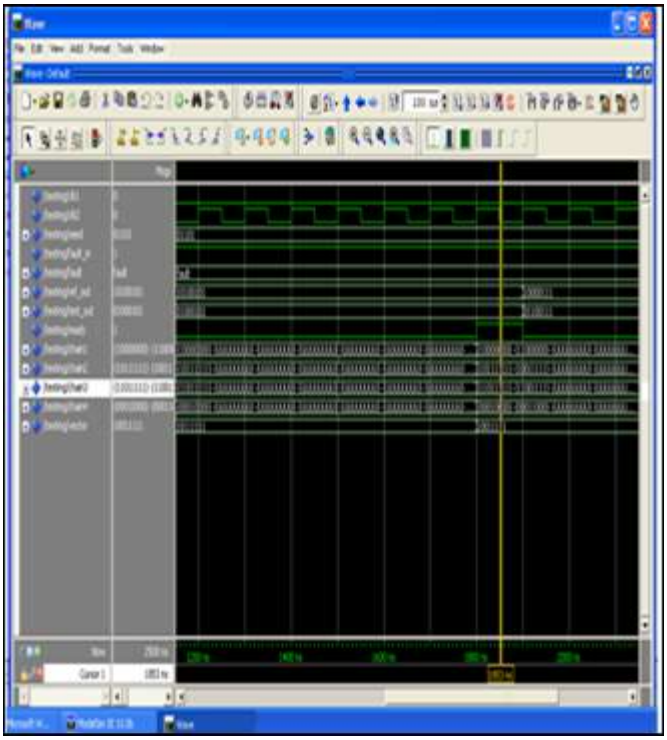

Fig.9 Simulation result for Existing method

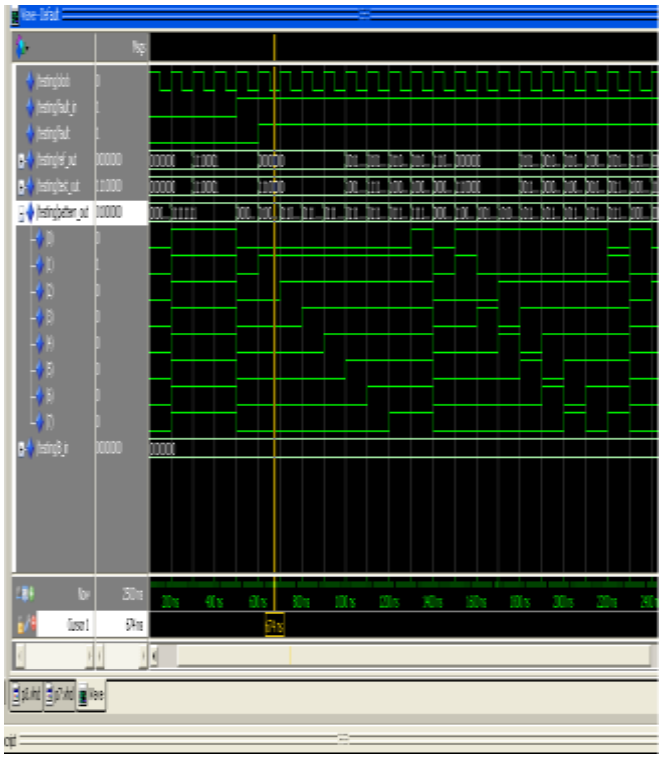

Fig.10 Simulation result for proposed method

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Total Number Slice Registers	135	1,536	9%	
Number used as Flip Flops	137			
Number used as Latches	2			
Number of 4 input LUTs	231	1,536	15%	
Logic Distribution				
Number of occupied Slices	177	768	23%	
Number of Slices containing only related logic	177	177	100%	
Number of Slices containing unrelated logic	0	177	0%	
Total Number of 4 input LUTs	330	1,536	21%	
Number used as logic	231			
Number used as a route-thru	99			
Number of bonded IOBs	3	124	2%	
Number of GCLKs	1	8	12%	
Total equivalent gate count for design	3,509			
Additional JTAG gate count for IOBs	144			

Fig.12 Area report for Test pattern generation using proposed method

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Total Number Slice Registers	457	1,536	29%	
Number used as Flip Flops	120			
Number used as Latches	337			
Number of 4 input LUTs	456	1,536	29%	
Logic Distribution				
Number of occupied Slices	421	768	54%	
Number of Slices containing only related logic	421	421	100%	
Number of Slices containing unrelated logic	0	421	0%	
Total Number of 4 input LUTs	682	1,536	44%	
Number used as logic	456			
Number used as a route-thru	226			
Number of bonded IOBs	88	124	70%	
Number of GCLKs	6	8	75%	
Total equivalent gate count for design	7,295			
Additional JTAG gate count for IOBs	4,224			

Performance Summary			
Final Timing Score:	0	Pinout Data:	Pinout Report
Routing Results:	All Signals Completely Routed	Clock Data:	Clock Report
Timing Constraints:	All Constraints Met		

Fig.11 Area report for Test pattern generation using Existing method

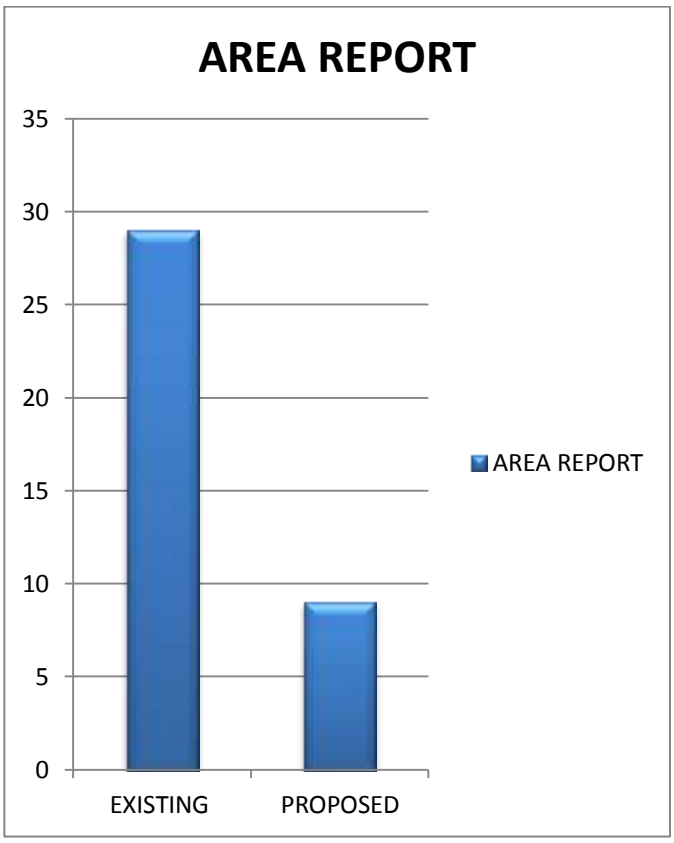

Fig.13 Comparison between Existing and Proposed method

V. CONCLUSION

This project implements a low power and area test pattern generation for the BIST schemes. The proposed method has an ability to detect the faults occurring in a combinational circuit. It has been found that the Existing method used for test pattern generation has high the area and power complexities. This drawback has been overcome by using the test patterns generated using Johnson counter and accumulator architecture in the proposed approach. There are various advantages of generating test patterns using this technique. They are minimum transition at the input, uniqueness of pattern, uniform distribution of pattern. This test pattern generation technique for BIST schemes is coded using VHDL and simulated using ModelSim 10.0b. The gate count and power consumption of this test pattern generation is analyzed using Xilinx ISE 9.1 software.

REFERENCES

[1] Y. Zorian, 'A distributed BIST control scheme for complex VLSI devices,' proceedings of 11th Annual IEEE VLSI Test Symposium Digital Papers, April 1993, pp. 4–9.

[2] P. Girard, 'Survey of low-power testing of VLSI circuits,' IEEE Design Test Comput., vol. 19, no. 3, pp. 80–90, May–June 2002.

[3] A. Abu-Issa and S. Quigley, 'Bit-swapping LFSR and scan-chain ordering: A novel technique for peak- and average-power reduction in scan-based BIST,' IEEE Trans. Computer-Aided Design Integrated Circuits System , vol. 28, no. 5, pp. 755–759, May 2009.

[4] P. Girard, L. Guiller, C. Landrault, S. Pravossoudovitch, J. Figueras, S. Manich, P. Teixeira, and M. Santos, 'Low-energy BIST design: Impact of the LFSR TPG parameters on the weighted switching activity,' Proceedings of IEEE International Symposium Circuits System, vol. 1. Jul. 1999, pp. 110–113.

[5] S. Wang and S. Gupta, 'DS-LFSR: A BIST TPG for low switching activity,' IEEE Transaction Computer Aided Design Integrated Circuits System, vol. 21, no. 7, pp. 842–851, July 2002.

[6] F. Corno, M. Rebaudengo, M. Reorda, G. Squillero, and M. Violante, 'Low power BIST via non -linear hybrid cellular automata,' Proceedings of 18th IEEE VLSI Test Symposium, April–May 2000, pp. 29–34.

[7] P. Girard, L. Guiller, C. Landrault, S. Pravossoudovitch, and H. Wunderlich, 'A modified clock scheme for a low power BIST test pattern generator,' Proceedings of 19th IEEE VTS VLSI Test Symposium , March–April 2001, pp. 306–311.

[8] D. Gizopoulos, N. Krantitis, A. Paschalis, M. Psarakis, and Y. Zorian, 'Low power/energy BIST scheme for datapaths,' proceedings of 18th IEEE VLSI Test Symposium, April–May 2000, pp. 23–28.

[9] Y. Bonhomme, P. Girard, L. Guiller, C. Landrault, and S. Pravossoudovitch, 'A gated clock scheme for low power scan testing of logic ICs or embedded cores,' proceedings of 10th Asian Test Symposium, November 2001, pp. 253–258.

[10] C. Laoudias and D. Nikolos, 'A new test pattern generator for high defect coverage in a BIST environment,' proceedings of 14th ACM Great Lakes Symposium VLSI, April 2004, pp. 417–420.

[11] S. Bhunia, H. Mahmoodi, D. Ghosh, S. Mukhopadhyay, and K. Roy, 'Low-power scan design using first-level supply gating,' IEEE Transaction Very Large Scale Integrated (VLSI) System, vol. 13, no. 3, pp. 384–395, March 2005.

[12] X. Kavousianos, D. Bakalis, and D. Nikolos, 'Efficient partial scan cell gating for low-power scan-based testing,' ACM Trans. Design Automation Electronic System, vol. 14, no. 2, pp. 28-1–28-15, March 2009.