

# High Frequency Power Optimized Ring Voltage Controlled Oscillator for 65nm CMOS Technology-Review

Neha K. Mendhe<sup>1</sup>, Prof. M. N. Thakare<sup>2</sup>, Prof. G .D. Korde<sup>3</sup>

Department of Electronics and Telecommunication Engineering,  
B.D.College of Engineering, Sewagram, Maharashtra, India

**Abstract**— A voltage controlled oscillator (VCO) is one of the most important basic building blocks in analog and digital circuits. Like any other circuit, with a VCO there are a number of design requirements that need to be known from the beginning of the design process. These basic requirements for the VCO will govern many of the decisions concerning the circuit topology and other fundamental aspects of the circuit. Some of the basic requirements are Tuning range, Tuning gain, tuning shift for a given tuning voltage change and low phase noise. This paper presents Ring voltage controlled oscillator (VCO) for wide tuning range with low power dissipation. The proposed ring oscillator is designed in four fully differential stages. The differential stages are designed to reduce phase noise. This paper presents the previous work on voltage controlled ring oscillator.

**Index Terms**-Phase noise, ring oscillator, voltage controlled oscillator (VCO)

## I. INTRODUCTION

Phase Locked Loops (PLL) is an essential for the synchronization purposes in space communication. PLLs are also widely employed in radio, telecommunications, computers and others electronic applications. PLL is composed of phase detector (PD), low pass filter (LPF), voltage controlled oscillator (VCO) and frequency divider. Voltage Controlled Oscillator (VCO) is vital part of PLL; its performance has strong impact on the PLL

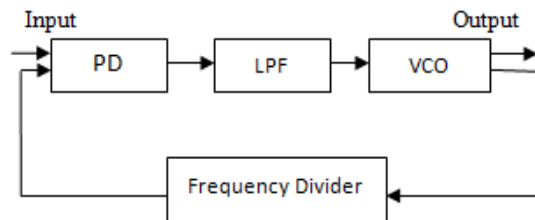


Fig 1 Block diagram of PLL

CMOS VCO can be designed using two types of structures, LC oscillators and Ring oscillators. LC oscillator is design by using inductor and capacitor. LC based VCO has narrow

tuning range, greater power dissipation and large die area. In addition, it is very difficult to integrate inductor in digital CMOS technology. Ring oscillator is composed of delay stages along with the feedback from output to input stage. Ring oscillator provides wide tuning range, relatively constant voltage swing and low voltage operation. Ring VCO requires less chip area and can be built in any standard CMOS processes.

VCRO can be implemented by single-ended or differential architecture of delay cell. Single ended ring topology comprises of inverters and each inverter is made up of an NMOS and PMOS transistors. On the other hand, differential topology is made up of a load (active or passive) with a NMOS differential pair. Currently, differential circuit topology is getting popularity among designers as it has common mode rejection of supply and substrate noise.

In this paper, a four-stage differential ring oscillator is analysed using 65 nm CMOS technology proposed by Joo-Myoung Kim [1]. It is redesigned by varying the design parameters to achieve high tuning range and low power consumption. Comparison with other oscillators is made to illustrate the advantages of this design.

## II. RING VCO DESIGN OBJECTIVE

The main requirement for designing the Ring VCO is that, it operates on wide tuning range, with low phase noise and low power dissipation. The VCOs performances are usually analysed by low phase noise, low power dissipation, low voltage operation, high speed oscillation, multi-phase application, supply sensitivity reduction, simplified integration method, small layout area and wide tuning range. The design of a VCO voltage controlled oscillator can be interesting and challenging. Whether the aim is to design a low noise VCO, a low current VCO, a PLL VCO, or one that will cover a wide tuning range there are many aspects that need to be addressed. Often when a successful design has been obtained, it will slightly modify to enable it to cover a wide range of similar applications. The proposed VCRO is designed at 6 GHz frequency with low power dissipation and low phase noise is achieved.

### III. RING VCO DESIGN

With the more development of wireless communication systems during the recent years, CMOS radio frequency integrated circuits have gained more attention and so did VCOs amenable for CMOS manufacturing process. Thus there is large number of publications on integrated CMOS VCO. There are also some books that explain the design of CMOS VCOs. The various realizations are differing in their frequency of operation, tuning range, phase noise characteristics, power consumption, circuit architecture and lastly whether they are fully integrated or not.

#### A. Ring VCO Design for Low Phase Noise

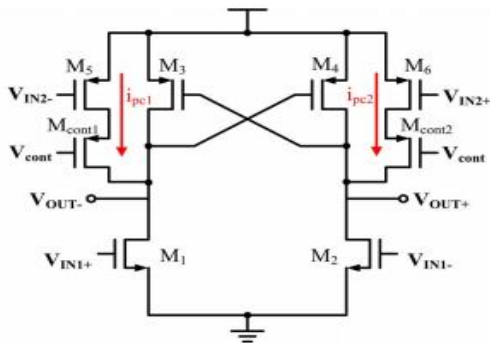


Fig 2(a) Delay cell

Fig 2(a) shows the schematic of the delay cell [1]. From Fig. 2(a), the delay cell consists of the NMOS input transistors (M1, M2), the cross-coupled PMOS transistors (M3, M4), the PMOS input transistors (M5, M6) and the PMOS control transistors (Mcont1, Mcont2) that are adopted to change the oscillation frequency by varying the control voltage Vcont.

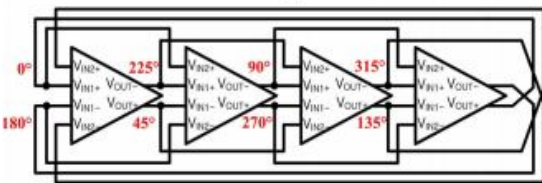


Fig 2(b) Four stage Ring VCO

Fig. 2(b) shows the four-stage ring VCO [1], which provides eight different phases ( $0^\circ, 45^\circ, 90^\circ, 135^\circ, 180^\circ, 225^\circ, 270^\circ, \text{ and } 315^\circ$ ). VIN1+ and VIN1- represent the differential voltage that is applied to the NMOS input transistors M1 and M2, and VOUT- and VOUT+ constitute the differential output voltage of the delay cell. Due to the oscillation condition of the four-stage structure, the phase difference between the input (VIN1+, VIN1-) and output (VOUT-, VOUT+) is  $225^\circ$ . VIN2- and VIN2+ are applied to the PMOS input transistors M5 and M6, respectively. As VIN2- and VIN2+ are taken from a delay cell that is two stages away from the corresponding delay

cell, VIN2- and VIN2+ come  $45^\circ$  earlier in phase than VIN1+ and VIN1-.

#### B. Design of VCRO for maximum frequency

The circuit schematics of delay cell [2] of ring oscillator are shown in Fig.3. The delay cell consists of one NMOS input pair (Mn1), one PMOS positive feedback pair (Mp1) for maintaining oscillation, one diode-connected PMOS pair (Mp2), and one PMOS transistor (Mb1) for frequency tuning.

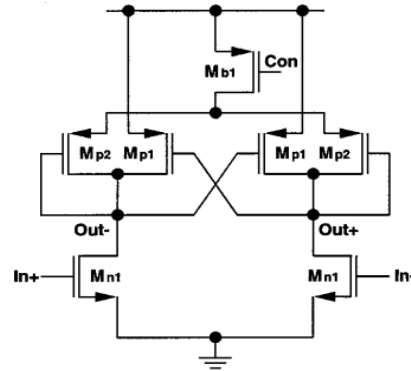


Fig 3 Delay cell

#### 1) High-Frequency Operation

An NMOS input pair is used to maximize the transconductance to capacitance ( $gm=C$ ) ratio to achieve high operating frequency with low power dissipation. To reduce the gm requirement and thus power dissipation, only parasitic capacitors of devices are utilized. Moreover, only two delay cells are included in the oscillator to minimize the power consumption.

#### 2) Wide Frequency-Tuning Range

A large tuning range is required to overcome the problem of process variation. The operating frequency of a ring oscillator can be tuned by variable capacitor (varactor) or by variable load impedance. In this design, frequency tuning is achieved by tuning the transconductance (gm) of the diode-connected PMOS devices Mp2. By controlling the current of Mb1, gm of Mp2 can be adjusted from zero to a value close to gm of Mp1. Therefore, over 50% tuning range can be easily achieved.

#### C. Low voltage VCRO

In the research [3], three stage ring oscillator is designed. For incorporation of this ring oscillator, only three of differential amplifiers are connected in a single delay path formation as shown in Fig.4. This VCRO is designed mainly for low power operation. Additionally, it will improve output voltage stability without redundant bias circuit, which occupies a large space in chip.

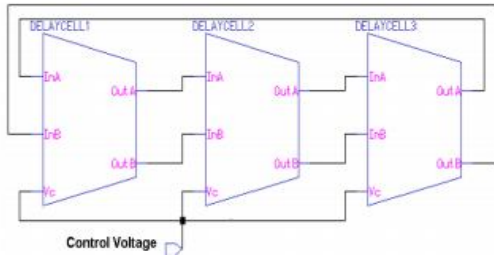


Fig 4 Three stage ring VCO

Fig. 5 shows the schematic diagram of single delay cell [3]. In this case a pair of CMOS differential push pulls inverter used as input. The push-pull inverter consists of two different sizing of PMOS and NMOS; two cross-coupled PMOS transistors connected in parallel with inverters PMOS transistors. These cross-coupled PMOS transistors are introduced for fast switching speed. Sizes of all four PMOS in the cell are chosen equally for smooth oscillation.

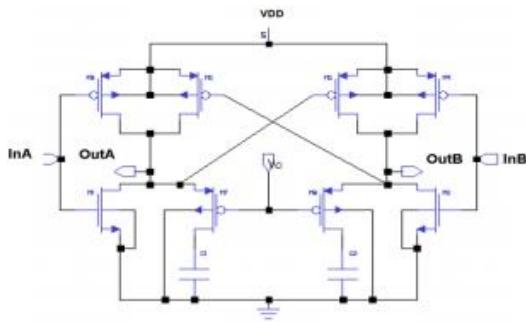


Fig.5 Delay cell

#### IV. COMPARISON AND DISCUSSION

TABLE 1

COMPARISON BETWEEN DIFFERENT APPROACHES

| Parameter  | Unit | Ref 1 | Ref 2 | Ref 3 |
|------------|------|-------|-------|-------|
| Technology | Nm   | 65    | 180   | 180   |
| Frequency  | MHz  | 645   | 2450  | 1770  |
| Pdiss      | Mw   | 10    | 11.7  | 13    |

|                |        |        |        |      |
|----------------|--------|--------|--------|------|
| Supply voltage | V      | 1      | 1.8    | 1.8  |
| Phase noise    | dbc/Hz | -110.8 | -108.5 | -102 |

It is clear from the Table 1 that for 180nm CMOS technology and frequency 1.77GHz, Power dissipation is more but phase noise is reduced. While in [2] frequency is increase up to 2.45GHz, Power dissipation is reduced but phase noise is more. Because of this Joo-Myoung Kim[1] uses 65nm technology to achieve low power dissipation.

#### V. CONCLUSIONS

Ring oscillators are basic building blocks of complex integrated circuits. They are mainly used as clock generating circuits. Many different types of ring oscillators are presented in literature. Ring VCO for low phase noise [1], for maximum frequency [2] and with low power consumption [3].

#### REFERENCES

- [1] Joo-Myoung Kim, Seok-Kyun Han, and Sang-Gug Lee "A Low-Noise Four-Stage Voltage-Controlled Ring Oscillator in Deep-Submicrometer" IEEE Transactions on Circuits And Systems—II: Express Briefs, Vol. 60, No. 2, Pp.71-75, February 2013.
- [2] William Shing Tak Yan "A 900-Mhz CMOS Low-Phase-Noise Voltage-Controlled Ring Oscillator" IEEE transactions on circuits and systems—II: analog and digital signal processing, vol. 48, no. 2, February 2001
- [3] JubayerJalil, Manum Bin Ibne Reaz, Labonah Farzana Rahman,"A 2.45 GHz CMOS Voltage Controlled Ring Oscillator for Active Transponder", Published in Intelligent and Advance systems(ICIAS) 2012<sup>th</sup> International Conference,pp.807-810.
- [4] Z. Z. Chen T. C. Lee, "The design and analysis of dual-delay-path ring oscillators,"IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 58, no.3,pp. 470-478, Mar. 2011.
- [5] Yuping Toh, John A. McNeill "Single-Ended to Differential Converter for Multiple-Stage Single-Ended Ring Oscillators" Published in IEEE Journal Of Solid-State Circuits, Vol. 38, No. 1, January 2003. Pp 141-145.
- [6] Wancheng Zhang, Nan-Jian Wu , Tamotsu Hashizume and Seiya Kasai, "Novel Hybrid Voltage Controlled Ring Oscillators Using Single Electron and MOS Transistors", Published in Nanotechnology, IEEE Transactions on volume 6,issue 2, March 2007,Pp 146-157.
- [7] Y. A. Eken and J. P. Uyemura, "A 5.9-GHz voltage-controlled ring oscillator in 0.18- $\mu$ m CMOS,"IEEE J. Solid-State Circuits, vol. 39, no. 1,pp. 230-233, Jan. 2004.
- [8] J. Choi and K. Lim J. Laskar, "A ring VCO with wide and linear tuning characteristics for a cognitive radio system," in Proc. IEEE Radio Freq. Integra. Circuits Symp., 2008, pp. 395-398.