Performance Evaluation of Multicarrier SPWM Strategies for Three Phase Z - source Seven Level Diode Clamped Inverter

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***Abstract*— This paper presents multicarrier PWM strategies for three phase diode clamped seven level Z-source inverter. Multilevel inverters posses the advantage of reduced harmonics, high power capability and high voltage level. Impedance network in the diode clamped multilevel inverter circuit will perform boost operation. This paper focuses on multicarrier sinusoidal pulse width modulation (MCSPWM) strategy for the three phase seven level Z-source diode clamped inverter. Performance parameters of three phase seven level Z-source diode clamped inverter have been analyzed. A simulation model of three phase seven level Z-source diode clamped inverter developed using MATLAB/SIMULINK and its performance has been analyzed.**

***Keywords*— APOD, CO, POD, PD, MCSPWM.**

I. INTRODUCTION

Multilevel inverter is a switching converter where the appropriate control of an arrangement of switching devices allows combining diverse input voltages to synthesize a sinusoidal output voltage waveform. Multilevel inverter presents several other advantages. Multilevel inverter generates better output waveforms with a lower dv/dt than the standard inverter. Then, multilevel inverter can increase the power quality due to the great number of levels of the output voltage: in this way, the ac side filter can be reduced, decreasing its costs and losses. Gajanayake et al [1] developed the closed-loop controller for a Z-source inverter. Huang et al [2] proposed Z-source inverter for residential photovoltaic applications. Loh et al [3] have used pulse-width modulated strategies for Z-source neutral point clamped inverter. Various pulse-width modulated strategies for Z-source inverter was discussed by Loh et al [4]. Different control strategies for Z-source neutral-point-clamped Inverter and also for cascaded MLI were discussed in [5, 6]. Shafie Bakar et al [7] described the various PWM techniques for single phase Z-source inverter. Yousuf et al [8] introduced multi carrier PWM technique for five level inverter. Three level Z-source inverter topology was introduced by Peng in [9]. Rendusara et al [10] analyzed common mode voltage and PWM strategies for adjustable speed drive. Ravi Chandrudu et al [11] developed Z-source inverter for induction motor drive. Shanthi and Natarajan [12] proposed carrier overlapping PWM methods for five level diode clampd inverter. Dehghan et al [13] proposed Z-source inverter with dual ac output and dual DC inputs. Ali and Kamaraj [14] introduced double carrier pulse width modulation control.

II. Z-SOURCE SEVEN LEVEL INVERTER

Figure 1 shows the two-port network that consists of an inductors (L1, L2) and capacitors (C1, C2) and connected in X shape is employed to provide an impedance source (Z-source) coupling the inverter to the dc source. The Z-source multilevel inverter utilizes shoot-through state to boost the input dc voltage of inverter switches when both switches in the same phase leg are on. The impedance source inverters are having lower costs, reliable, less complexity and higher efficiency.

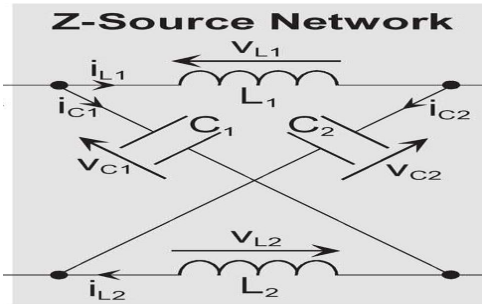

Figure 1 Impedance Network

Figure 2 shows the seven level Z-source diode clamped inverter, Which delivers the staircase output voltage using several levels of DC voltages developed by input DC capacitors. If m is the number of output voltage level, then the number of capacitors required on the DC bus are (m-1), the number of power electronic switches per phase are 2(m-1) and the number of diodes per phase are 2(m-2). This design formula is most common for all the neutral clamped

multilevel inverters. The DC bus voltage is split into seven levels using six capacitors. The voltage across each capacitor is $V_{DC}/6$ and the voltage stress across each switch is limited to one capacitor voltage through clamping diodes. The midpoint of the six capacitors 'n'can be defined as the neutral point. As the number of levels increase the harmonic distortion decreases and efficiency of the inverter increases because of the reduced switching losses. The number of levels in multilevel inverters is limited because of the large number of clamping diodes required. The reverse recovery of these diodes is especially with multicarrier PWM techniques in a high voltage application is a major design challenge.

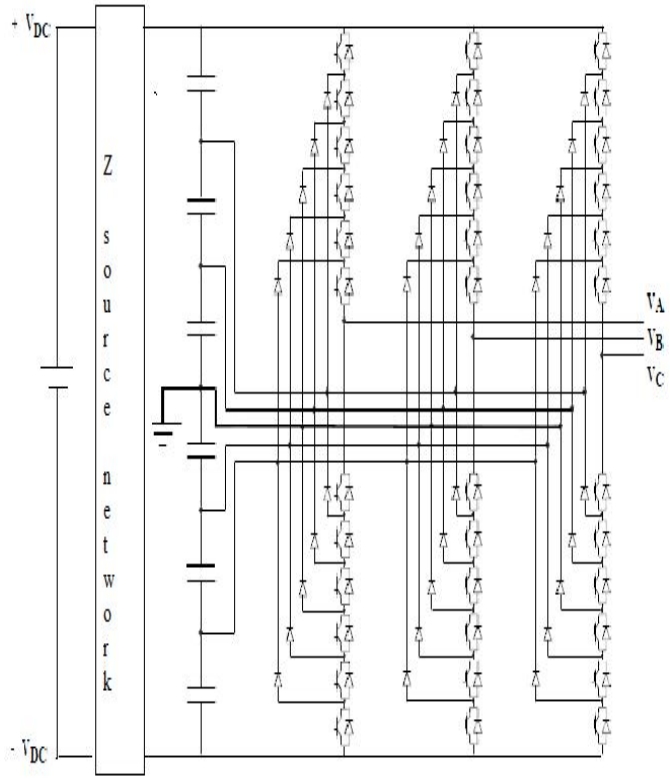

Figure 2 Seven level Z-source diode clamped multilevel inverter.

III. MULTICARRIER PWM STRATEGY

Multicarrier PWM strategy is the widely adopted modulation strategy for MLI. It is similar to that of the sinusoidal PWM strategy except for the fact that several carriers are used. Multicarrier PWM is one in which several triangular carrier signals are compared with one sinusoidal modulating signal. The number of carriers required to produce m-level output is m-1. All carriers have the same peak to peak amplitude A_c and same frequency f_c except for variable frequency PWM. The reference waveform has peak to peak amplitude of A_m and a frequency f_m. The reference is continuously compared with each of the carrier signals and whenever the reference is greater than the carrier signal, pulse is generated. There are many carrier arrangements to implement the PWM strategies. In this work the following strategies were carried out.

A. Phase disposition PWM strategy (PDPWM).

B. Phase opposition disposition PWM strategy (PODPWM).

C. Alternate phase opposition disposition PWM strategy (APODPWM).

D. Carrier overlapping PWM strategy (COPWM).

E. Variable frequency PWM strategy (VFPWM).

The formulae to find the Amplitude of modulation indices are as follows:

For PDPWM, PODPWM, APODPWM and VFPWM:

$$m_a = 2A_m/(m-1)A_c) \qquad (1)$$

For COPWM:

$$m_a = A_m / 2A_c \qquad (2)$$

The frequency ratio m_f is as follows: $m_f = f_c / f_m$ (3)

A. *Phase Disposition PWM strategy.*

In PDPWM Strategy for an m-level inverter, (m-1) carriers with the same frequency f_c and same amplitude A_c are positioned such that the bands they occupy are contiguous. If the reference wave is more than a carrier signal, then the active devices corresponding to that carrier are switched on. Otherwise, the devices switch off. Figure 3 shows the arrangement of carrier and modulation signals of PDPWM strategy.

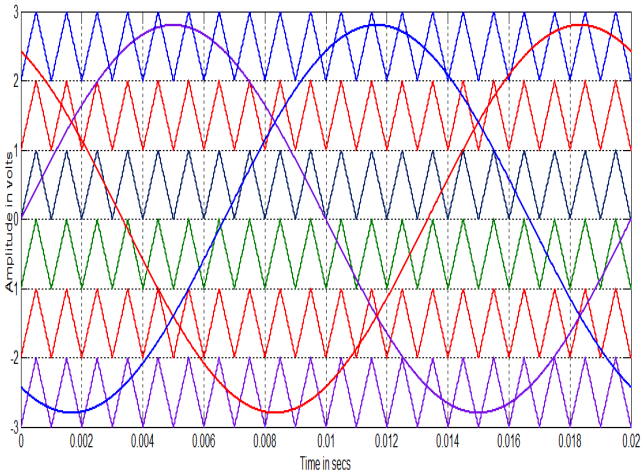

Figure 3 Carrier arrangement for PDPWM strategy (m_a=0.9 and m_f=20)

B. *Phase Opposition Disposition PWM strategy.*

In POD strategy the carrier waveforms above the zero reference are in phase. The carrier waveforms below zero reference are also in phase, but are 180 degrees phase shifted from those above zero as shown in Figure 4.

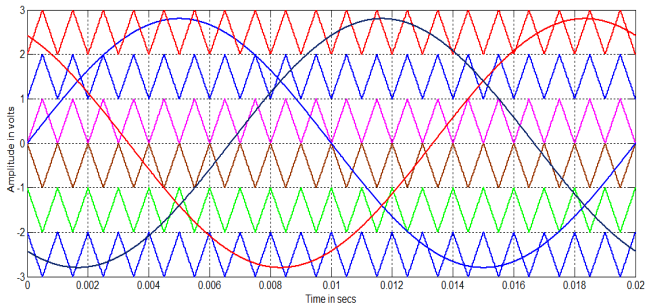

Figure 4 Carrier arrangement for PODPWM strategy (m_a=0.9 and m_f=20)

C. *Alternate Phase Opposition Disposition PWM strategy*

In APOD strategy the carriers of same amplitude are phase displaced from each other by 180 degrees alternately. The carrier arrangement is shown in Figure 5.

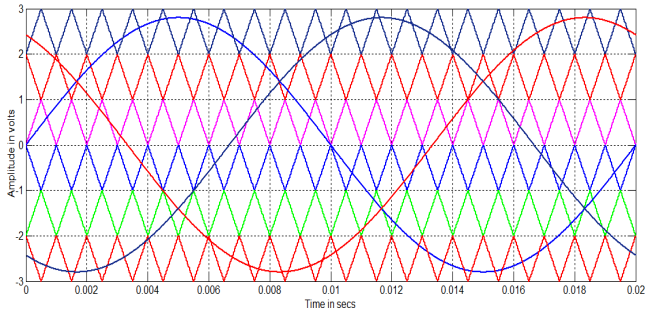

Figure 5 Carrier arrangement for APODPWM strategy (m_a=0.9 and m_f=20)

D. *Carrier overlapping PWM strategy.*

In COPWM strategy, carriers with the same frequency f_c and same peak-to-peak amplitude A_c are disposed such that the bands they occupy are overlap each other; the overlapping vertical distance between each carrier is $A_c/2$. The reference waveform is centered in the middle of the carrier set as in Figure 6.

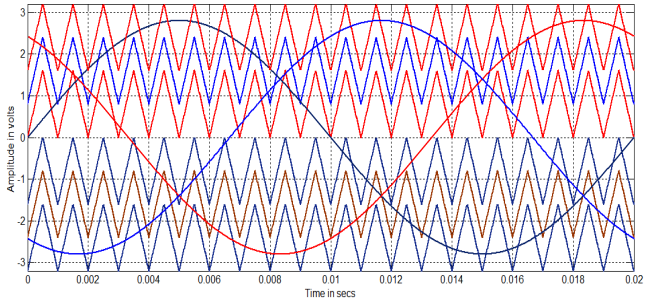

Figure 6 Carrier arrangement for COPWM strategy (m_a=0.9 and m_f=20)

E. *Variable frequency PWM strategy.*

The number of switching for upper and lower devices of chosen MLI is much more than that of intermediate switches in other PWM using constant frequency carriers. In order to equalize the number of switching for all the switches, variable frequency PWM strategy is used.

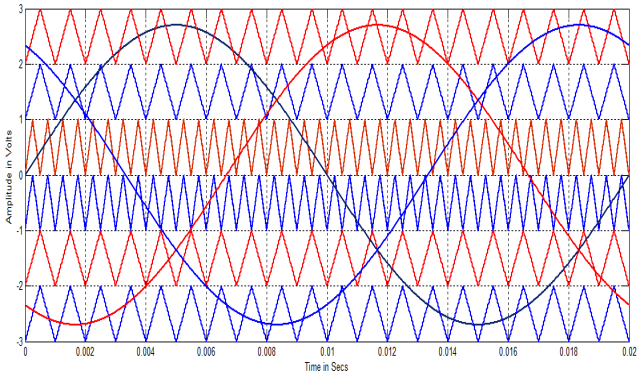

Figure 7 Carrier arrangement for VFPWM strategy (m_a=0.9 and m_{f1}=20,m_{f2}=40)

IV. SIMULATION RESULTS

The Z-source diode clamped seven level inverter is modeled in SIMULINK using power system block set. Switching signals for diode clamped multilevel inverter using MCSPWM strategies are simulated. Simulations are performed for different values of m_a ranging from 0.8 to 1 and the corresponding %THD are measured using the FFT block and their values are listed in Table I. Figure 8-17 show the simulated output voltage of three phase seven level Z-source DCMLI and their harmonic spectra. Figure 8 displays the seven level output voltage generated by PDPWM switching strategy and its FFT plot is shown in Figure 9. Figure 10 shows the seven level output voltage generated by PODPWM strategy and its FFT plot is shown in Figure 11. Figure 12 shows the seven level output voltage generated by APODPWM strategy and its FFT plot is shown in Figure 13. Figure 14 shows the seven level output voltage generated by COPWM strategy and its FFT plot is shown in Figure 15. Figure 16 shows the seven level output voltage generated by VFPWM strategy and its FFT plot is shown in Figure 17. Tables II and III displayed the V_{RMS} (fundamental) of the output voltage and Crest Factor (CF) for various modulation indices of Z -source diode clamped seven level inverter respectively.

The following parameter values are used for simulation: V_{DC} =420V, C=1000e-3 F, R (load) = 100 ohms, f_c=1000 Hz and f_m=50Hz.

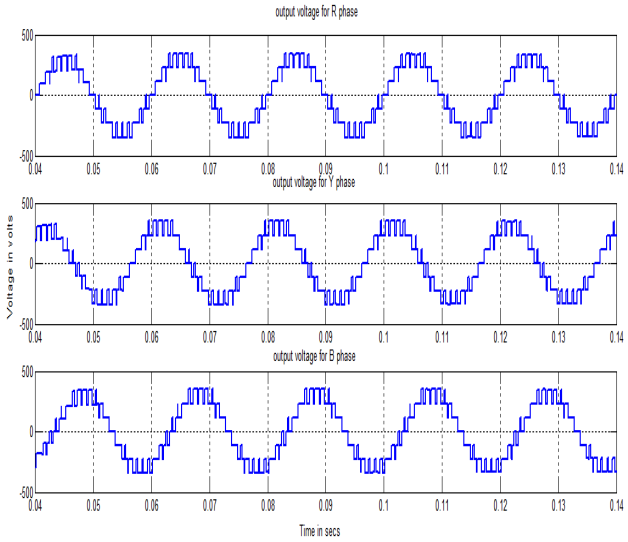

Figure 8 Output voltage generated by PDPWM

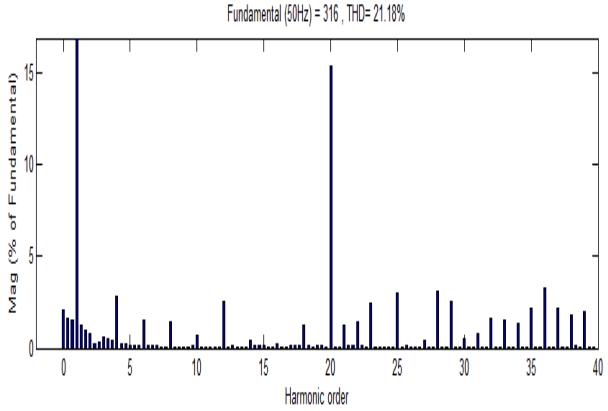

Figure 9 FFT plot for output voltage of PDPWM

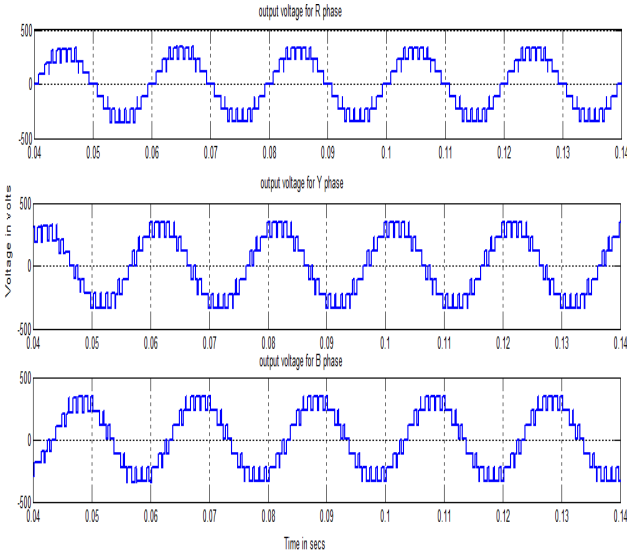

Figure 10 Output voltage generated by PODPWM

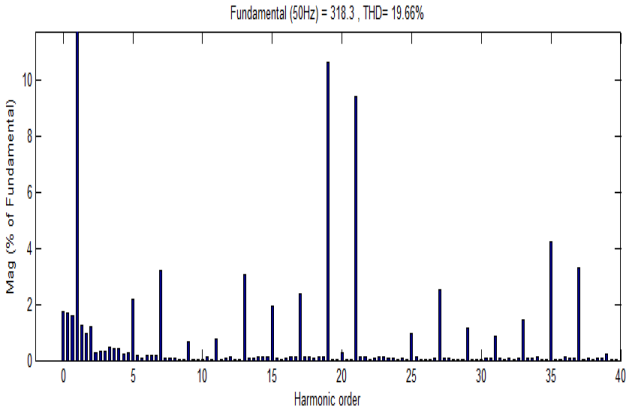

Figure 11 FFT plot for output voltage of PODPWM

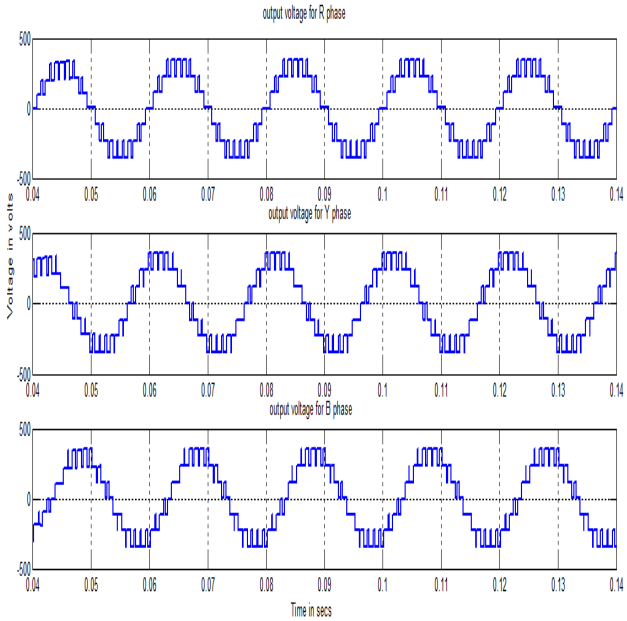

Figure 12 Output voltage generated by APODPWM

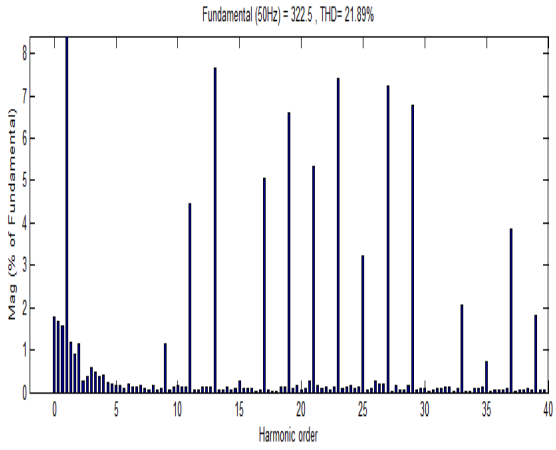

Figure 13 FFT plot for output voltage of APODPWM

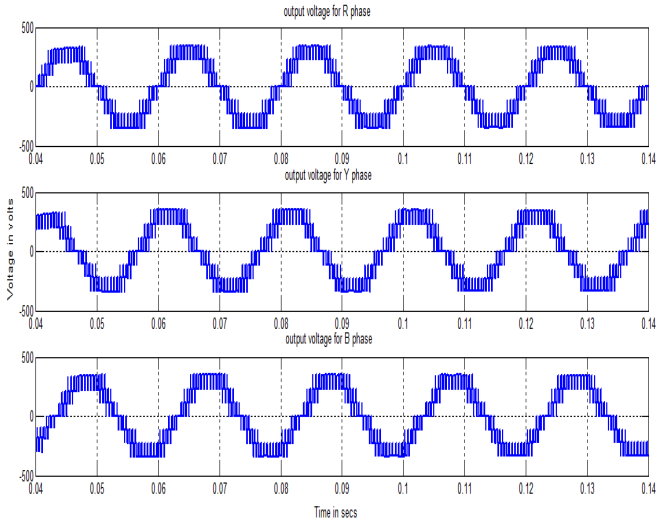

Figure 14 Output voltage generated by COPWM

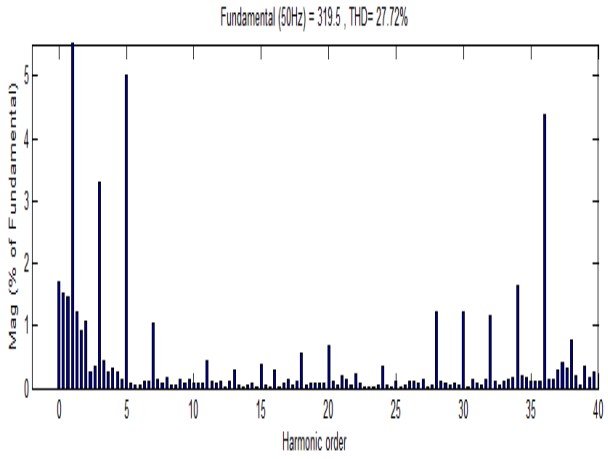

Figure 15 FFT plot for output voltage of COPWM

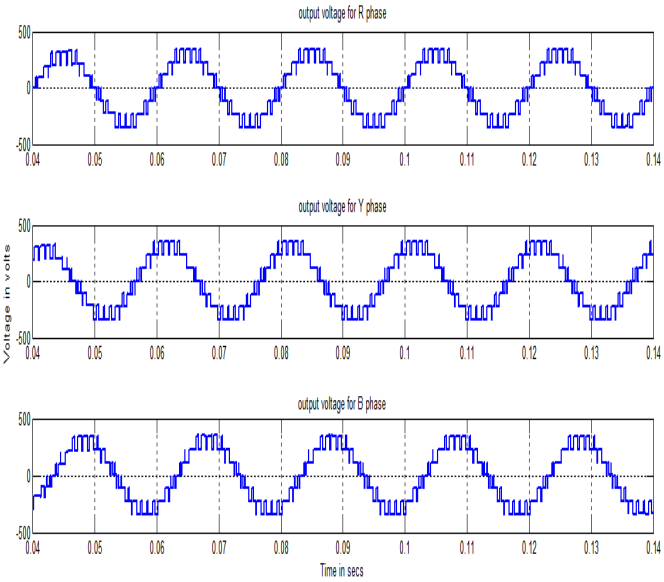

Figure 16 Output voltage generated by VFPWM

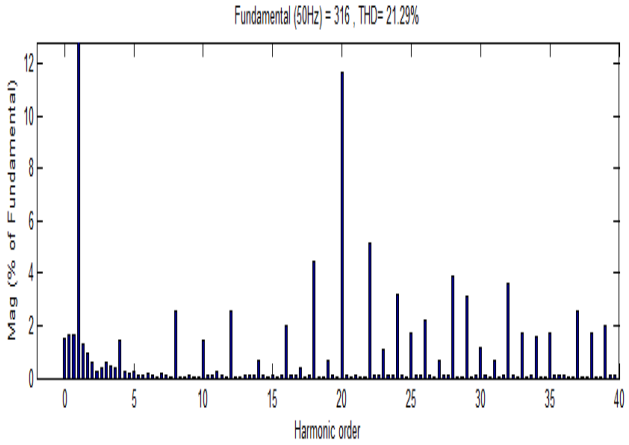

Figure 17 FFT plot for output voltage of VFPWM

TABLE I.

% THD For Different Modulation Indices

ma	PD	POD	APOD	CO	VF
1	17.90	16.24	18.57	22.19	18.32
0.9	21.18	19.66	21.89	27.72	21.29
0.8	23.68	22.56	22.86	32.52	23.63

TABLE II.

V_{RMS} (Fundamental) For Different Modulation Indices

m_a	PD	POD	APOD	CO	VF
1	239.9	239.7	244.7	246.6	239.6
0.9	223.3	225.1	228	225.9	216
0.8	207	207.1	211.1	203	207.3

TABLE III.

Crest Factor for Different Modulation Indices

m_a	PD	POD	APOD	CO	VF
1	1.41433	1.414267	1.41438	1.411597	1.41444
0.9	1.413793	1.414038	1.414473	1.414342	1.41323
0.8	1.41009	1.413809	1.414495	1.414285	1.41437

V. CONCLUSION

In this paper, multicarrier SPWM strategy for three phase Z source seven level diode clamped inverter have been presented. Z source multilevel inverter gives higher output voltage through its Z source network. Performance factors like %THD, V_{RMS} and CF have been measured, presented and analyzed. It is found that the PODPWM strategy provides lower %THD and less number of dominant harmonics than the other strategies and APODPWM strategy provides higher V_{RMS} and CF is almost same for all the strategies.

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