

# Low Power Full Adder With Reduced Transistor Count

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**Abstract**— Basic building blocks of most of the arithmetic and logic circuits are formed by XOR logic gate. This paper proposes a new 3T-XOR gate with significant area and power savings. In most of the digital systems adder lies in the critical path that increases the overall computational delay of the system. A new eight transistors one bit full adder based on 3T-XOR gate is presented. Simulations results utilizing standard 90nm CMOS technology illustrate a significant improvement in terms of number of transistors, chip area and propagation delay.

**Keywords**— Full adder, CMOS, PDP, Pass transistor, XOR, low power.

## I. INTRODUCTION

The growing demand for portable devices is driving the chip designers to rely on scaling down of device sizes with increased computation performance and longer battery life. The increasing chip density and complexity has led to more power consumption. This directly affects the battery operated portable devices and requires expensive cooling and packaging technologies.

There are three types of power consumption in VLSI circuits namely short circuit power, static power and dynamic power. The short circuit power dissipation is due to the short circuit current generated when both NMOS and PMOS transistors are simultaneously active for a small duration. The static power dissipation varies with process technology. The dominant dynamic power due to charging and discharging of load capacitance is given by the following equation (1),

$$\text{Dynamic Power} = \alpha (V_{DD})^2 f C_L \quad \text{--- (1)}$$

where  $\alpha$  is the switching activity,  $V_{DD}$  is the supply voltage,  $f$  is the switching frequency  $C_L$  is the load capacitance. Lower the voltage is, the smaller the power consumption. However, using a lower  $V_{DD}$  increases the delay. The alternate way of decreasing the power is by reducing the number of switching transistors.

Around 30% of the total power is consumed by the data path. Adders are an extensively used component in data path and therefore careful design and analysis is required. The overall system performance can be increased significantly by enhancing the performance of the full adders. XOR logic gates play an important role in building up of most of the data path units, specifically adders, multipliers, phase detectors, comparators, parity checkers and compressors. The early designs of XOR gate was based on either eight transistors or six transistors [1] that are conventionally used in most designs. This paper proposes a new design technique for a 3T-XOR gate [2] circuit based on static CMOS inverter logic and Pass transistor logic (PTL). The rest of the paper is organized as follows, in Section 2, a review of full adders in previous works is presented. In Section 3, the proposed work on XOR gate and full adder circuit is presented, which is followed by the simulation results and conclusions in Sections 4 and 5, respectively.

II. REVIEW OF FULL ADDER TOPOLOGIES

Most of the Full adder structures make use of XOR and XNOR logic gates. Conventional CMOS [3] full adder with 28 transistors is a high power and robust full adder. This design is based on complementary pull up and pull down topologies. It has high noise margin and reliability. The CMOS full adder suffers from large power consumption and high delay. New 14T full adder [4] based on simultaneous XOR-XNOR signals is an improvement from 14T full adder. However, it suffers from high delay. The feedback transistors need special attention, when sizing is done that increases the layout complexity. The TGA full adder [5] using 20 transistors is based on CMOS transmission gates and CMOS inverters. It provides full output voltage swing. In TFA [6], the design was improved with 16 transistors and maintains full output voltage swing operation. Complementary pass transistor logic (CPL) full adder [3] provides high speed and full swing operation. The presence of many internal nodes and inverters results in large power dissipation. The Hybrid pass logic (HPSC) full adders [7] with 22 transistors have poor PDP. For low supply voltages, the PDP rises drastically making them unsuitable for low-voltage operation. The hybrid CMOS style full adder [8] with 24 transistors has better noise immunity and performs well with low voltages. The proposed 8T full adder shows better results in terms of power, delay and PDP. It occupies less area in terms of transistor counts, more suitable for supply voltage scaling and under different load conditions.

III. PROPOSED 3T-XOR GATE AND FULL ADDER

The proposed new design of XOR logic gate using three transistors is shown in Figure-1. The design is based on modified CMOS inverter and PMOS pass transistor logic. When the input Y is at logic one, the inverter on the left functions as a normal CMOS inverter. Therefore the output

is the complement of input X. When the input Y is at logic zero, the CMOS inverter output is at high impedance. However, the PMOS pass transistor M3 is turned ON and the output gets the same logic value as input X. The operation of the whole circuit could be given as a 2 input XOR gate as given in Table-1.

Exact output logic levels are obtained for all the input combinations without any voltage degradation. However, when X=0 and Y=0, voltage degradation due to threshold drop occurs across the PMOS pass transistor M3 while passing the output logic zero and consequently the output is degraded with respect to the input. The voltage degradation due to threshold drop can be considerably minimized by increasing the W/L ratio of transistor M3 [9]. The equation (2) relates the threshold voltage of a MOS transistor to its channel length and width.

$$V_t = V_{t0} + g \left( \sqrt{V_{SB} + \phi_0} \right) - \alpha_1 \frac{t_{ox}}{L} (V_{SB} + \phi_0) - \alpha_v \frac{t_{ox}}{L} V_{ds} + \alpha_w \frac{t_{ox}}{W} (V_{SB} + \phi_0) \quad \text{---(2)}$$

where  $V_{t0}$  is the zero bias threshold voltage,  $g$  is bulk threshold coefficient,  $\phi_0$  is  $\phi_F$ , where  $\phi_F$  is the Fermi potential,  $t_{OX}$  is the thickness of the oxide layer and  $\alpha_1$ ,  $\alpha_v$  and  $\alpha_w$  are process dependent parameters. From equation (2) it is obvious that by increasing the width  $W$  of transistor M3, keeping the length constant it is possible to reduce the voltage degradation due to the threshold voltage. Typical values of transistor widths  $W_p = 3.0\mu m$  for PMOS M1,  $W_n = 1.5\mu m$  for NMOS M2, and  $W_p = 5.0\mu m$  for PMOS M3 have been taken. The length for all the transistors have been taken constantly as  $L = 0.09 \mu m$  (90 nm).

TABLE 1

LOGIC TABLE OF 3T XOR GATE

Input-A	Input-B	Output = $X'Y+XY'$
0	0	X/0
0	1	X'/1
1	0	X/ 1
1	1	X'/0

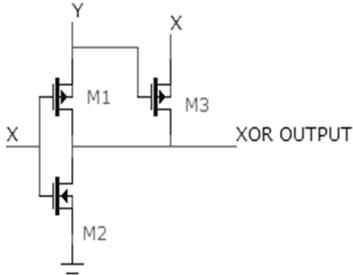
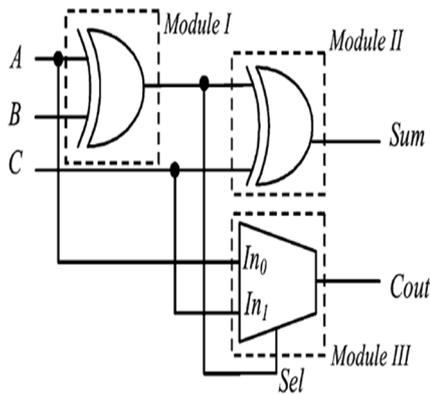
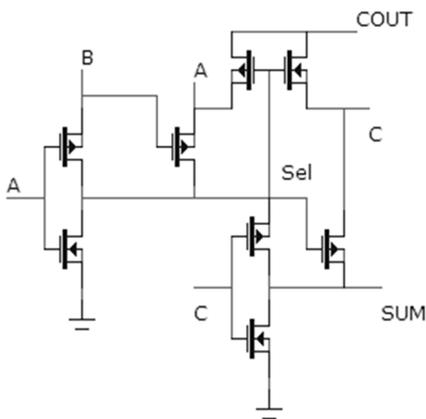


Fig 1. 3-Transistor based XOR



(a)



(b)

Fig 2. Full adder using two XOR gates and multiplexer (a) Block diagram (b) Circuit diagram

A. Full adder module

The full adder operation can be given as follows: Given the three 1-bit inputs A, B, and C, it is desired to calculate the two 1-bit outputs Sum and Carry, where  $Sum = (A \oplus B) \oplus C$  and  $Cout = A.B + X(A \oplus B)$ .

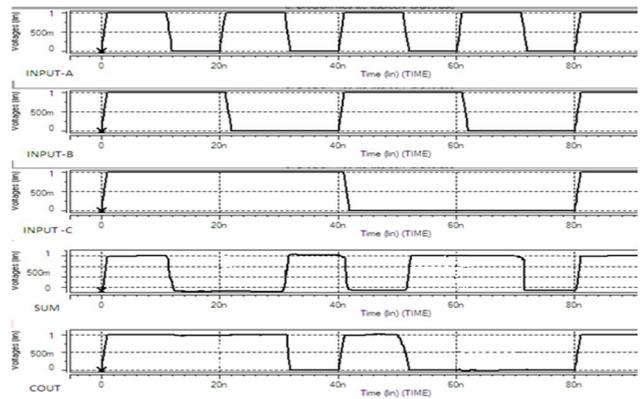
Full adder circuit can be implemented with different combinations of XOR, XNOR and 2x1 multiplexer blocks. The goal of this paper is to design a high performance and low power full adder module with 8T. Compared to the various logic structures, the proposed Full Adders embodies only 8 transistors and the number of interconnections between them is highly reduced. Having each transistor a lower interconnection capacitance, the power consumption is reduced to a great extent. The proposed 8T full adder is based on XOR/XOR logic constructed using two 3T XOR cells and one multiplexer as shown in block diagram of Figure-2(a). Two XOR gates generate the sum and 2T multiplexer block generate Cout. The 1-bit full adder with eight transistors has been implemented and shown in Figure-2(b). The typical values of width ( $W_n$  &  $W_p$ )  $1.5\mu m$  &  $3\mu m$  have been taken for NMOS and PMOS transistors respectively in the multiplexer block with gate length of  $0.09\mu m$ .

IV. RESULTS

In order to compare the results of the proposed full adder circuits with the existing full adders, a wide range of experiments was carried out. Schematics are designed for all the circuits using Custom Designer in Synopsys for TSMC  $0.18\mu m$  technology. Netlists obtained from the schematics are used to simulate and test performance. The original netlists are modified according to the process technology targeted using the Berkeley Predictive Technology Model (BPTM) 90nm process. The modified netlists are simulated using Synopsys HSPICE for power and delay estimations. The worst case power and delay measurements are made in all the cases.

Figure-3 (a) & (b) shows input and output waveform results for XOR cell and 8 transistor full adder respectively. The XOR and full adder circuits provide full swing output voltage with respect to sizing of transistors for threshold voltage degradation. Short circuit currents are also quite low in the XOR circuit as direct path from supply to ground is eliminated.

Full adder circuits discussed in [3] to [8] have been simulated and comparisons have been presented in Table-2. During the HSPICE simulation, for all the existing adders transistor width was taken as  $W_n = 1.5\mu\text{m}$  &  $W_p = 3\mu\text{m}$  with input voltage = 1V and transistor length  $L=0.09\ \mu\text{m}$ . Graph drawn in Figure-4 shows comparison of power and delay of proposed adder circuit with other adder circuits. It has been shown that proposed adder circuit show less power consumption and delay than previously reported adders. Proposed circuits also show superiority in terms of transistor count with earlier reported circuits. Proposed full adder has less internal capacitance as number of transistors is reduced and gives reduced power consumption.



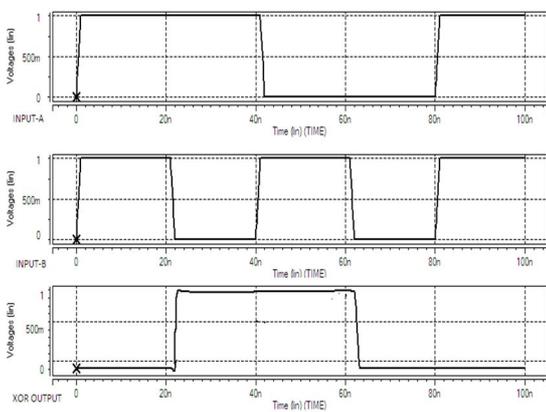
(b)

Fig 3. Input-Output waveforms with VDD=1V (a) proposed XOR circuit (b) 8T Full adder

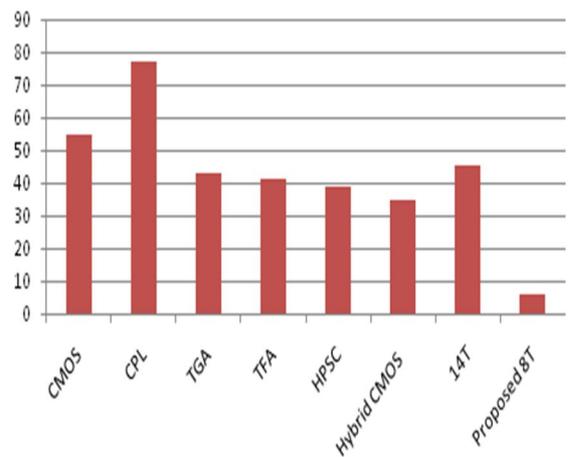
TABLE II

SIMULATION RESULTS FOR THE PROPOSED FULL ADDER CIRCUITS IN 90NM PROCESS TECHNOLOGY AT 50MHZ FREQUENCY

Adder	No. Of Transistors	Power(nW)	Delay(ps)	PDP( E-21 J)
CMOS	28	54.72	375.2	20530
CPL	32	76.82	462.8	35552
TGA	20	42.99	282.5	12144
TFA	16	41.02	297.1	12187
HPSC	22	38.83	539.8	20960
Hybrid CMOS	24	34.68	372.9	12932
14T	14	45.29	427.6	19366
Proposed 8T	8	5.87 Power(nW)	288.4	1692



(a)



(c)

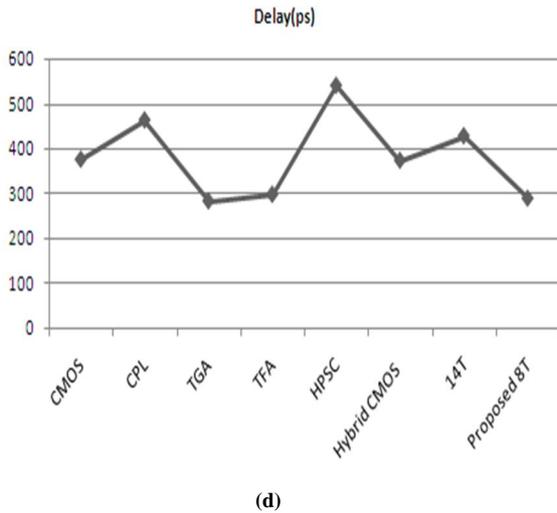


Fig 4. Comparison of (c) Power and (d) Delay for various Full adders

## V. CONCLUSION

In this paper, we have presented a systematic approach to construct full adder using only eight transistors based on new XOR cell. The proposed approach resulted in low power consumption and high speed compared to the existing full adder architectures. According to HSPICE simulation in 90 nm CMOS process technology at room temperature, and under given conditions, the proposed full adder shows an improvement of 89% average power consumption over conventional CMOS adder. In addition, the delay and power-delay product results depict impressive improvement over conventional CMOS adder.

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