SRF Based Cascaded Multilevel Active Filter

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Abstract - In this paper a power line conditioner using a cascaded multilevel inverter based shunt active filter using synchronous reference frame (SRF) controller is developed to improve the power quality in the distribution system . The cascaded multilevel inverter consists of two H-bridges in which each bridge has separate dc source. Gating signals to the cascaded multilevel voltage source inverter are generated from proposed triangular-carrier current controller. Here control strategy is different from conventional methods and provides superior performance. Using Reference Frame Transformation, the current is transformed from $a-b-c$ stationery frame to rotating $0-d-q$ frame. Using the PI controller, the current in the $0-d-q$ frame is controlled to get the desired reference signal. This proposed cascaded five level active power filter system is validated through MATLAB/SIMULINK Platform. From simulation results observed that the cascaded multilevel inverter based shunt active filter effectively compensates the current harmonics.

Keywords—Power line conditioner, Synchronous reference frame controller, triangular carrier current controller, power quality.

I. INTRODUCTION

Electric Power quality is a term which has captured increasing attention in power engineering in the recent years, the measure of power quality depends upon the needs of the equipment that is being supplied. What is good power quality for an electric motor may not be good enough for a personal computer. Usually the term power quality refers to maintaining a sinusoidal waveform of bus voltages at rated voltage and frequency. Nonlinear loads such as diode/thyristor rectifiers, switched mode power supply(SMPS), welding equipment, incandescent lighting, and motor drives are degrading power quality in transmission and distribution grid systems. These non-linear loads result in harmonic or distortion current and create reactive power problems. These harmonics induce malfunctions in sensitive equipment, overvoltage by resonance, increased heating in the conductors and harmonic voltage drop across the network impedance that affects power factor . Traditionally passive filters have been used to compensate harmonics and reactive power; but passive filters are large in size; aging and tuning problems exist and can resonate with the supply impedance.

. This paper present a novel synchronous reference frame controller based cascaded shunt active power filter for the harmonics and reactive power mitigation of the non-linear loads. The cascaded H-bridge active filter has been applied for power quality applications due to increase the number of voltage levels, low switching losses and higher order of harmonic elimination. The cascade M-level inverter consists of (M-1)/2 H-bridges and each bridge has its own separate dc source. The cascaded voltage source inverter switching signals are generated using proposed triangular periodical current controller; it provides better dynamic performance under both transient and steady state conditions. The compensation process is based on sensing load currents only, which require current harmonics and reactive power elimination due to the loads. The PI-controller is used to maintain the capacitance voltage of the cascaded inverter constant. The shunt APLC system is validated through extensive simulation and investigated under steady state and transient with different non-linear loads.

II. SHUNT ACTIVE FILTER

The waveform of electric power at generation stage is purely sinusoidal and free from any distortion. Many of the Power conversion and consumption equipment are also designed to function under pure sinusoidal voltage waveforms. However, there are many devices that distort the waveform. These distortions may propagate all over the electrical network.

In recent years, there has been an increased use of non-linear loads which has resulted in an increased fraction of non-sinusoidal currents and voltages in Electric Network. Classification of power quality areas may be made according to the source of the problem such as converters, magnetic circuit non linearity, arc furnace or by the wave shape of the signal such as harmonics, flicker or by the frequency spectrum (radio frequency interference). The wave shape phenomena associated with power quality may be characterized into synchronous and non synchronous phenomena. Synchronous phenomena refer to those in synchronism with A.C waveform at power frequency.

Recently Active Power Line Conditioners (APLC) or Active Power Filters (APF) overcome these problems and are designed for compensating the harmonics and suppressing the reactive power simultaneously. The controller is the most significant part of the APF topology and extensive research is being conducted to improve its control strategy. In 1979, FBD (Fryze-Buchholz-Dpenbrock) method is used in time domain and real time for compensating current harmonics. In 1984, H.Akagi introduced instantaneous active and reactive power theory method that is quite efficient for balanced three-phase loads, being later worked by Watanabe and Aredes for three-phase four wires power systems, zero sequence currents was later proposed by F.Z.Peng. In 1995, Bhattacharya proposed the calculation of the d-q components of the instantaneous three phase currents and this method creates a synchronous reference frame concept. The SRF method is consists of a phase locked loop (PLL) circuit and abc - dqo transformation;

it is a simple algorithm and good dynamic responses. The SRF is ability to compensate harmonics and reactive-power component from the distortion load currents.

Shunt active power filter compensate current harmonics by injecting equal-but-opposite harmonic compensating current. In this case the shunt active power filter operates as a current source injecting the harmonic components generated by the load but phase shifted by 180. This principle is applicable to any type of load considered a harmonic source. Moreover, with an appropriate control scheme, the active power filter can also compensate the load power factor. In this way, the power distribution system sees the non linear load and the active power filter as an ideal resistor. The current compensation characteristic of the shunt active power filter is shown in Fig1.

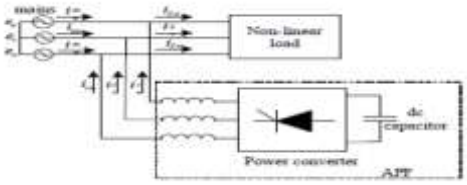

Fig.1. Basic Active Power Filter

Cascaded active filter for power line conditioning system is connected in the distribution network at the PCC through filter inductances and operates in a closed loop. Three phase active power filter comprises of 24-power transistors with freewheeling diodes; each phase consists of two-H-bridges in cascaded connection and every H-bridge having a dc capacitor. The shunt APLC system contains a cascaded multilevel inverter, RL-filters, a compensation controller (synchronous reference frame controller) and switching signal generator (triangular carrier current controller) as shown in the Fig2.

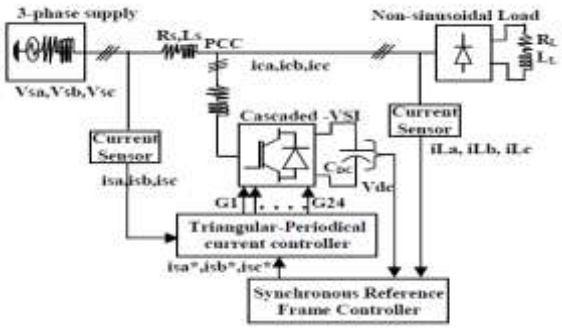

Fig.2. Shunt Active Power Line Conditioner system

The parallel active filter approach is based on the principle of injection of load harmonic currents and hence is characterized by non sinusoidal current reference tracking and high current regulator bandwidth requirement. The parallel active filter is controlled as a harmonic current source and requires a suitable controller for extraction of load harmonic currents and an appropriate current regulator.The nonlinear load current should contain fundamental component and harmonic current components. For harmonic compensation, the active filter must provide the compensation Current.

$$i_C(t) = i_l(t) - i_s(t)$$

III. MULTILEVEL INVERTERS

Multilevel converters have been introduced as static high-power converters for medium- to high-voltage applications such as large electric drives, dynamic voltage restorers, reactive power compensations, and FACTS devices. The multilevel converters synthesize a desired stepped output voltage waveform by the proper arrangement of the power semiconductor devices from several lower dc voltage sources. The main advantage of multilevel converters is the use of mature medium power semiconductor devices, which operate at reduced voltages. As a result, the switching losses and voltage stress on power electronic devices are reduced. Also, the output voltage has small voltage steps, which results in good power quality, low-harmonic components, and better electromagnetic compatibility. Multilevel converters have obtained more and more attention in recent years and new topologies with a wide variety of control strategies have been developed. There are three different basic multilevel converter topologies: neutral point clamped (NPC) or diode clamped, flying capacitor (FC) or capacitor clamped, and cascaded H-bridge (CHB).

The main drawback of the NPC topology is unequal voltage sharing between the series connected capacitors, which leads to dc-link capacitor unbalancing and requires a great number of clamping diodes for a high number of voltage levels. Also, the maximum voltage across the switches is closest to the switching node. Therefore, the three-level NPC converter has been commercialized in industry as a standard topology. The FC multilevel converter, and its derivative, the stacked multilevel (SM) converter and, use flying capacitors as clamping devices. These topologies have several attractive properties compared to NPC converters, including the advantage of transformer-less operation and have redundant phase leg states that allow the switching stresses to be equally distributed among semiconductor switches. But, these converters require an excessive number of storage capacitors for a high number of voltage steps.

A double FC multi-cell converter has been presented. This topology has been implemented by adding two low-frequency switches to the conventional configuration of the FC multilevel converter. The main advantages of the presented converter, in comparison with the FC multilevel and SM converters, are the doubling of the rms value of the output voltage and the number of output voltage steps and the canceling of the midpoint of the dc source. But two additional switches must operate at the peak of the output voltage. This restricts high-voltage applications of this converter.

The CHB topologies are a good solution for high-voltage applications due to the modularity and the simplicity of control. But, in these topologies, a large number of separated voltage sources are required to supply each conversion cell. To reduce the number of separate dc voltage

sources for high-voltage applications, new configurations have also been presented; however, a capacitor-voltage balancing algorithm is required

A cascaded multilevel active power inverter is constructed by the conventional of H-bridges. The three phase active filter comprises of 24power transistors and each phase consists of two H-bridges in cascaded method for 5-level output voltage, shown in Fig 3.

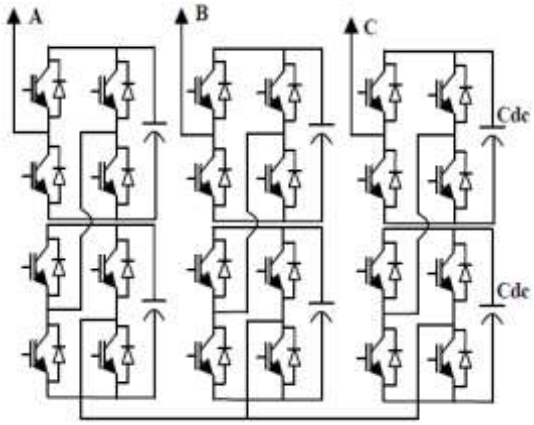

Fig.3. Cascaded Multilevel Inverter

Each H-bridge is connected a separate dc side capacitor and it serves as an energy storage elements to supply a real power difference between load and source during the transient period. The capacitor voltage is maintained constant using PI-controller. Each H-bridge can produce three different voltage levels + Vdc , 0, - Vdc by four switching operations. The ac output of the each H-bridge is connected in series such that the synthesized output voltage waveform is the sum of all the individual H-bridges.

The 24-IGBT switching operations are performed using proposed triangular carrier current modulator and harmonics it is achieved by injecting equal but opposite current harmonic components at a point of common coupling (PCC).

IV. CONTROL STRATEGIES

The proposed control system consists of reference current control strategy using SRF method and triangular current controller for switching signals of cascaded VSI.

A. Synchronous Reference Frame Control Strategy:

The synchronous reference frame theory is developed in time-domain based reference current generation techniques. The SRF is performing the operation in steady-state or transient state as well as for generic voltage and current; it's capable of controlling the active power filters in real-time system. Another important characteristic of this theory is the simplicity of the calculations, which involves only algebraic calculation. The block diagram of the synchronous reference frame controller is shown in Fig 4.

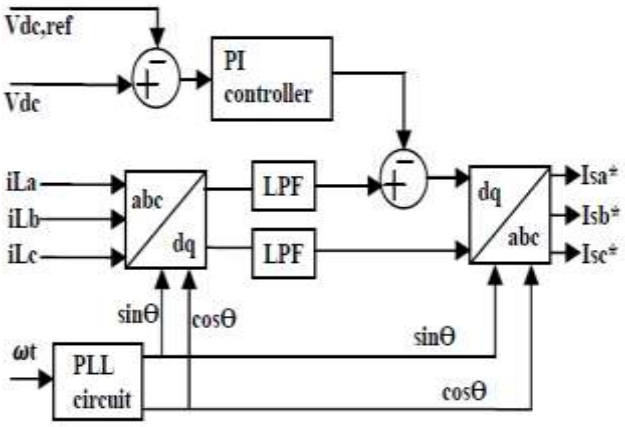

Fig.4. Synchronous Reference Frame Controller

B. PI- Controller:

Figure 5 shows the block diagram of the proportional integral control scheme for the active Power filter The DC side capacitor voltage is sensed and compared with a desired reference voltage.

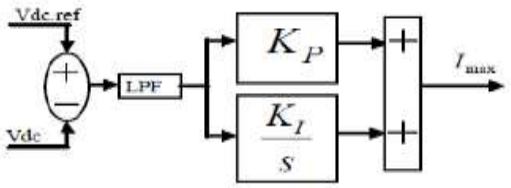

Fig.5. PI - Controller

The voltage error $e = V_{dc,ref} - V_{dc}$ at the n^{th}sampling instant is used as an input for PI controller. The error signal passes through Butterworth Low Pass Filter (LPF). The LPF filter has cutoff frequency at 50 Hz that can suppress the higher order components and pass only Fundamental components. The PI controller estimates the magnitude of peak reference current *I* max and controls the dc side capacitor voltage of cascaded multilevel inverter. It transferred by the function which is represented as,

$$H(S) = K_p + \frac{K_i}{S}$$

C. Operation of SRF Controller:

The reference frame transformation is formulated from a three-phase $a - b - c$ stationery system to the two phase direct axis (d) – quadratic axis (q) rotating coordinate system. In a-b-c stationary axes are fixed on the same plane and separated from each other by 120o. These three phase space vectors stationary coordinates are easily transformed into two axis d-q rotating reference frame. This proposed algorithm derivate from a three-phase stationary coordinate load current i_{La}, i_{Lb}, i_{Lc} are convert to id-iq rotating coordinate current, as follows

$$i_d = \frac{2}{3}\left[i_{La}\sin\omega t + i_{Lb}\sin\left(\omega t - \frac{2\pi}{3}\right) + i_{Lc}\sin\left(\omega t + \frac{2\pi}{3}\right)\right]$$

$$i_q = \frac{2}{3}\left[i_{La}\cos\omega t + i_{Lb}\cos\left(\omega t - \frac{2\pi}{3}\right) + i_{Lc}\cos\left(\omega t + \frac{2\pi}{3}\right)\right]$$

The d-q transformation output signals depend on the load currents (fundamental and harmonic frequency components) and the performance of the phase locked loop. The PLL circuit of rotation speed (rad/sec) of the rotating reference frame ωt set as fundamental frequency component. The PLL circuit is providing sinΘ and cosΘ for synchronization. The id-iq current passed through low pass filter (LPF) for filtered the harmonic components and allows only the fundamental frequency components. The LPF design is based on Butterworth method and the filter order is 2. The band edge frequency is selected the fundamental of 50 Hz for eliminate the higher order harmonic components. Proportional Integral (PI) controller is used to eliminate the steady state error of the DC-component of the cascaded multilevel inverter and maintains the dc-side capacitor voltage constant. The dc capacitor voltage is sensed and compared with reference voltage for calculate the error voltage. These error voltage involved the P-I gain (KP=0.1 and KI=1) for regulate the capacitance voltage in the dynamic conditions. In accordance to the PI controller output is subtracted from the direct axis (d axis) of harmonic component for eliminate the steady state error. The algorithm is further developed to the desired reference current signals in d-q rotating frame is converted back into $a - b - c$ stationery frame. The inverse transformation from $d - q$ rotating frame to a$- b - c$ stationery frame is achieved by the following equations

$$i_{sa}^* = i_d \sin\omega t + i_q \cos\omega t$$
$$i_{sb}^* = i_d \sin\left(\omega t - \frac{2\pi}{3}\right) + i_q \cos\left(\omega t - \frac{2\pi}{3}\right)$$
$$i_{sc}^* = i_d \sin\left(\omega t + \frac{2\pi}{3}\right) + i_q \cos\left(\omega t + \frac{2\pi}{3}\right)$$

The reference frame is rotates synchronous with fundamental currents. Therefore, time variant currents with fundamental frequencies would be constant after transformation. Thus, currents would be separated to DC and AC components. AC components of d-axis and in q-axis current are used for harmonics elimination and reactive power compensation.

D. Triangular Carrier Current Controller:

The triangular carrier current controller is one of the familiar methods for active power filter applications to generate gate control switching pulses of the voltage source inverter. To determine the switching transitions by means the error current [desired reference current (i_{sa}^*) compared with the actual source current(i_{sa})] is multiplied with proportional gain (Kp). The output signal of the proportional gain is compared with triangular carrier signal.

The four triangular signals are generated same frequency with different amplitude for cascaded multilevel inverter, because each phase in one converter does not overlap other phase shown in Figure 6. Thus the switching frequency of the power transistor is equal to the frequency of the triangular carrier signal.

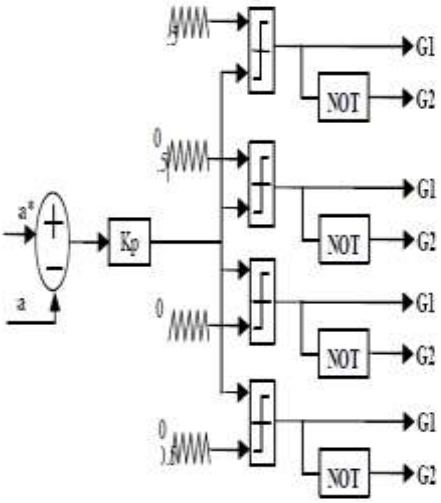

Fig.6. Triangular Carrier Current Controller

V. SIMULATION RESULTS

The performance of the proposed SRF controller based cascaded active filter is evaluated through Matlab/Simulink power tools.

Here the simulation is carried out by two cases

a. Non-linear load Without Filter
b. Non-linear load with SRF based five level cascaded multilevel APF.

The system parameters values are shown in table 1.

TABLE 1

SYSTEM PARAMETERS AND VALUES

Parameters	Values
Line to Line Source Voltage	440 V
System Frequency	50 Hz
Source Impedance of Ls	3mH
Filter impedance of Rc , Lc	0.1 Ω ; 1 mH
Diode Rectifier RL,LL Load	20 Ω ; 100 mH
DC side Capacitance (Cdc)	2100 µF
Reference Voltage (Vdc,ref)	700 V

Fig.7 shows the three phase source currents respectively without and with APF.

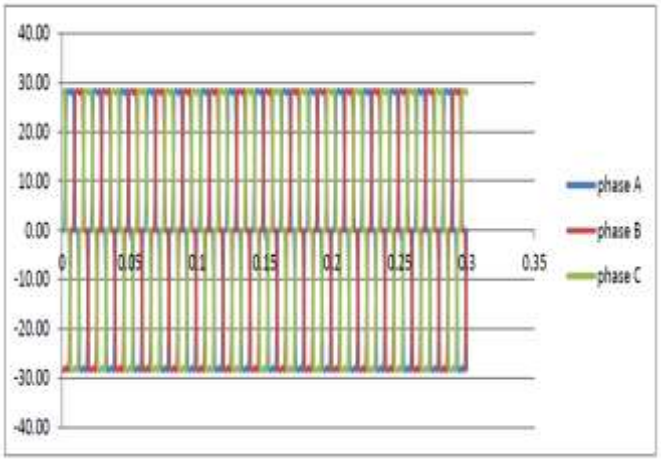

Fig.7.1. 3-Phase Source Current without APF

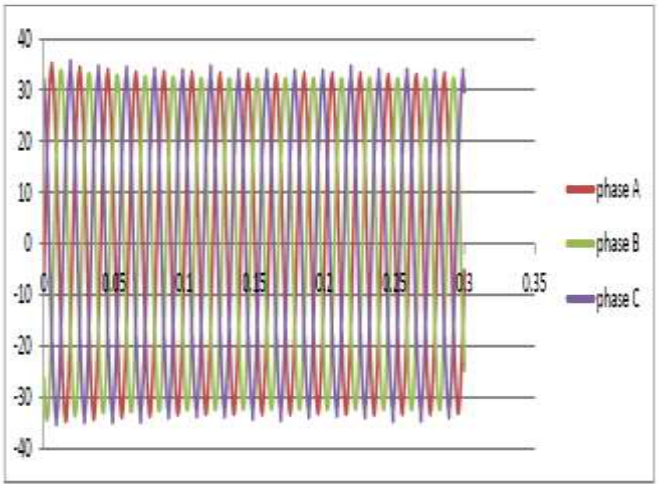

Fig.7.2. 3-Phase Source Current with APF

Fig.8 shows the three phase load currents respectively without and with APF. It is clear that with Active power filter load current are same

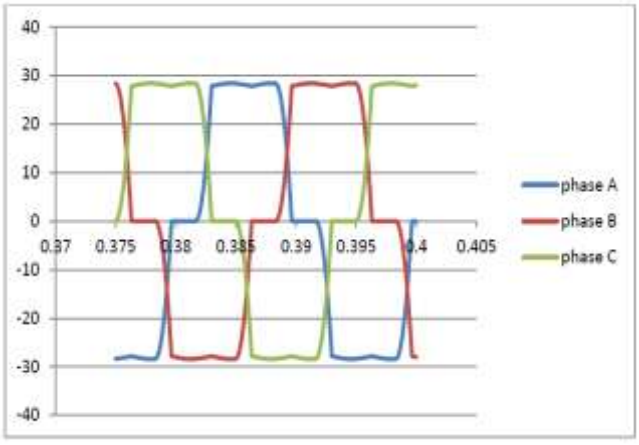

Fig.8.1. 3-Phase Load Current without APF

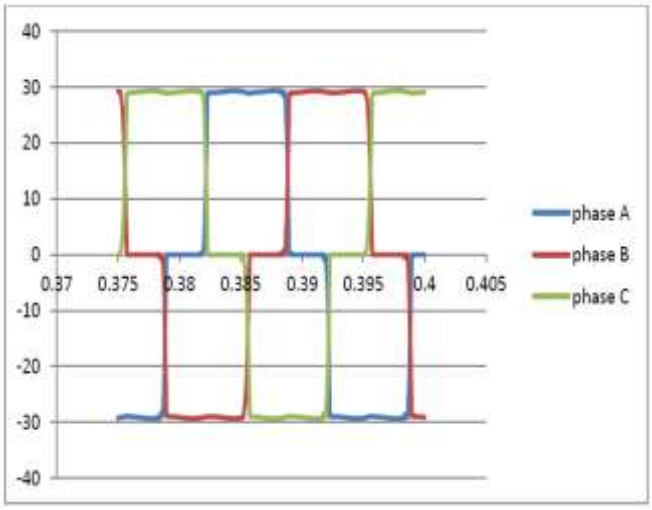

Fig.8.2. 3-Phase Load Current with APF

The active filter must provide the harmonic filter current or compensation current as, shown in Fig 9.

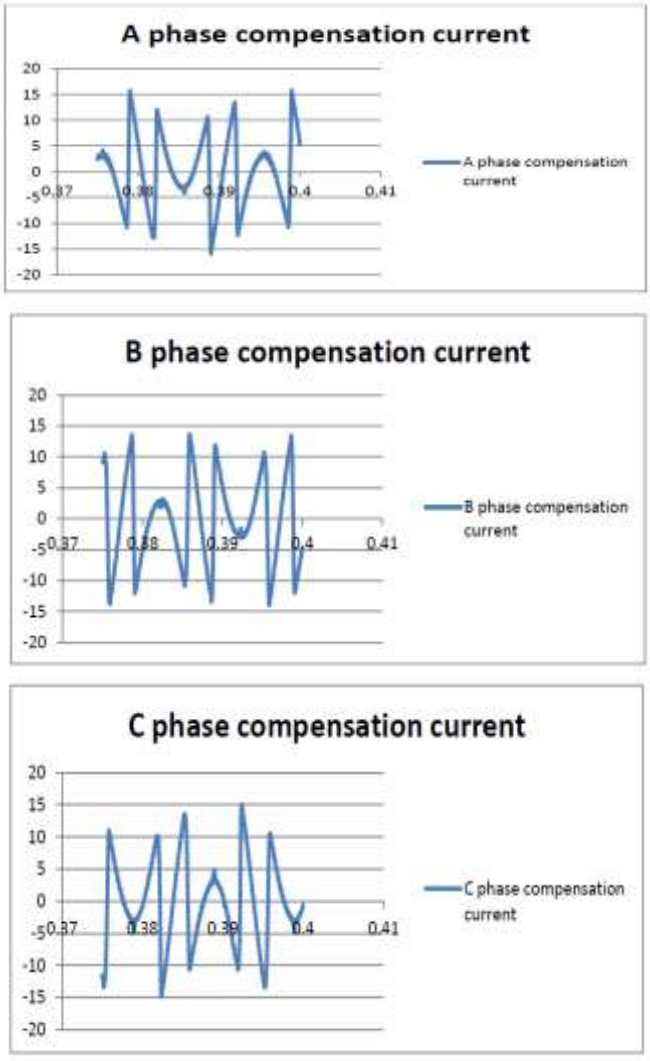

Fig.9. Compensation Current

The reference fundamental current is extracted from the loads using the proposed SRF controller is shown in Fig10.

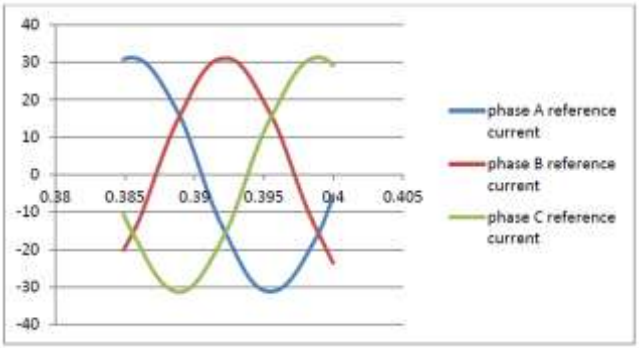

Fig.10. Extracted Reference current from loads using SRF

The DC-side capacitors voltage is controlled by PI-controller that is shown in Fig 11. It serves as an energy storage element to supply a power to operate three phase cascaded multilevel inverter.

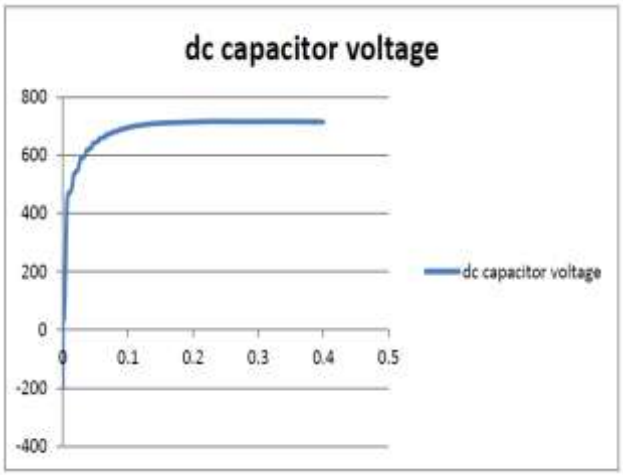

Fig.11. DC- side Capacitor Voltage

Fig 12 shows the power factor waveform without and with compensation

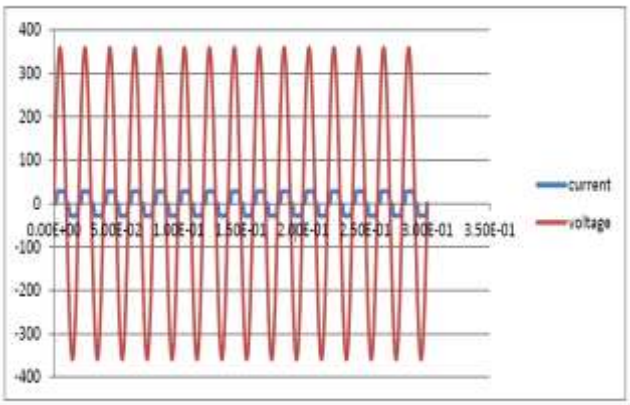

Fig.12.1. Power factor without Compensation

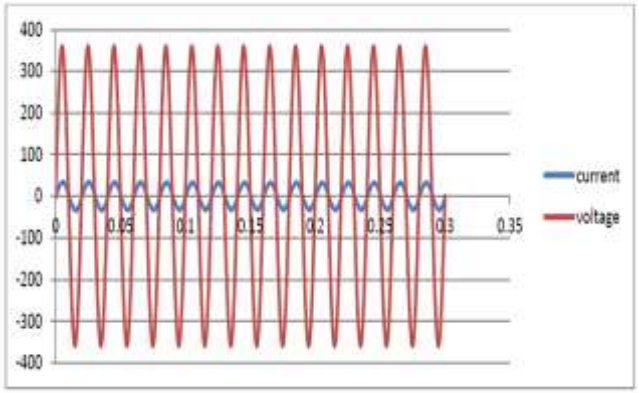

Fig.12.2. Power factor with Compensation

Fig 13 shows the Active and Reactive power waveform without and with compensation

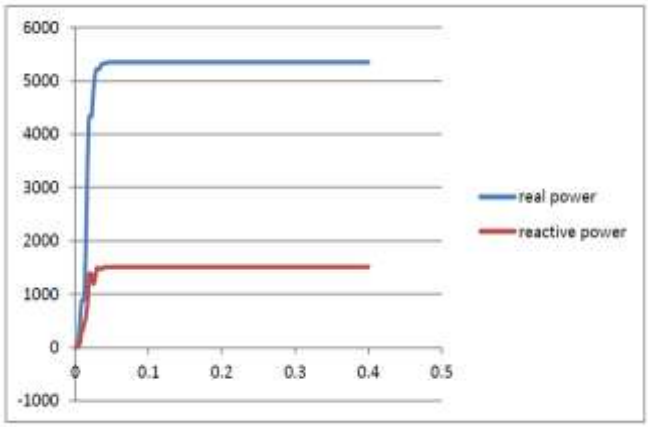

Fig.13.1. Active and Reactive power without Compensation

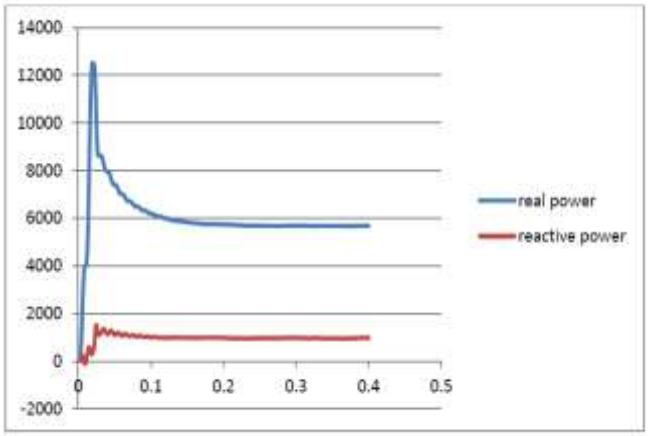

Fig.13.2. Active and Reactive power with Compensation

The Fast Fourier Transform (FFT) is used to measures the order of harmonics with the fundamental frequency at 50 Hz for the source current that is shown in Fig14.

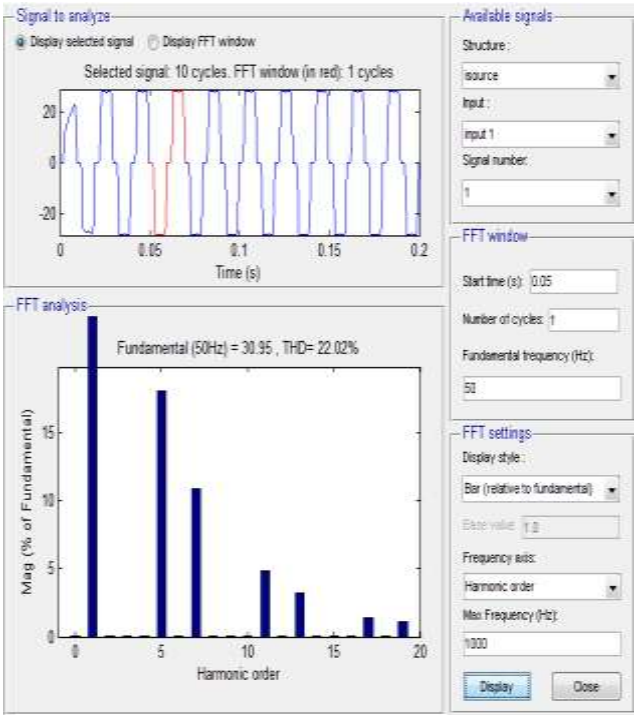

Fig.16.1. Order of harmonics , Source current without APF (THD=22.02%)

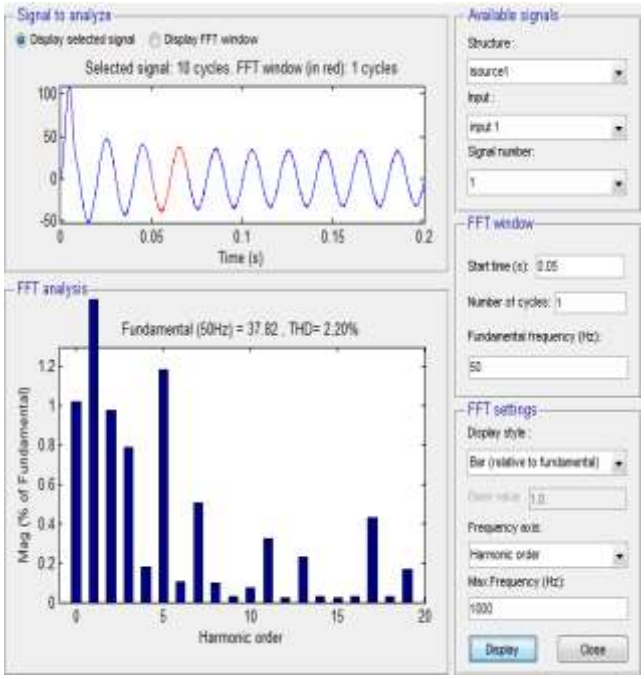

Fig.16.2. Order of harmonics , Source current with APF (THD=2.20%)

The total harmonic distortion (THD) measured at the source(current) on the distribution system and the various parameters measured without APF and with APF are presented in Table 2

TABLE 2
Various parameters measured without APF and with APF

Parameters	Source Current Without APF	Source Current With APF
THD	22.02 %	2.20%
Active Power	5350 W	5731 W
Reactive Power	1512 VAR	982 VAR
PF	0.9623	0.9856

The SRF based cascaded active filter simulation is done with various non-linear load conditions. FFT analysis indicates that the active filter brings the THD of the source current to 2.20 %.

VI. CONCLUSION

This paper indicates the suitability of cascade multilevel inverter based active filter for power line conditioning of distribution networks. The cascaded inverter provides lower cost, higher performance and higher efficiency than the traditional PWM-inverter for power line conditioning applications.

The cascaded inverter switching signals are derived from the proposed triangular-periodical current modulator that provides good dynamic performance under both transient and steady state operating conditions.

SRF is employed to extract the fundamental component from the nonlinear load currents. This controller is developed by sensing load currents only. This approach is fairly simple to implement and is different from conventional methods.

The PI-controller maintains the capacitance voltage of the cascaded inverter nearly constant. The extensive simulation results demonstrate the performance of the APF under different non-linear load conditions.

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