# A 1.8GHz Differential Low Noise Amplifier for Wireless Receivers

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***Abstract*— In this paper the Differential Low Noise Amplifier (DLNA) operating with a center frequency of 1.748GHz is designed using 0.35µm CMOS technology. The Differential Low Noise Amplifier provides a Gain of 25.5dB with a noise figure of 1.3. The DLNA is designed using inductive source degeneration architecture.**

***Keywords:- D*LNA, CMOS, Gain, Noise figure.**

## I. INTRODUCTION

In a wireless receiver the information being transmitted is either data or voice which is used to change a radio frequency (RF) carrier. In RF front end design the first stage is a LNA. CMOS has become a competitive technology for radio transceiver implementation of various wireless communication systems due to high cut off frequency, higher level of integrability, lower cost, etc[2]. The main advantage of using CMOS for RF frontends is ease of integration with digital section leads to whole system on a single chip. LNA plays an influential role in determining the noise figure of a microwave receiver as it is the first component of the receiver front-end placed just after the receiving antenna[3]. As the gain provided by the LNA increases the overall noise figure of the receiver reduces correspondingly. For a receiver high gain is required when the received signal is very weak. So the LNA has to provide high gain, good input and output matching and very low power consumption. Moreover, the differential topology improves the performance by providing better rejection of common mode noise, less sensitivity to substrate and power supply noise, improved power supply rejection ratio and higher linearity[7]. Aside from providing enough gain while adding as little noise as possible, an LNA should accommodate large signals without distortion, it should have a large dynamic range, and good matching to its input and output, which is extremely important if a passive bandselect filter and image-reject filter precede and succeed the DLNA, since the transfer characteristics of many filters are quite sensitive to the eminence of the termination. In general the performance of a receiver depends on the LNA gain and noise figure. In addition the standard used for implementation of communication system is low data rate, low power and usually each node is operated with battery. So the design of LNA is aimed at lower power utilization. This paper organized as, section 2 presents DLNA design, section 3 gives simulation results and discussion.

## II. DLNA DESIGN

There are several advantages in using a differential LNA. The key features are the virtual ground formed at the 'tail' eliminates the sensitivity to parasitic ground inductances, which makes the actual part of the input impedance purely controlled by the source degeneration inductance ($L_s$). The differential amplification of the signal ensures reduction of the common mode signal, in most of the systems this common mode signal will be noise. Differential Low noise amplifier is designed using 0.35µm CMOS technology with a center frequency of 1.748Ghz. DLNA is designed with source degeneration configuration. The design is done using Advanced Design System. Fig. 2 shows the schematic of Differential Low Noise Amplifier design. The design equations for the DLNA is given below.

$$L_s = \frac{R_s}{\omega_T} = 0.5nH \qquad (1)$$

Where Ls is the source inductance, Rs is the source resistance and $\omega_T$ is the cut off frequency.

$$C_{ox} = \frac{\mathcal{E}_{ox}}{T_{ox}} = 4.6mF \qquad (2)$$

$$\mathcal{E}_{ox} = \mathcal{E}_s . \mathcal{E}_o \qquad (3)$$

Where $C_{ox}$ is the oxide layer capacitance, $\mathcal{E}_s$ is the dielectric constant for silicon and $\mathcal{E}_o$ is the permittivity of free space. $T_{ox}$ is the gate oxide thickness. The minimum length of the transistor is taken as 0.35µm.

$$W = \frac{1}{{\omega_0}^2 L_{min} C_{ox} R_s} = 350\mu m \qquad (4)$$

Where W is the width of the transistor, $L_{min}$ is the minimum length of the transistor and $\omega_0$ is the center frequency. The differential input voltage is supplied via the balun transformer (CMP1). An ideal current source has been added at this stage on the 'tail'.The two output nodes V1 & V2 are now terminated in 50-ohm loads. The width of the transistor is optimally sized to be 350µm and the length of the transistor is 0.35 µm . The design specifications are tabulated below in table 1.

TABLE I
DESIGN SPECIFICATIONS

| Parameter | Specification |
|---|---|
| Topology | Differential LNA |
| Frequency | 1800MHz |
| Center Frequency | 1.748GHz |
| Channel Bandwidth | 75 MHz |
| Length | 0.35 µm |
| Width | 350 µm |
| DC voltage | 3.15V |
| Ls | 0.5nH |
| Cox | 4.6mF |
| $L_D$ | 8.2nH |

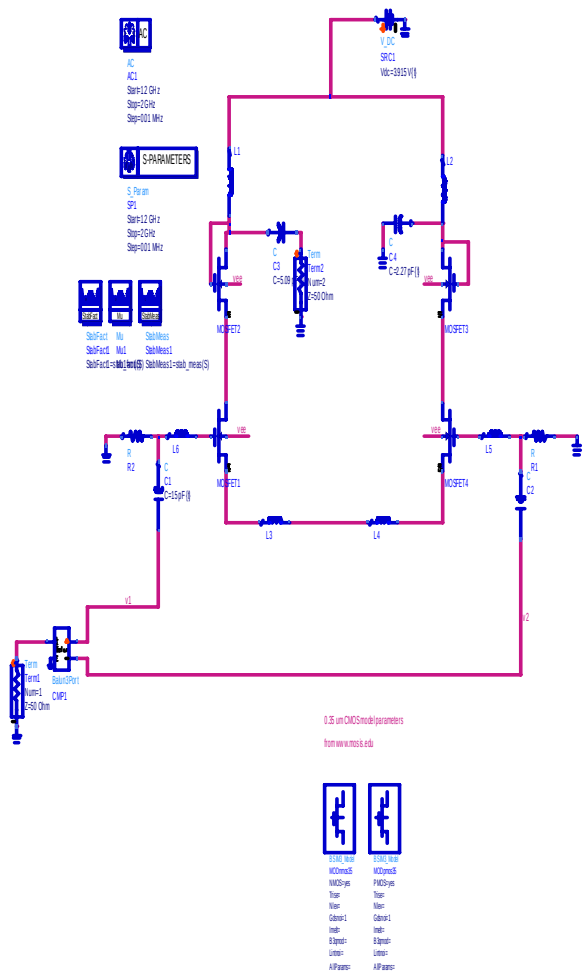


Fig. 2. ADS Schematic for Differential Low Noise Amplifier Design

The design specifications for Differential Low Noise Amplifier include center frequency, Channel Bandwidth, Length and width of the transistor. The gain and Noise figure plays an important role in Differential Low Noise Amplifier design. The Noise Figure must be less the 2.5dB and Gain must be greater than 20dB. The designed Low Noise Amplifier provides a gain of 25.70 dB and a Noise Figure of 1.07. the formula for gain and Noise figure is given in the equation (5) and (6)

Gain=20*log(Vout/Vin) (5)

Where Vin and Vout are respective input and output voltage.

Noise is measured in terms of Noise Figure as a function of frequency. Noise figure is the measure of degradation of the Signal to Noise Ratio (SNR) caused by the component of Radio Frequency signal chain.

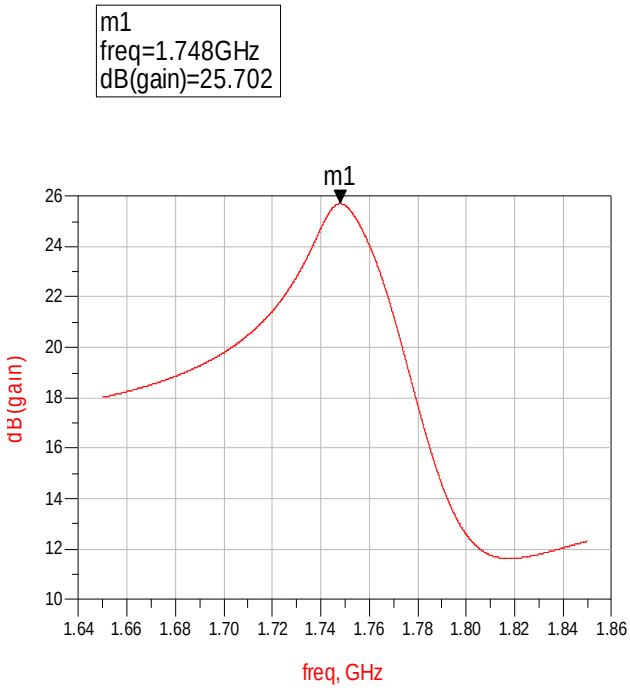
Noise Figure(NF)= SNRi/SNRo (6)

Where SNRi is the SNR in dB at input of the Low Noise Amplifier and SNRo is the SNR in dB at the output of the Amplifier. A balun is used at the input to convert the single ended signal from the antenna to a differential ended signal. The simulation is done using Advanced Design System software.

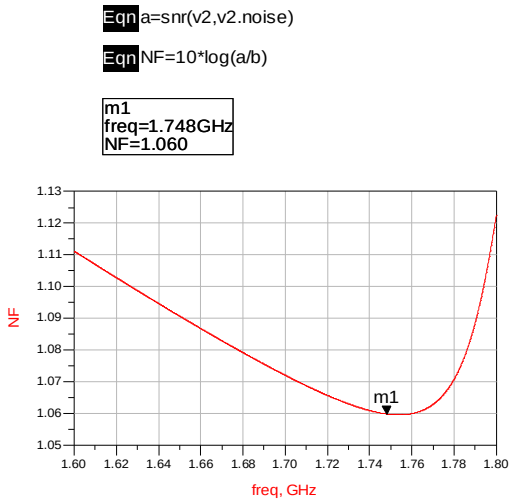
## III. SIMULATION RESULTS

### *A. AC Simulation*

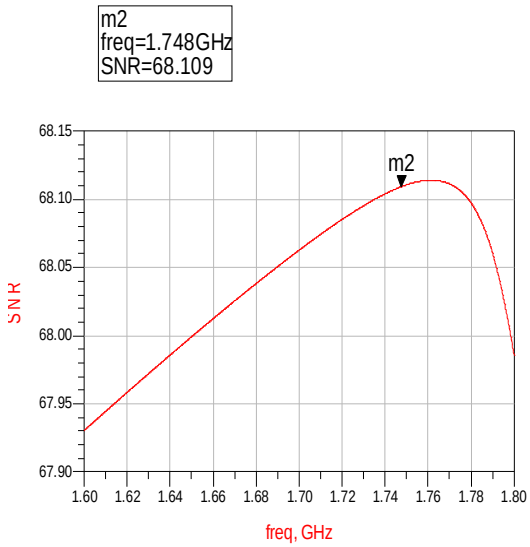
AC simulation is done to find out the Gain Noise figure and Signal to Noise Ratio. Noise figure must be low at the designed frequency, Gain and SNR should be high at the designed frequency.




(a) Gain




(b)Noise figure




(c) SNR

Fig.3. (a)Gain, (b)NF,(c) SNR of Low Noise Amplifier

Fig. 3. shows Gain, Noise Figure and SNR of a low Noise Amplifier. The designed Low Noise Amplifier has a gain of 25.7dB, Noise figure of 1.060dB and Signal to Noise ratio of 68.10.The center frequency of operation is 1.748GHz. The designed Differential Low Noise Amplifier gives high gain and low Noise Figure at the center Frequency.

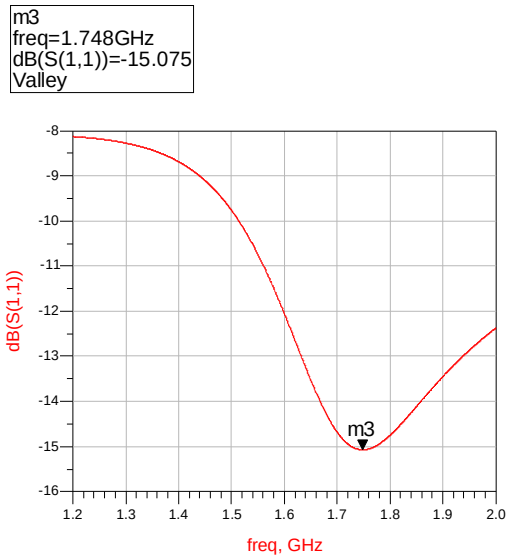
*B. S parameter simulation*

S-Parameter simulation is performed to find the return loss and stabilty factor. K greater than one implies the circuit is unconditionally stable for the designed frequency. Rolette Stability factor(K) is given by the equation (7)

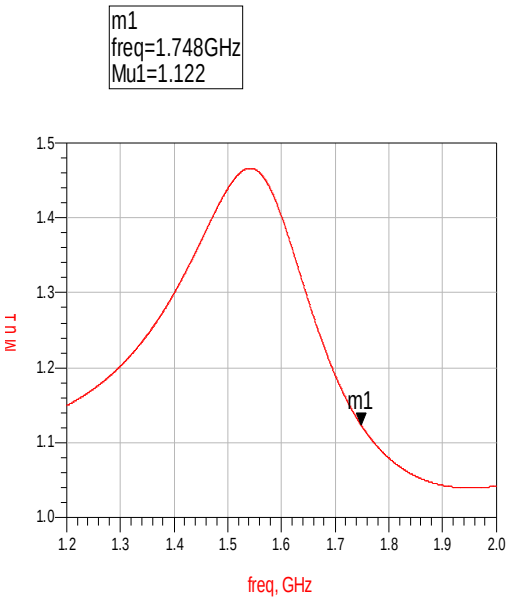
$$K = \frac{1+|\Delta|^2-|S_{11}|^2-|S_{22}|^2}{2|S_{12}S_{21}|} \quad (7)$$

Where $\Delta = | S_{11} S_{22} - S_{12} S_{21} | < 1$

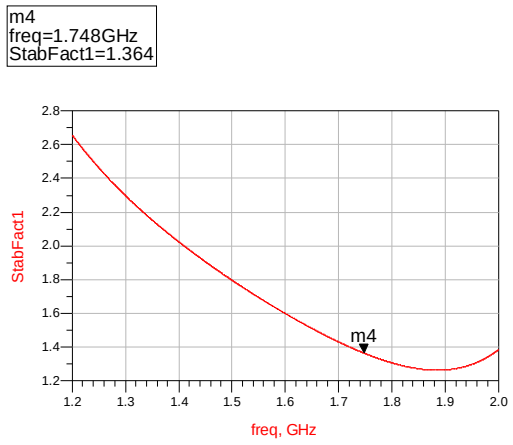
When K-factor is greater than one, the circuit will be unconditionally stable for any combinations of source and load impedance.



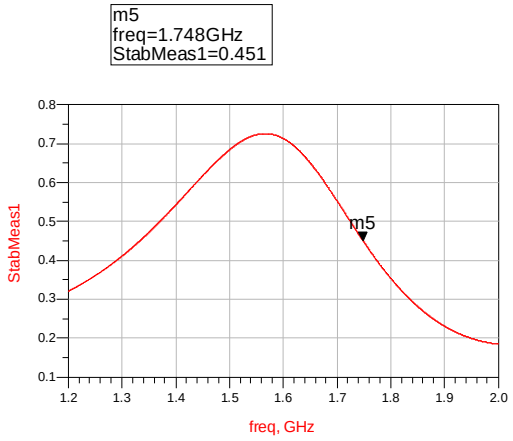

(a)Return loss( S11)




(b)Stability factor(μ)




(c)Stability factor(K)




(d)Stability measure(Δ)

Fig.4. S parameter Simulation of Differential Low Noise Amplifier

Fig. 4. shows the S parameter simulation results for DLNA, the Return loss ($S_{11}$)for the designed DLNA is -15.075dB, stability factor K is 1.364 which is greater than one. The stability measure (Δ) is 0.045 which is less than one. This implies the designed circuit is unconditionally stable for the designed frequency.

## IV. CONCLUSION

Differential Low Noise Amplifier is designed using 0.35µm CMOS technology for 1800MHz band wireless receiver. The design has been done using Advanced Design System Software. The designed Differential Low noise Amplifier provides a gain of 25.07dB, Noise Figure of 1.07dB and a SNR of 68.109.

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