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Implementation of Frequency Down Converter using Multiplier free filter on FPGA

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Abstract — **In a Communication system, especially in some applications where confidential data is to be communicated, wideband of signals are used. Also the bandwidth of the signal is frequently varied so that it is undetectable by the third person. In such cases to detect the signal a Wideband DDC with variable filter specifications is required. In this paper, an efficient way of designing and implementing a Wideband Digital down Converter has been discussed. Though the received signal is RF signal with high data rates an IF stage is used to frequency shift the signal to fixed IF which is the input to ADC. This is sampled and given as input to DDC. Signal extraction using DDC is presented in detail. It is shown that filter bandwidth varies by varies with decimation factor. Decimation range in this paper is 2 to 16384. Filtering is implemented in stages to obtain efficient response. Also, the reasons for choosing FPGA over ASSP's to implement DDC are provided. Xilinx ISE 10.1 version software is used for simulating each block of DDC at system level testing and Chip Scope Pro Analyzer tool is used for board level testing. Vitex-5 FPGA with speed -2 is the hardware used for implementing the design.**

Keywords — **Wideband Digital down converter, ADC, Baseband signal, Decimation, ASSP, FPGA, System level testing, Board level testing.**

I. INTRODUCTION

Communication plays vital part in day to day life for transfer of information. Though there are different modes of communication, at present Digital communication is more popular. It is a process of transferring signals, in digital format i.e., as bits. A transmitter, channel and a receiver are the main blocks of a communication system. The DDC presented in this paper is the key component of Receiver. The digital IF signal from ADC is given as input to DDC. The speed of the ADC depends on the band of interest as the Nyquist's theory states that the signal should be sampled at a rate "at least double the bandwidth of interest". A DDC allows the frequency band of interest to be moved down the spectrum to baseband signal near to 0Hz such that further processing on the signals become easier. Later techniques are involved for varying the filter specifications to extract the signal of interest.

The remainder of this paper is structured as follows: Section 2 provides an overview of Digital Down Converter. Section 3 mentions the steps involved in converting IF signal to base band signal. Section 4 is about filtering and decimation. Section 5 gives a detailed explanation on implementing the design on FPGA. Section 6 provides Simulation results and the last section gives the conclusion of the paper.

II. OVERVIEW OF DDC

Down Conversion involves the process of shifting a high rated signal to a standard signal. Generally the receivers receive wide band of signals but the end user may only require a small portion of the entire band. So fulfilling the above requirement might involve prohibitively large filters. A variable decimation DDC makes this process easier.

A DDC consists of five basic blocks

i. DDS (Direct Digital Synthesizer)
ii. Mixer
iii. CIC (Cascaded integrate comb)
iv. CFIR (Compensation FIR) filter
v. PFIR (Programmable FIR) filter

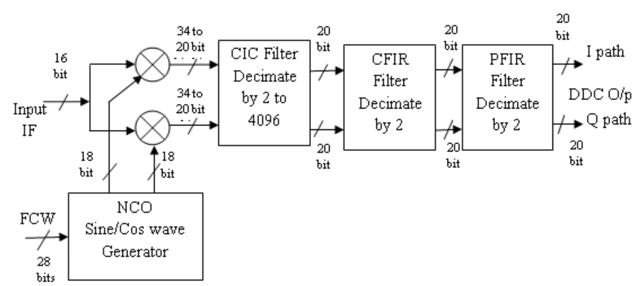

Fig. 1 Practical Implementation of DDC

A. Fixed point Representation for real numbers

In Digital Signal Processing the numbers are represented as bits. Most commonly real numbers are used for computations, i.e., numbers with fractional part. So to represent these real numbers fixed point data type can be used for faster computations rather than fractional point arithmetic. It represents fractional values, usually in base 2 or base 10. In this project work base 2 (binary) representation is used. All digits (or bits) to the left of the binary point carries a weight of 2^0, 2^1, 2^2, and to the right of binary point carries a weight of 2^{-1}, 2^{-2}, 2^{-3}, and so on.

B. Signed 2's complement

A fixed point number (an integer) X can be represented by signed 2's complement, defined as:

- When X > = 0, MSB = 0 represents the plus sign, and the remaining n-1 bits represent the magnitudes in the range $0 \leq X \leq (2^{n-1} - 1)$.
- When X < 0, MSB = 1 represents the minus sign, and the remaining n-1 bits represent the magnitude in the range $-2^{n-1} \leq X \leq -1$.

The MSB is thus used as the sign-bit to indicate whether the number is positive or negative. Thus the overall range for Signed-Complement representation is $-2^{n-1} \leq X \leq (2^{n-1} - 1)$.In some computations like multiplications the result may have more number of bits than the storage capacity of the output register. In that case the bits are to be truncated or rounded. To avoid more information loss MSBs of integer value and LSBs of fractional value are truncated.

III. CONVERSION TO BASEBAND

The signal received from the antenna is difficult to process further as it consumes complex hardware. So this Radio Frequency (RF) signal is to be converted to Intermediate Frequency (IF) signal, later it is frequency shifted to baseband.

A. Direct Digital Synthesizer

A Direct Digital Synthesizer also called Numerically Controlled Oscillator generates a complex sinusoid at the intermediate frequency. It provides a flexible architecture which enables easy programmability such as on-the-fly frequency/phase. A sine wave can be generated by rotating a vector around the phase circle [4].

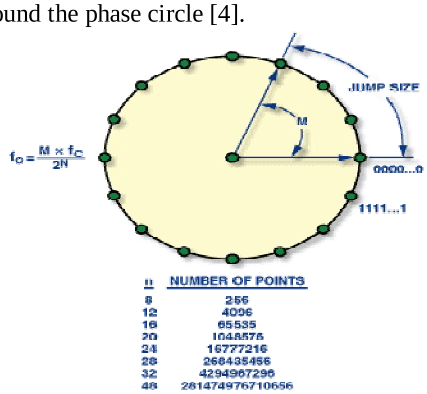

Fig. 2 Principle of NCO

An NCO generally consists of two parts [5]:

- A **phase accumulator** (PA), that adds a frequency value also called tuning frequency (Δf) to its previously stored value at each clock pulse. This word forms the phase step size between reference-clock updates; it effectively sets how many points to skip around the phase wheel. Tuning frequency is obtained by using the below formula.

$$F_{out} = \frac{\Delta f}{2^N} \cdot f_{clk}$$

- A **phase-to-amplitude converter** (PAC), which uses the N-bit output from the PA (phase word) usually as an address into a waveform look-up table (LUT) to provide corresponding amplitude of sine wave. The output value at the phase-to-amplitude converter may be expressed by

$$x(n) = \sin\left(2\pi \frac{\varphi(n)}{2^N}\right)$$

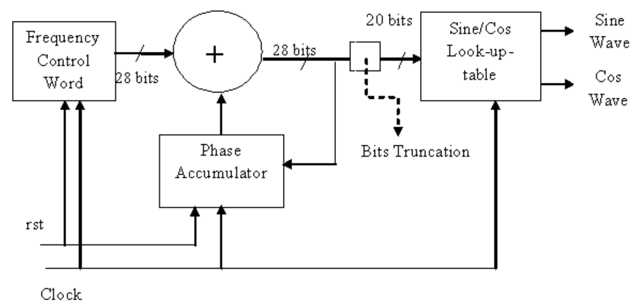

Fig. 3 Numerically Controlled Oscillator

B. The Mixer

A mixer is used to convert the IF signal to baseband signal by multiplying the input signal with complex sinusoidal signal cos (wt)-*j* sin(wt) = e-jwt which is generated by NCO thus giving two signals as output which are 90 degrees out of phase with each other i.e.;

i. In-Phase signal
ii. Quadrature-Phase signal

This works on the (simplified) mathematical principle:

Frequency(A) * Frequency(B) = Frequency(A-B) + Frequency(A+B)[4].

But aliases obtain at the mixer stage due to the difference frequencies which are removed in further stages using filtering techniques.

IV. FILTERING TECHNIQUES

A. CIC Filter

The cascaded integrator-comb (CIC) filter is a class of hardware-efficient linear phase finite impulse response (FIR) digital filters [6]. The CIC filter is suitable for this high-speed application because of its ability to achieve high decimation factors and other reason is it is implemented using additions and subtractions rather than using multipliers. It decimates by R which is programmable.

The two basic building blocks of a CIC filter are

1) An integrator (decimator): An integrator is simply a single-pole IIR filter with a unity feedback coefficient [7],[8]:

Y [n] = y [n-1] + x[n]

This system is also known as an accumulator [7],[8]. The transfer function for an integrator on the z-plane is

$$H_I(Z) = 1/(1 - Z^{-1})$$

2) Comb Filter (Interpolator): A comb filter running at the slow sampling rate fs/R is described by

y[n] = x[n] - x[n -M].

A comb filter is a differentiator with a transfer function

$$H_C(z) = (1 - z^{-M})$$

In this equation, *M* is the differential delay, and is usually limited to 1 or 2. To summarize, a CIC filter would have N cascaded integrator stages clocked at fs, followed by a rate change by a factor R, followed by N cascaded comb stages running at fs/R [8].

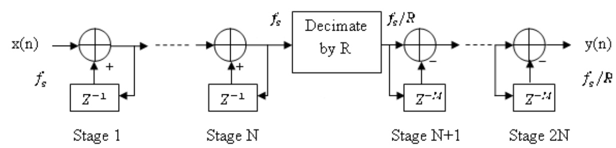

Fig. 4 CIC Filter

Frequency Characteristics:

The transfer function for a CIC filter at fs is

$$H_{cic}(z) = H_I^N(Z)H_C^N(Z) = \frac{(1 - Z^{-RM})^N}{(1 - Z^{-1})^N} = \left[\sum_{K=0}^{RM-1} Z^{-K}\right]^N$$

The magnitude response at the output of the filter is as shown below[3] .We can obtain an expression for the CIC filter's frequency response by evaluating $H_{cic}(z)$ transfer function on the *z*-plane's unit circle, by setting $z = e^j 2\pi f$, yielding a sinc like function.

$$|H(f)| = \left|\frac{\sin \pi RMf}{\sin(\pi f)}\right|^N$$

As already mentioned the frequency response of CIC filters is affected by the parameters N, M, R. Differential delay, M, affects the location of nulls at any given rate change value and increases attenuation levels generally at all lobes in the response. Varying the rate change value, R, adjusts the null positions up or down accordingly without having much affect on the attenuation of each lobe and increasing the number of stages increases attenuation of the lobes without shifting null positions.

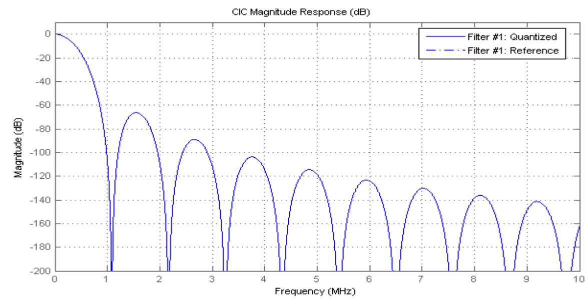

Fig. 5 Frequency response of CIC (N=5)

In the CIC Filter there is a disadvantage i.e.; it exhibits pass band droop. So we use CFIR to compensate this.

B. Compensation FIR filter:

The output of the CIC filter has a sinc shape, which is not suitable for most applications. A "clean-up" filter can be applied at the CIC output to correct for the pass band droop, as well as to achieve the desired cut-off frequency and filter shape. This filter typically decimates by a factor of 2 or 4 to minimize the output sample[1],[8].

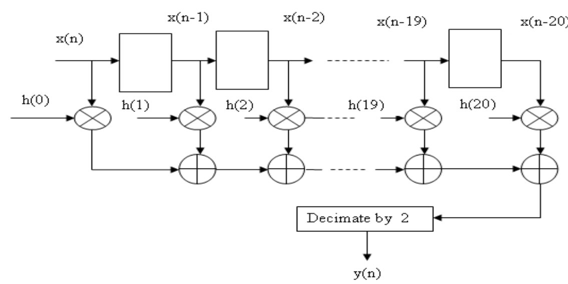

Fig. 6 Compensation Finite Impulse Response Filter

$$y(k) = \sum_{n=0}^{N-1} a(n)x(k-n) \quad k = 0,1,\ldots$$

Here a(n) represents coefficients. For this filter 21 coefficients are chosen with 18-bit precision. This filter will operate at low frequency (fs/*R)* to achieve a more efficient hardware solution. Its magnitude response is an inverse-sinc function.

$$H(f) = \left|MR\frac{\sin \pi f}{\sin(\pi RMf)}\right|^N \approx \left|\frac{\pi MRf}{\sin(\pi RMf)}\right|^N = |\mathrm{sinc}^{-1}(MRf)|^N$$

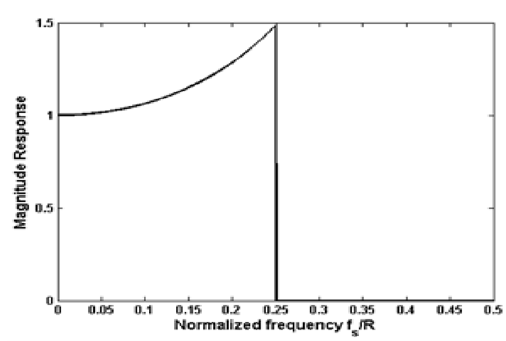

Fig. 7 Magnitude Response of CFIR Filter

C. *Programmable FIR filter:*

For the third and final stage a equiripple filter is chosen which provides an additional filtering, decimation by 2. The output from the PFIR is the output of DDC which is of 20 bits. All other characteristics are same as CFIR[1].

V. IMPLEMENTATION ON FPGA

An advantage of using an FPGA for the DDC is that we can customize the filter chain to exactly meet our requirements. ASSPs don't offer the design flexibility or integration attainable in an FPGA.

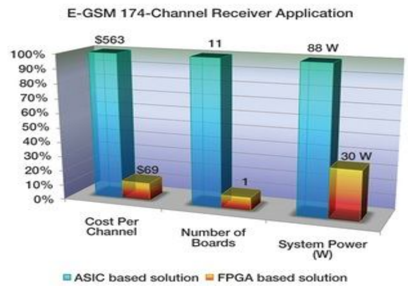

Fig. 8 Comparison of ASIC and FPGA

During the design, a behavioral model of the complete DDC is developed using Xilinx ISE software by writing VHDL code for each individual block and their operation is tested by simulating the design using Modelsim Simulator. Later the design is synthesized and implemented on an FPGA by generating a .bit file of the design and programming, configuring the FPGA with the .bit file [13]. The Xilinx Design flow is shown below

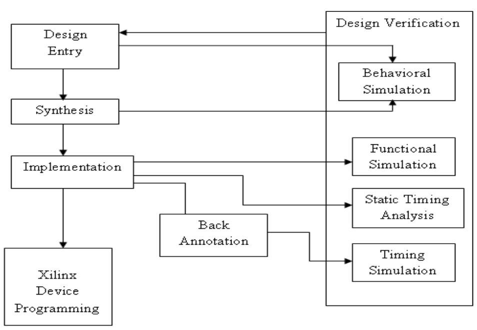

Fig. 9 Xilinx Design Flow

The correct operation of the design in the FPGA is tested using Chip Scope Pro Analyzer tool which uses three main blocks to analyze any part of DDC. These blocks are generated through the IP Core Generator tool in Xilinx ISE. The blocks are:

1) *ICON:* Integrated controller is use as an interface between the other two blocks and PC, JTAG which is connected to FPGA on which the design is programmed.

2) *ILA:* Integrated Logic Analyzer is used to control the inputs of any part of DDC thus achieving Controllability of inner circuits.

3) *VIO:* Virtual input output is used to observe the outputs of any part of DDC thus achieving observability.

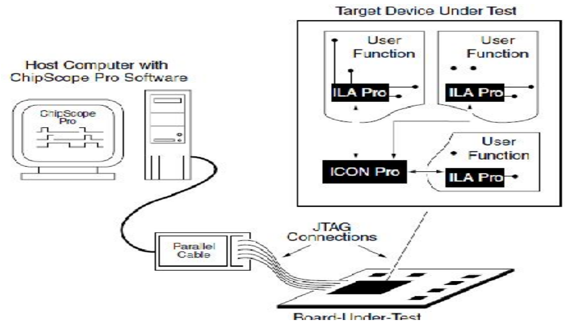

Fig. 10 Chip Scope pro Block Diagram

Thus Board level testing has also been performed.

VI. SIMULATION RESULTS

The behavior of the design is described in Very High Speed Integrated Circuit Hardware Description Language (VHDL). The VHDL code is simulated using Modelsim Simulation Tool. Xilinx Synthesis Technology (XST) tool is selected for synthesis. Maximum clock rate of 120.697MHz is achieved for the Digital Down Converter design in the XC5VSX95T device.

A.Device Specifications

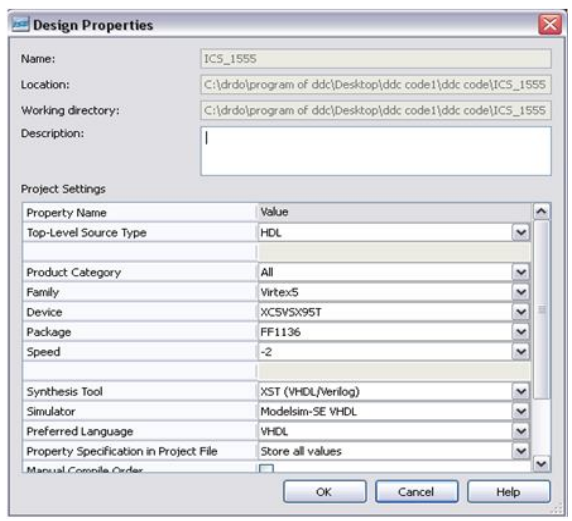

Fig. Device Specifications in Xilinx 10.1 for DDC

B. System level Testing

In the system level testing the functioning of the design is tested using Modelsim. In this design the first block is the Numerically Controlled Oscillator(NCO). Here the NCO is tuned to 0.78 MHz carrier where its clock frequency is

100MHz. Thus the Frequency Control Word (tuning frequency) is calculated from the formula $\Delta F = \frac{f_{out}}{f_{clk}} \times 2^{28}$ $= \frac{0.78}{100} \times 2^{28} =$ 2093798.5568. In binary representation the tuning frequency is 0000001000000000000000000000 which is added to the previous value of phase accumulator. For each value of phase out the corresponding amplitude value of sine & cosine wave is generated from the look up table as shown below.

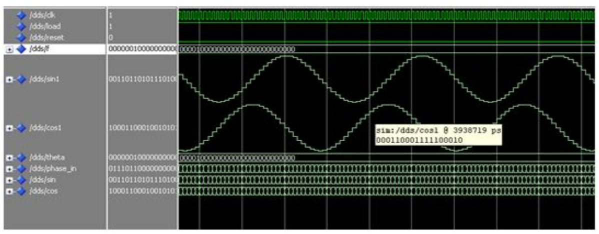

Fig.11 Sine and Cos carrier signals generated by NCO

The input from the ADC cannot be given to the system due to which mixer output cannot be taken in system level testing. So a manual signal is to be generated to test the functionality of the filters. The input to the CIC is taken as 2.5MHZ signal and the corresponding outputs of CIC, CFIR and PFIR for an overall decimation of 16 are shown below.

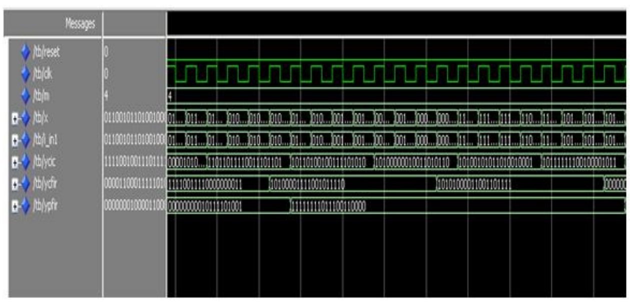

Fig. 12 CIC, CFIR, PFIR filters as literals for total decimation of 16

From the above figure it can be observed that as the decimation for CIC is 4 its output occurs for every four clock cycles and for CFIR the output changes for every eight clock cycles as it performs decimation by 2 to the CIC output, and similarly for PFIR for every 16 clock cycles. The corresponding analog format output is shown below.

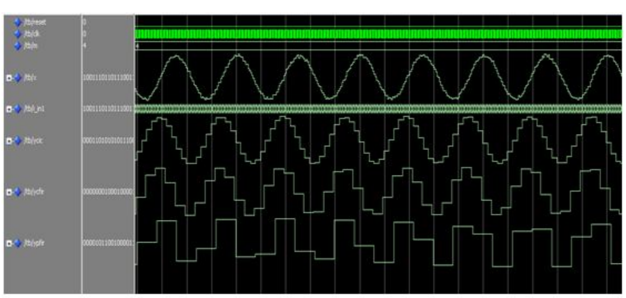

Fig. 13 Analog format of CIC CFIR and PFIR for overall decimation of 16

C. Timing Summary

Speed Grade: -2

Minimum period: 8.285ns (Max Frequency: 120.697MHz)

Minimum input arrival time before clock: 1.856ns

Maximum output required time after clock: 3.838ns

Maximum combinational path delay: No path found

D. *Device utilization summary*

TABLE I

DEVICE UTILIZATION SUMMARY

Device Utilization Summary			
Slice Logic Utilization	Used	Available	Utilization
Number of Slice Registers	68	58,880	1%
Number used as Flip Flops	68		
Number of Slice LUTs	135	58,880	1%
Number used as logic	135	58,880	1%
Number using O6 output only	135		
Number of occupied Slices	55	14,720	1%
Number of LUT Flip Flop pairs used	150		
Number with an unused Flip Flop	82	150	54%
Number with an unused LUT	15	150	10%
Number of fully used LUT-FF pairs	53	150	35%
Number of unique control sets	3		
Number of slice register sites lost to control set restrictions	4	58,880	1%
Number of bonded IOBs	319	640	49%
IOB Flip Flops	124		
Number of BUFG/BUFGCTRLs	2	32	6%
Number used as BUFGs	2		
Average Fanout of Non-Clock Nets	1.62		

E. ChipScope Pro Results

After porting the .bit file on the FPGA the results obtained on the FPGA are observed using ChipScope Pro software. Here two cases are taken in first case a single tone signal is taken as input and in second case a two tone signal is taken as input to the DDC.

Case 1: Single Tone signal

A single tone signal of frequency 30MHz is given as input to Digital Down Converter.

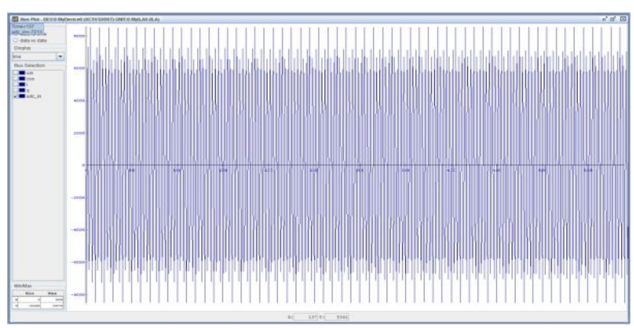

Fig. 14 Input signal of 30MHZ from ADC

First the 30MHz IF signal is to be shifted to baseband frequency. This is done by multiplying the input signal with 30MHz carrier generated by NCO.

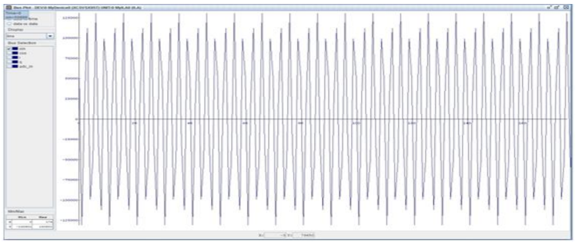

Fig. 15 Sine carrier of frequency 30MHz generated by NCO

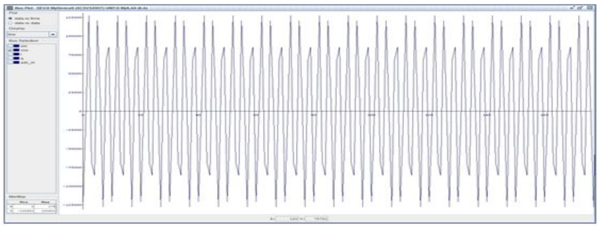

Fig. 16 Cos carrier of frequency 30MHz generated by NCO

The input signal is multiplied with the sin and cos carriers separately by two different mixers generating In phase (I) and Quadrature phase (Q) components at base band.

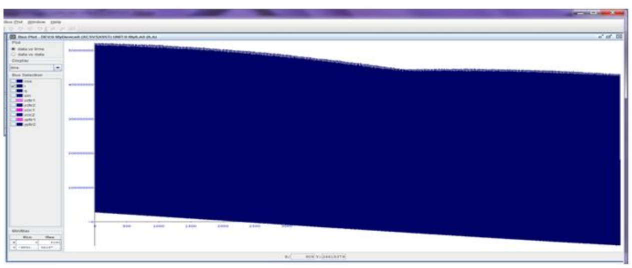

Fig. 17 Mixer1(In phase)output

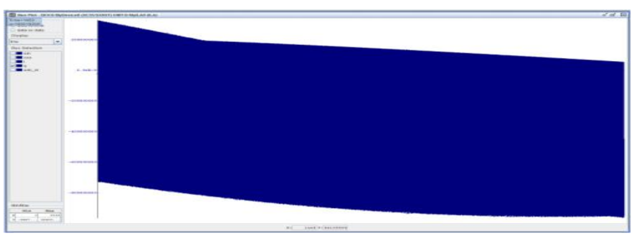

Fig. 18 Mixer2 (Quadrature phase) output.

The mixer output is further filtered and decimated by CIC, CFIR and PFIR filters.

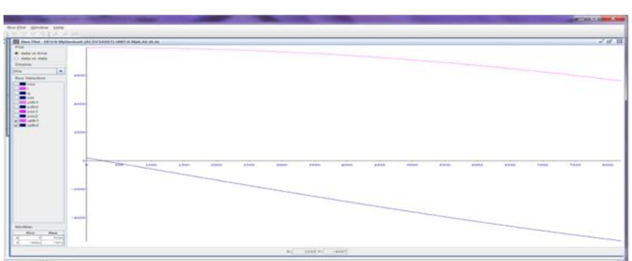

Fig. 19 Output of DDC for decimation of 16

Case 2 Two tone signal

Two signals one at frequency 30 MHz and other at frequency 27MHz are given to ADC these signals are sampled with a sample rate 100MSPS by ADC. The sampled two tone output from the ADC is given as input to DDC which is shown in the below figure.

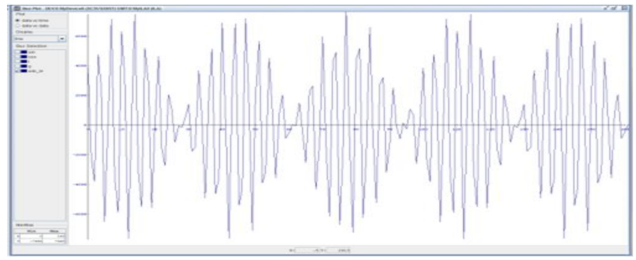

Fig. 20 Two tone input signal to DDC

On mixing the ADC signal with the sin and cos waves the resultant I and Q signals where I signal is shown and Q is same as I with just 90 degrees phase difference.

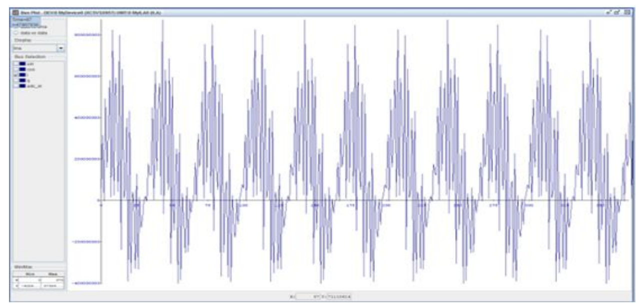

Fig. 21 Mixer(I) output for two tone

The I and Q signals are decimated by 4 in the CIC filter and futher by 4 in CFIR, PFIR filters. The output of DDC is

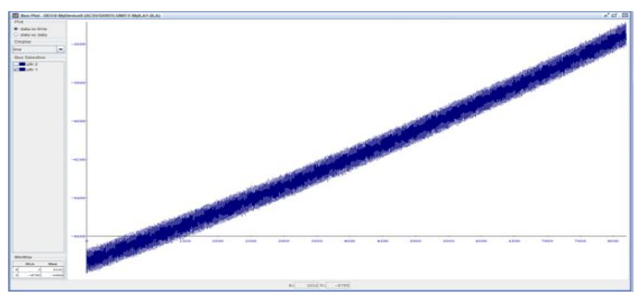

Fig. 22 Output of DDC(PFIR I path) for two tone

The output of the filters for decimation 13 at CIC stage are givan below. Here it can be seen that the 27MHz sinal is filtered at the CIC stage itself. Later decimation by 2 is done at each low pass FIR fiter that follows. Thus the overall decimation is 52.

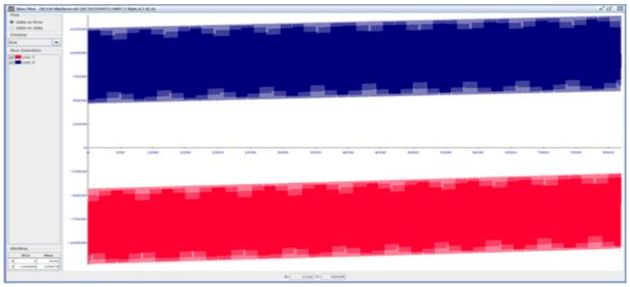

Fig. 23 CIC(I & Q) for total decimation 52

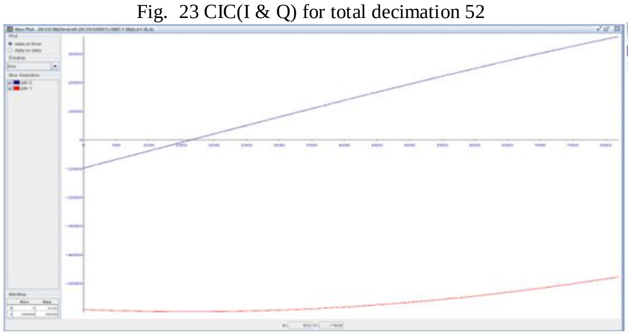

Fig.24 PFIR(I & Q) output for total decimation of 52

The output of all filters for decimation of 4095 at CIC is shown below

Fig. 25 Comparision of three filter outputs for overall decimation of 16384

Thus the DDC is tested for different decimations to obtain the signal of interest as output.

VII. CONCLUSION

Thus a configurable Digital Down Converter for Wideband signals has been developed All the blocks in the DDC are efficiently designed using Xilinx and implemented on FPGA. This project can also be applicable for Narrowband of signals. The implementation of variable decimation to extract the actual signal from the band of signals received makes the design more important. The fulfillment of the speed requirements stated has been shown through the timing summary. The components are been designed such that the end users can customize the design according to their requirements by simply modifying certain parameters in each block. Also as FPGA is chosen as the target technology, it results in a design with low power consumption, accurate performance, high integration and customizability.

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