SOPC Based Convolutional Encoding and Viterbi Decoding

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Abstract:-Viterbi decoder is a basic and important block in any Code Division Multiple Access (CDMA) and CDMA uses Convolutional encoder to prevent Interference. Convolutional encoding and Viterbi decoding are widely used in various communication systems because of their excellent error control performance. This paper deals with the implementation of Convolutional encoding and Viterbi decoding using SOPC. By analyzing the Viterbi decoder algorithm, the paper explores method to design Convolutional encoder and Viterbi decoder. The design has been implemented on SOPC using XILINX 12.2 software with supporting simulation tool ISim.

Keywords: - SOPC, Convolutional encoder, Viterbi decoder, Trellis diagram

I. INTRODUCTION

The Viterbi algorithm, proposed in 1967[1] is the most extensively employed decoding algorithm for convolutions codes. Convolutional coding is a popular error-correcting coding method used in digital communication [2]. A message is convoluted, and then transmitted into a noisy channel .This convolution operation encodes some redundant information into the transmitted signal, thereby improving the data capacity of the channel.

FPGA Implementation of modified Architecture For Adaptive Viterbi Decoder is presented in [3].It is found that the survivor path decoder is capable of supporting frequency up to 790 MHz for constraint lengths 7 and 9 ,rate 1/3 and long survivor path is 4. The synthesis results show that different constraint length didn't affect of the complexity of the decoder and the processing time of the computing the correct path.

Design and Implementation of a Parallel Processing Viterbi Decoder Using FPGA is presented in [4].It means trace back and decoder can simultaneously work in order to improve the processing speed.

Design and FPGA implementation of a high-speed hard decision Viterbi decoder with a constraint length of 7 and a code rate of ½ is presented in [5]. The design was functionally verified in two different self-checking simulation environments. The synthesis results show that the FPGA implementation can run as high as & also increased throughput.

In proposed work for a Viterbi decoder based on the strongly connected trellis decoding of binary Convolutional codes has been presented. The use of error-correcting codes has proven to be an effective way to overcome data corruption in digital communication channels. Paper deals with the implementation of Convolutional encoding and Viterbi decoding using SOPC .

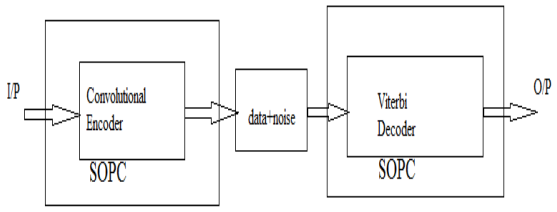

Fig.1 Typical FEC Scheme

II. CONVOLUTIONAL ENCODER

A Convolutional code is a type of error-correcting code which differs a lot from block codes. First the former does not have code words made up of distinct data sections and block sections. Instead, redundant bits are distributed throughout the coded data. Second, the encoder of the former contains memory and the n encoder outputs at any given time unit depend not only on the k inputs at that time unit but also on m previous input blocks. Convolutional codes are sometimes referred as trellis codes.

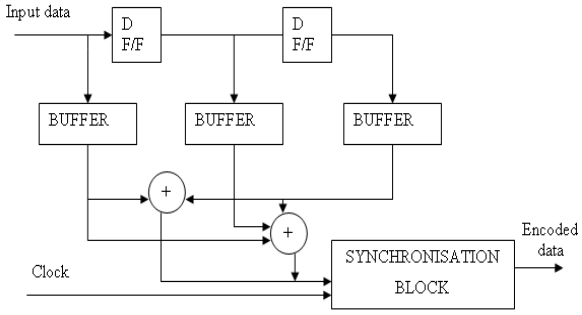

Fig.2 Convolutional Encoder

A Convolutional encoder can be viewed as a finite state machine . It can be implemented with registers ,XOR gates and a multiplexer .A Convolutional coding is done by combining the fixed number of input bits .The Input bits are stored in the fixed length shift register and they are combined with the help of mod-2 adders. This operation is equivalent to binary convolution and hence it is called Convolutional coding.

III. VITERBI DECODER

A Viterbi decoder uses the Viterbi Algorithm for a decoding a bit stream that has been encoded using FEC based on a Convolutional code. The Viterbi Algorithm belongs to the maximum likelihood decoding category. A Viterbi Decoder drops the least likely Trellis path at each transmission stage. In this way it decreases decoding complexity with early rejection of unlike paths and gets its efficiency via concentrating on survival paths of the Trellis. The receiver receives the serial encoded data and converts it into 2-bit parallel data. This parallel data is now feed to the subsequent blocks. Trellis Generator generates the predefined sequence which is used to calculate the branch metric unit. Fig shows Viterbi decoder

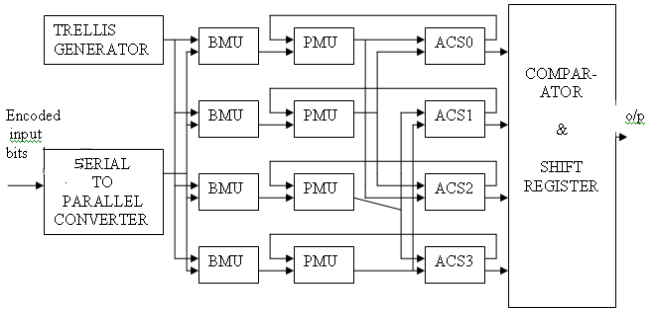

Fig.3 Viterbi Decoder

III. SOPC

SOPC is nothing but system on programming chip. It is semiconductor device containing programmable logic components and interconnects. The programmable logic components can be programmed to implement the function of basic logic gates such as AND, OR, NOT, XOR or more complex combinational functions such as encoder and decoder

or simple math functions. These programmable logic devices also include memory elements, which may be simple flip-flops or more complex blocks of memories [5] . In order to design the behavior of the SOPC, users must provide a Hardware Description Language [HDL].Such as Verilog Hardware Description Language or VHDL i.e. Very High Speed Integrated Circuit Hardware Description Language. Then, using an electronic design automation tool generates the netlist into actual devices.

IV. RESULTS

The Convolutional encoder and Viterbi decoder was implemented using Xilinx.

The experimental results are shown in Fig.

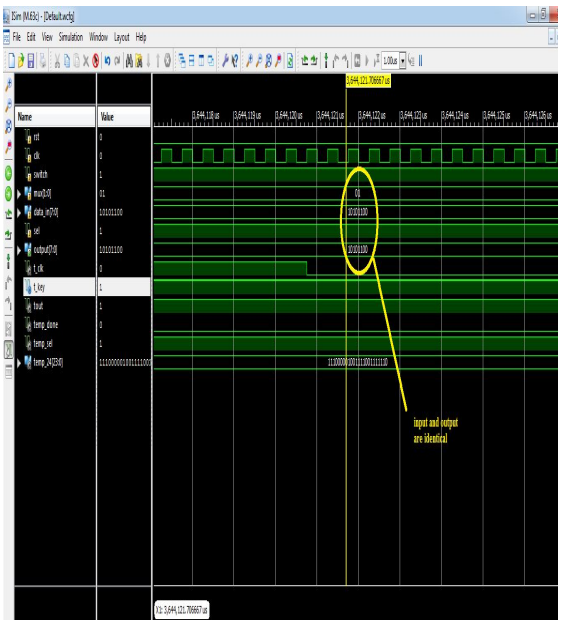

Fig.4 Experimental Results of Convolutional encoder & Viterbi decoder

The clk is the clock signal of whole system, and the rst is the reset signal of whole system. When the reset is set low and Switch is high then the Convolutional encoder and Viterbi decoder begin to work. The data_in and output respectively stand for input signals to Convolutional encoder and output signals from Viterbi decode. The mux (multiplexer) and sel (selection of code rate) is used to select noise and code rate respectively

From the experimental results, it is clear that the input signal given to the Convolutional encoder is identical to the output signal from the Viterbi decoder.

V. CONCLUSION

Viterbi decoder is one of the most important blocks in CDMA modem. This paper has implemented the Convolutional encoder and Viterbi decoder targeting a SOPC. Viterbi algorithm allows safe data transmission via error correction and original message can be recovered accurately without any noise.

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