Performance and Evaluation of Three Phase Bridge Module Type Diode Clamped Multilevel Inverter

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Abstract— This work proposes three phase five level Bridge module type Diode Clamped Multilevel Inverter (DCMLI) using various modulating techniques for induction motor load. These Pulse Width Modulating (PWM) techniques include Carrier Overlapping (CO) strategy, Variable Frequency (VF) strategy, Phase Shift (PS) strategy and Sub-Harmonic Pulse Width Modulation (SHPWM) i.e. Phase Disposition (PD) strategy, Phase Opposition Disposition (POD) strategy and Alternate Phase Opposition Disposition (APOD) strategy. The Total Harmonic Distortion (THD), V_{RMS} (fundamental), crest factor, form factor and distortion factor are evaluated for various modulation indices. Simulation is performed using MATLAB-SIMULINK. It is observed that PODPWM/PSPWM methods provide output with relatively low distortion for R Load. It is also observed that PSPWM method provides output with relatively low distortion for IM load. COPWM is also found to perform better since it provides relatively higher fundamental RMS output voltage for Induction Motor (IM) load and R load.

***Keywords*— DCMLI, PWM, THD, V_{rms}, CF**

I. INTRODUCTION

Multilevel inverters are finding increased attention in industries as a choice of electronic power conversion for medium voltage and high power applications. Multilevel inverters have lower harmonic spectra and lower device voltage stresses; so they are particularly suitable for high voltage and high power applications. With more voltage levels the staircase waveform is much closer to the sinusoidal waveform. Zhang et al [1] proposed a study on modified cascaded inverter with hybrid modulation. Corzine et al [2] described various control strategies for cascaded multilevel inverter. Haiwen et al [3] introduced hybrid cascaded multilevel inverter with PWM control method. Jing Zhao et al [4] developed a novel PWM control method for hybrid clamped multilevel inverters. Jinghua and Zhengxi [5] carried out research on hybrid modulation strategies based on general hybrid topology of multilevel inverter. Govindaraju and Baskaran [6] proposed optimized hybrid phase disposition PWM control method for multilevel inverters. Zhong et al [7] also developed fundamental frequency switching strategies of a seven level hybrid cascaded H-bridge multilevel inverter. Konstantinou et al [8] presented harmonic elimination control of a five level DC-AC cascaded H-bridge hybrid inverter. Khoucha et al [9] introduced hybrid cascaded H-bridge multilevel inverter for induction motor drive applications. Sepahvand et al [10] presented a hybrid multilevel inverter with both staircase and PWM switching schemes. Satyanarayanan et al [11] developed hybrid algorithm based vector controlled induction motor drive to achieve superior waveform quality. This literature survey reveals few papers only on various hybrid PWM techniques and hence this work presents a novel approach for controlling the harmonics of output voltage of chosen three phase cascaded MLI employing sinusoidal switching PWM strategies. Simulations are performed using MATLAB-SIMULINK. Harmonic analysis and evaluation of performance measures for various modulation indices have been carried out and presented.

II. MULTILEVEL INVERTER

The general structure of the multilevel converter is to synthesize a near sinusoidal voltage form several levels of DC voltage, typically obtained from capacitor voltage sources. As the number of levels increases the synthesized output waveforms have more steps, which produce a staircase wave that approaches a desired sine waveform. Also as more steps are added to the waveform, the harmonic distortion of the output wave decreases approaching zero as the number of levels increases infinitely. As the number of levels increases the voltage that can be spanned by summing multiple voltage levels also increases. MLI consists of a number of semiconductors connected in series and another identical number of voltage sources also connected in series. These two chains are connected with diodes at the upper and lower semiconductor. The results of the simulation study are presented in this work in the form of the PWM outputs of the chosen multilevel inverter.

TABLE I
SWITCHING SCHEME FOR SINGLE LEG 5 LEVEL CONVENTIONAL TYPE DCMLI

Sa_1	Sa_2	Sa_3	Sa_4	Sa_1'	Sa_2'	Sa_3'	Sa_4'	V_{AN}
1	1	1	1	0	0	0	0	$V_{dc}/2$
0	1	1	1	1	0	0	0	$V_{dc}/4$
0	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	$-V_{dc}/4$
0	0	0	0	1	1	1	1	$-V_{dc}/2$

TABLE II
SWITCHING SCHEME FOR SINGLE LEG 5 LEVEL BRIDGE MODULE TYPE DCMLI

S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{b1}	S_{b2}	S_{b3}	S_{b4}	V_{AN}
1	0	1	0	0	1	0	1	$V_{dc}/2$
1	0	0	1	0	1	0	1	$V_{dc}/4$
0	1	1	0	0	1	1	0	0
0	1	1	0	1	0	1	0	$-V_{dc}/4$
0	1	0	1	1	0	1	0	$-V_{dc}/2$

TABLE III
COMPARISON OF CONVENTIONAL DCMLI AND CASCADED TYPE DCMLI FOR FIVE LEVEL OUTPUT

Inverter Type	Conventional DCMLI	Cascaded Type DCMLI
Main switching devices	8	8
Main diodes	8	8
Clamping diodes	12	4
DC bus capacitors	4	2
Balancing capacitors	0	0

III. BRIDGE MODULE TYPE DCMLI

This paper presents a general multilevel hybrid topology through research on several basic multilevel topologies and introduces a few controllable degrees of freedom in the general hybrid topology. No matter what changes occur in the mentioned hybrid topologies, they can result in change and combination of the degrees of freedom, which expand the topology collection of multilevel inverter. All the cascaded topologies are unified through introduction of the degrees of freedom in the general multilevel hybrid topology. Based on research on hybrid topologies and multi-carrier SPWM applied to multilevel inverter, the paper makes a deep study on hybrid topology as in Fig.1 and Fig.2 with comparison of switching schemes and device count as in Tables I to III.

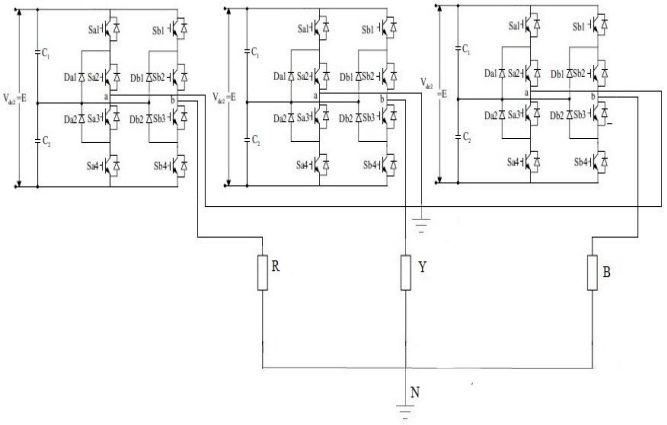

Fig.1 Three phase five level bridge module type DCMLI with R Load

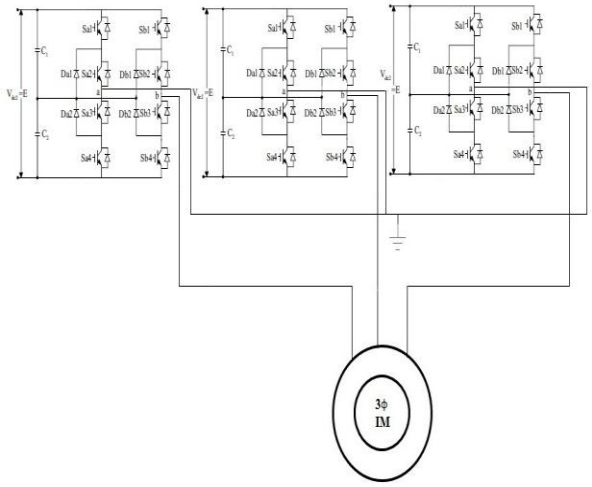

Fig.2 Three phase five level bridge module type DCMLI with Induction motor Load

IV. CARRIER BASED PWM METHODS

This paper uses the intersection of a sine wave with a triangular wave to generate firing pulses. There are many alternative strategies to implement this. They are as given below.

I. Phase Disposition PWM Strategy

The rules for phase disposition method Fig.3 for a five level inverter are :

1) 4 carrier waveforms in phase are arranged.
2) The converter is switched to + Vdc/2 when the sine wave is greater than both upper carriers.
3) The converter is switched to + Vdc/4 when the sine wave is greater than first upper carrier.
4) The converter is switched to zero when sine wave is lower than upper carrier but higher than the lower carrier.

5) The converter is switched to – Vdc/4 when the sine wave is less than first lower carrier.
6) The converter is switched to - Vdc/2 when the sine wave is less than both lower carriers.

The following formula is applicable to sub harmonic PWM strategy i.e. PD, POD and APOD

The frequency modulation index

$$m_f = f_c/f_m$$

The amplitude modulation index

$$m_a = 2A_m/ (m-1) A_c$$

where

f_c – Frequency of the carrier signal
f_m – Frequency of the reference signal
A_m –Amplitude of the reference signal
A_c – Amplitude of the carrier signal
m – number of levels.

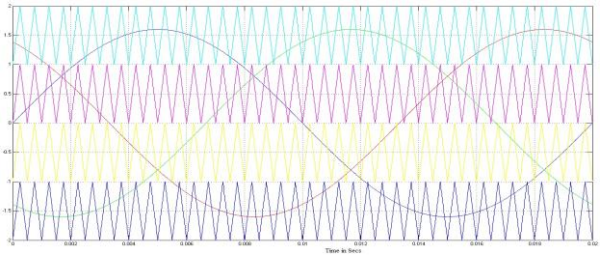

Fig.3 Carrier arrangement for PDPWM strategy
(m_a=0.8 and m_f=40)

II. Phase Opposition Disposition Strategy

Four carrier waveforms are arranged so that all carrier waveforms above zero are in phase and they are 180 degrees out of phase with those below zero (Fig.4).

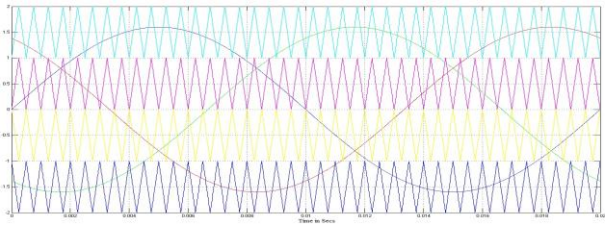

Fig. 4 Carrier arrangement for PODPWM strategy
(m_a=0.8 and m_f=40)

III. Alternative Phase Opposition and Disposition Strategy

Carriers are arranged in such a manner that each carrier is out of phase with its neighbor by 180 degrees (Fig.5).

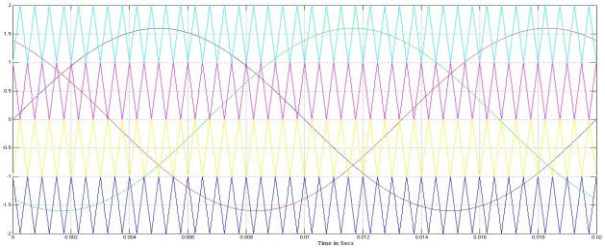

Fig. 5 Carrier arrangement for APODPWM strategy
(m_a=0.8 and m_f=40)

IV. Phase Shift PWM (PSPWM) Strategy

The phase shift multicarrier PWM technique (Fig.6) uses four carrier signals of the same amplitude and frequency which are shifted by 90 degrees to one another to generate the five level inverter output voltage. The gate signals for the chosen inverter can be derived directly from the PWM signals (comparison of the carrier with the sinusoidal reference).

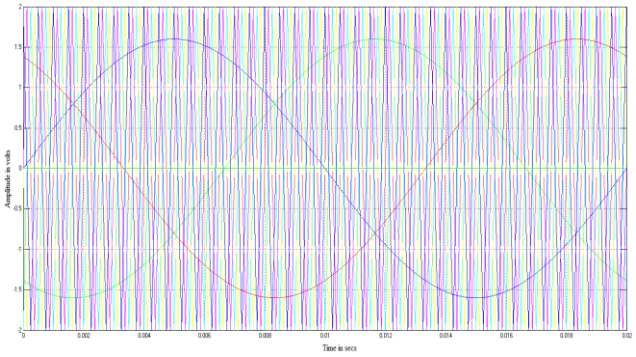

Fig. 6 Carrier arrangement for PSPWM strategy
(m_a=0.8 and m_f=40)

$$m_a = A_m/(A_c/2)$$

V. Carrier Overlapping PWM (COPWM) Strategy

For an m-level inverter using carrier overlapping technique, m-1 carriers with the same frequency f_c and same peak-to-peak amplitude A_c are disposed such that the bands they occupy overlap each other; the overlapping vertical distance between each carrier is $A_c/2$. The reference waveform has amplitude of A_m and frequency of f_m and it is centred in the middle of the carrier signals. The reference wave is continuously compared with each of the carrier signals. If the reference wave is more than a carrier signal, then the active devices corresponding to that carrier are switched on. Otherwise, the devices switch off. The amplitude modulation index m_a and the frequency ratio m_f are defined in the carrier overlapping method (Fig.7) as follows:

$$m_a = A_m / (m / 4)* A_c$$
$$m_f = f_c / f_m$$

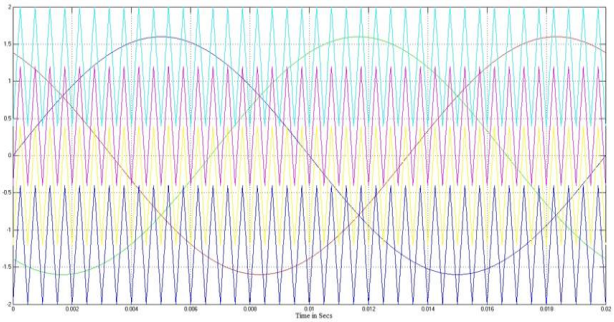

Fig. 7 Carrier arrangement for COPWM strategy
(m_a=0.8 and m_f=40)

VI. Variable Frequency PWM (VFPWM) Strategy

The number of switchings for upper and lower devices of chosen MLI is much more than that of intermediate switches in SHPWM using constant frequency carriers. In order to equalize the number of switchings for all the switches, variable frequency PWM strategy is used as illustrated in which the carrier frequency of the intermediate switches is properly increased to balance the numbers of switching for all the switches (Fig.8).

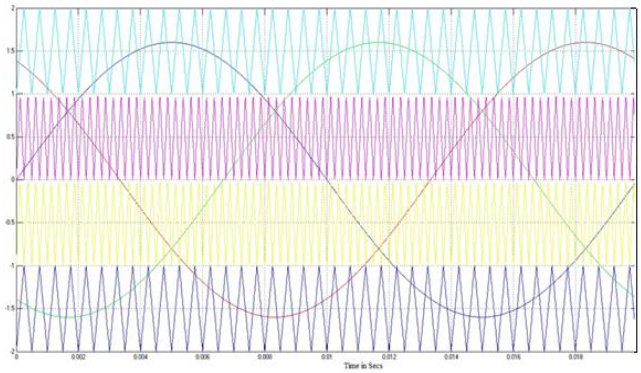

Fig.8 Carrier arrangement for VFPWM strategy (m_a=0.8 and m_f=40 (Upper and Lower Switches) and m_f=80 (Intermediate Switches))

In this paper, m_f = 40 and ma is varied from 0.6 to 1. m_f is chosen as 40 as a trade off in view of the following reasons:

1) to reduce switching losses (which may be high at large m_f)
2) to reduce the size of the filter needed for the closed loop control, the filter size being moderate at moderate frequencies
3) to effectively utilise the available dSPACE system for hardware implementation.

V. Simulation Results

The three phase bridge module type diode clamped five level inverter is modelled in SIMULINK using power system block set. Simulations are performed for different values of m_a ranging from 0.6 to 1 and the corresponding %THD are measured using the FFT block and their values are shown in Table IV and V. Figs. 9 – 26 show the simulated output voltages of bridge module type DCMLI fed IM and their harmonic spectrum, speed and torque characteristics of Induction Motor (IM) with above strategies but for only one sample value of m_a = 0.8. Fig. 10 shows the five level output voltage generated by PDPWM strategy and its FFT plot is shown in Fig. 11. From Fig. 11, it is observed that the PDPWM strategy produces significant 30th, 32nd, 36th and 38th harmonic energy. Fig 13 shows the five level output voltage generated by PODPWM strategy and its FFT plot is shown in Fig. 14. From Fig. 14, it is observed that the PODPWM strategy produces significant 33rd and 35th harmonic energy. Fig. 16 shows the five level output voltage generated by APODPWM strategy and its FFT plot is shown in Fig. 17. From Fig. 17, it is observed that the APODPWM strategy produces significant 35th and 37th harmonic energy. Fig 19 shows the five level output voltage generated by COPWM strategy and its FFT plot is shown in Fig. 20. From Fig. 20, it is observed that the COPWM strategy produces significant 35th and 37th harmonic energy. Fig 22 shows the five level output voltage generated by VFPWM strategy and its FFT plot is shown in Fig. 23. From Fig. 23, it is observed that the VFPWM strategy produces significant 34th and 38th harmonic energy. Fig. 25 shows the five level output voltage generated by PSPWM strategy and its FFT plot is shown in Fig. 26. From Fig. 26, it is observed that the PSPWM strategy produces no significant harmonic energy. The following parameter values are used for simulation : V_{dc} = 440V, induction motor load – 50HP(37 KW), 400V, 50Hz, 1480rpm, T_m = 4Nm, f_c = 2000Hz, f_m = 50Hz. Figs. 9, 12, 15, 18, 21 and 24 show speed torque characteristics of IM fed by chosen MLI for PD, POD, APOD, CO, VF PWM strategies.

Figs. 27 – 36 show the simulated output voltage of bridge module type DCMLI fed R Load. Fig. 27 shows the five level output voltage generated by APODPWM strategy and its FFT plot is shown in Fig. 28. From Fig. 28, it is observed that the APODPWM strategy produces significant 35th and 37th harmonic energy. Fig. 29 shows the five level output voltage generated by PODPWM strategy and its FFT plot is shown in Fig. 30. From Fig. 30, it is observed that the PODPWM strategy produces significant 33rd and 35th harmonic energy. Fig. 31 shows the five level output voltage generated by PDPWM strategy and its FFT plot is shown in Fig. 32. From Fig. 32, it is observed that the PDPWM strategy produces significant 30th, 32nd, 36th and 38th harmonic energy. Fig. 33 shows the five level output voltage generated by COPWM strategy and its FFT plot is shown in Fig. 34. From Fig. 34, it is observed that the COPWM strategy produces significant 3th and 37th harmonic energy. Fig. 35 shows the five level output voltage generated by VFPWM strategy and its FFT plot is shown in Fig. 36. From Fig. 36, it is observed that the VFPWM strategy produces significant 34th and 38th harmonic energy. Fig. 37 shows the five level output voltage generated by PSPWM strategy and its FFT plot is shown in Fig. 38. From Fig. 38, it is observed that the PSPWM strategy produces no significant harmonic energy. The following parameter values are used for simulation (R Load) : V_{dc} = 440V , R=100 ohms, f_c = 2000Hz and f_m = 50Hz.

A. Simulation Results for Induction Motor Load

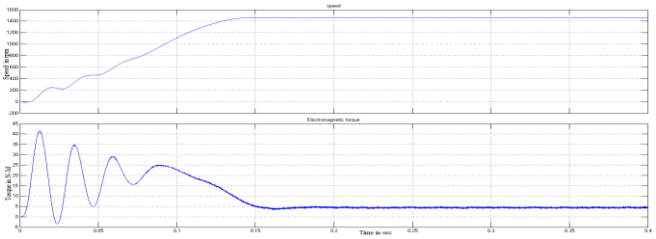

Fig.9 Speed and torque characteristics of IM load (PDPWM)

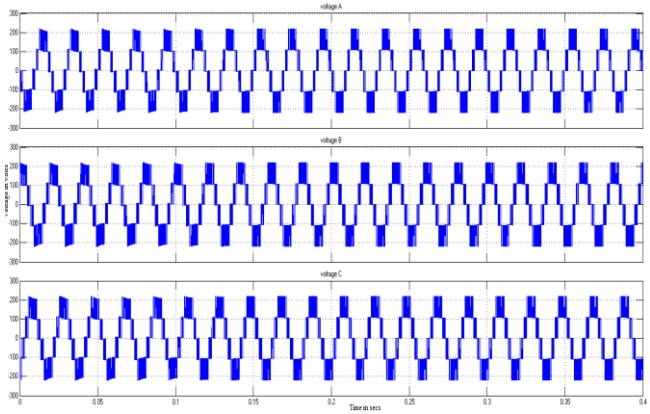

Fig. 10 Output voltage generated by PDPWM method for m_a=0.8 and m_f =40

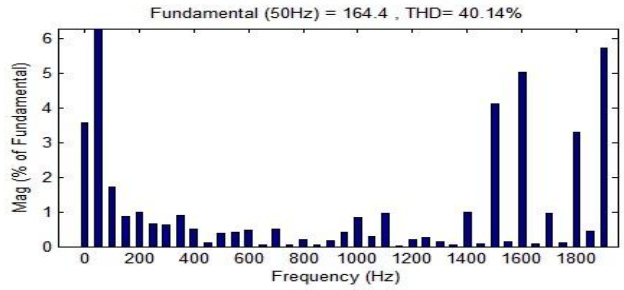

Fig. 11 FFT plot for output voltage of PDPWM method

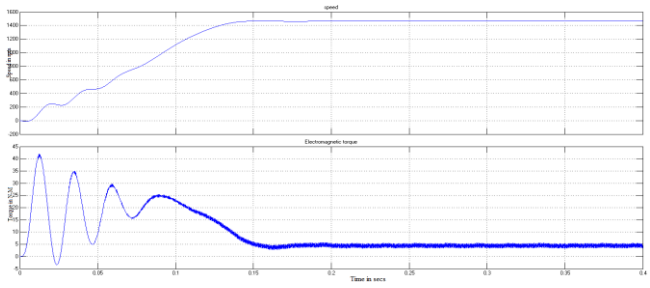

Fig.12 Speed and torque characteristics of IM load (PODPWM)

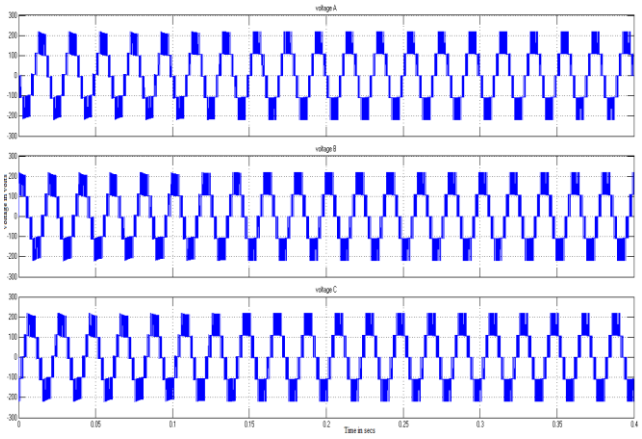

Fig. 13 Output voltage generated by PODPWM method for m_a=0.8 and m_f=40

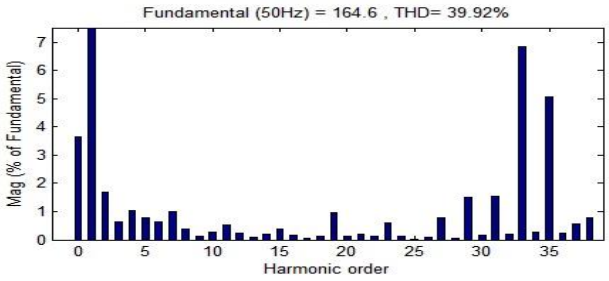

Fig. 14 FFT plot for output voltage of PODPWM method

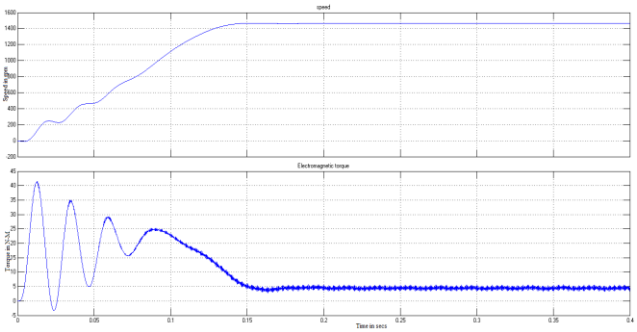

Fig. 15 Speed and torque characteristics of IM load (APODPWM)

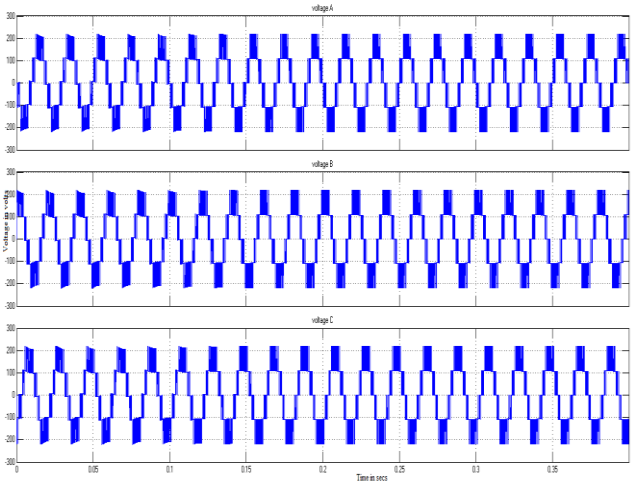

Fig.16 Output voltage generated by APODPWM method for m_a=0.8 and m_f=40

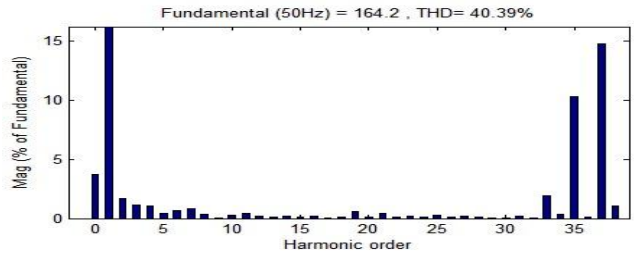

Fig. 17 FFT plot for output voltage of APODPWM method

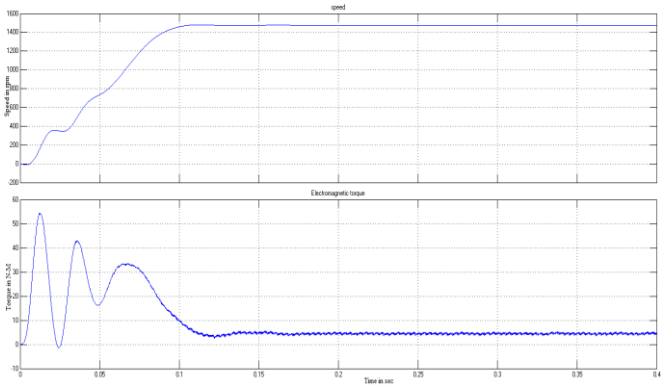

Fig. 18 Speed and torque characteristics of IM load (COPWM)

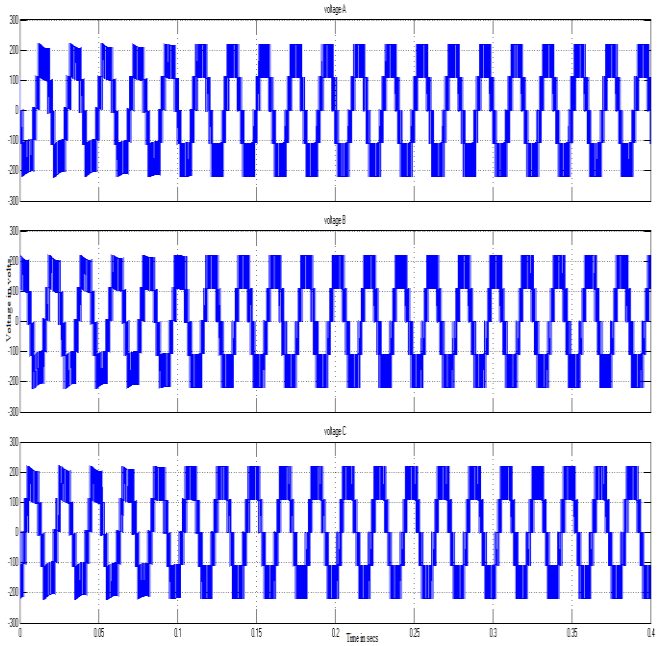

Fig. 19 Output voltage generated by COPWM method for m_a=0.8 and m_f=40

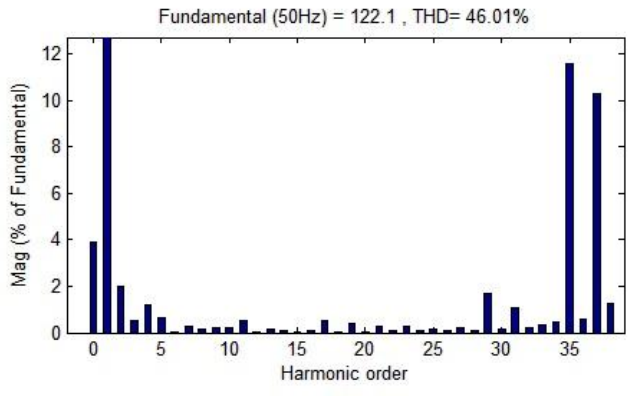

Fig. 20 FFT plot for output voltage of COPWM method

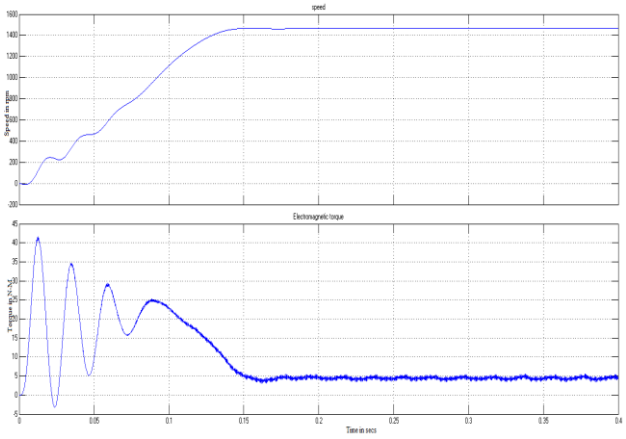

Fig. 21 Speed and torque characteristics of IM load (VFPWM)

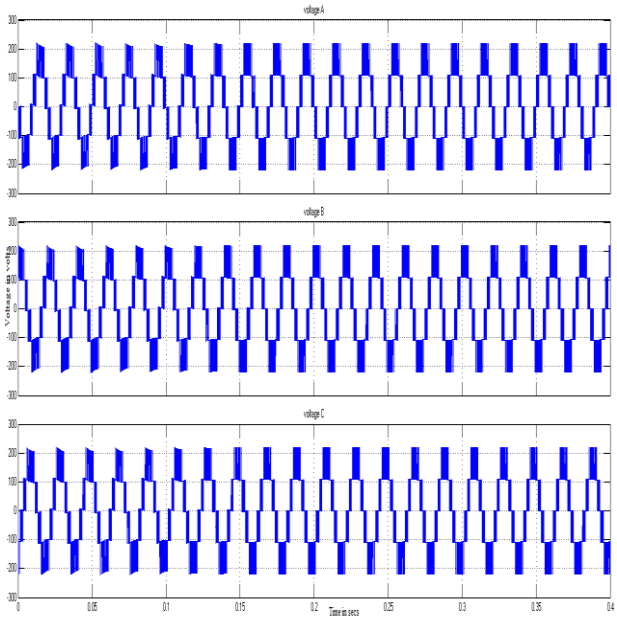

Fig. 22 Output voltage generated by VFPWM method for m_a = 0.8 and m_f=40

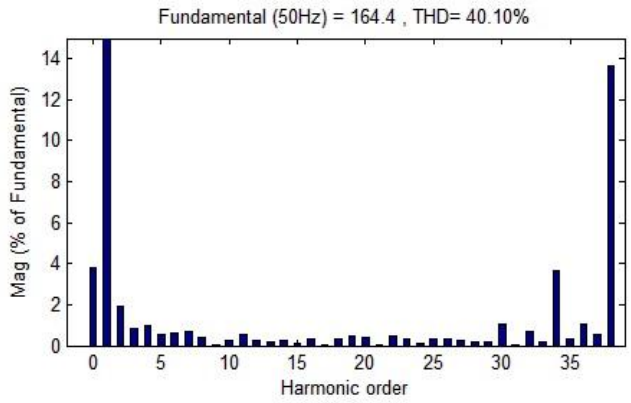

Fig. 23 FFT plot for output voltage of VFPWM method

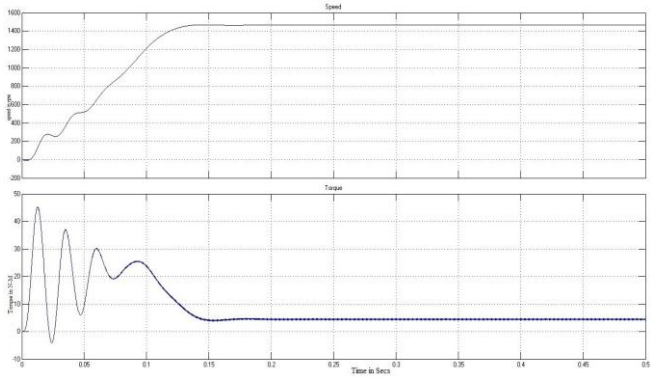

Fig. 24 Speed and torque characteristics of IM load (PSPWM)

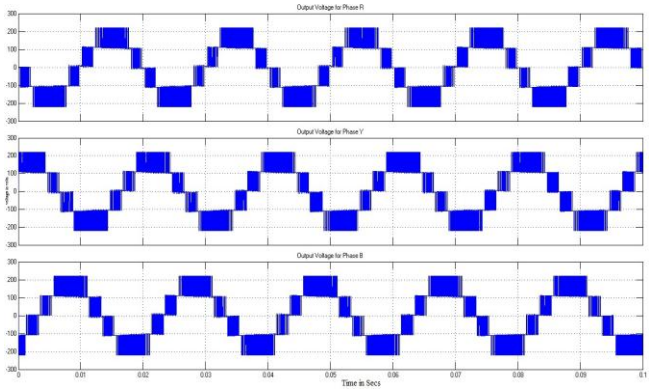

Fig. 25 Output voltage generated by PSPWM method for m_a=0.8 and m_f=40

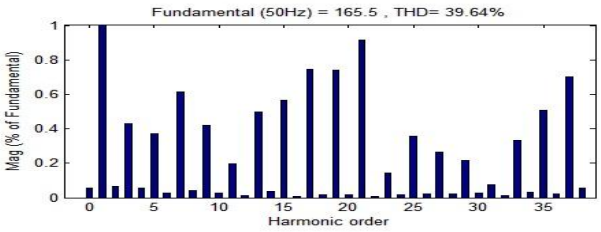

Fig. 26 FFT plot for output voltage of PSPWM method

B. Simulation Results for R Load

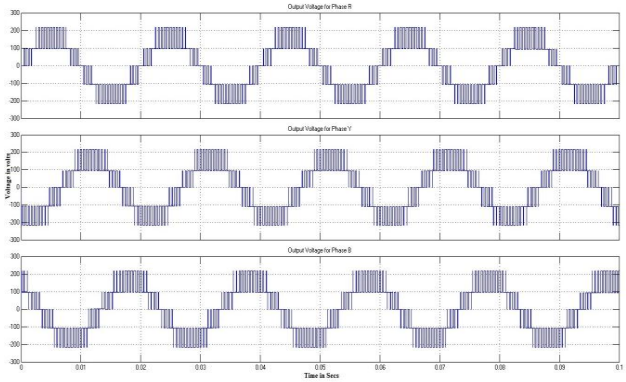

Fig.27 Output voltage generated by APODPWM strategy for R load

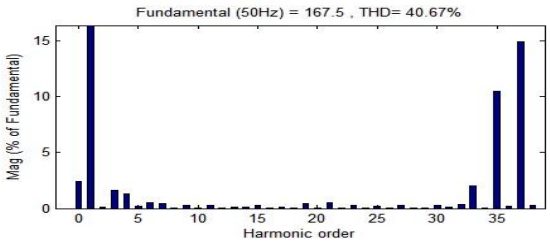

Fig.28 FFT plot for output voltage of APOD PWM strategy for R load

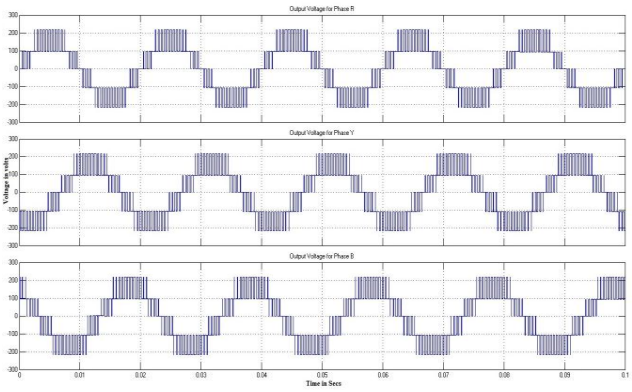

Fig.29 Output voltage generated by PODPWM strategy for R load

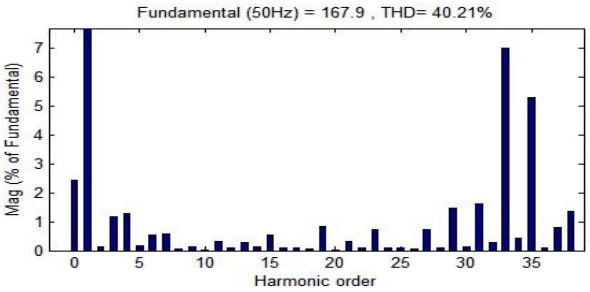

Fig.30 FFT plot for output voltage of PODPWM strategy for R load

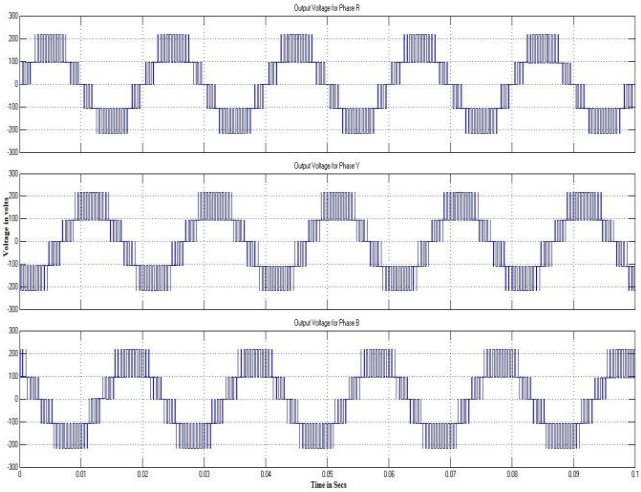

Fig. 31 Output voltage generated by PDPWM strategy for R load

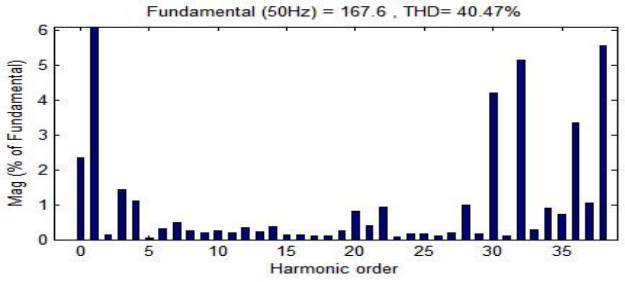

Fig.32 FFT plot for output voltage of PDPWM strategy for R load

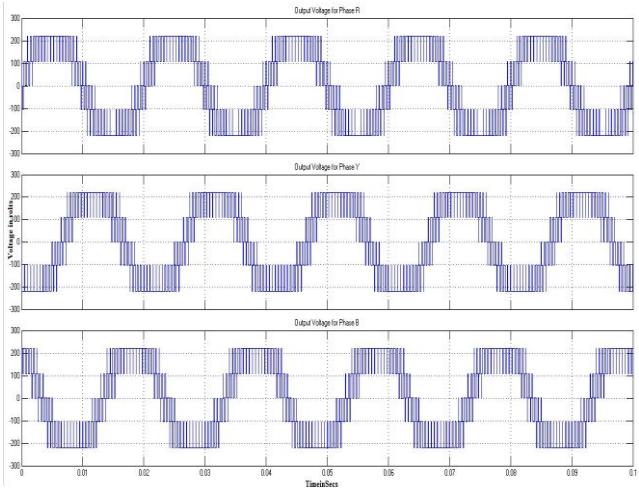

Fig.33 Output voltage generated by COPWM strategy for R load

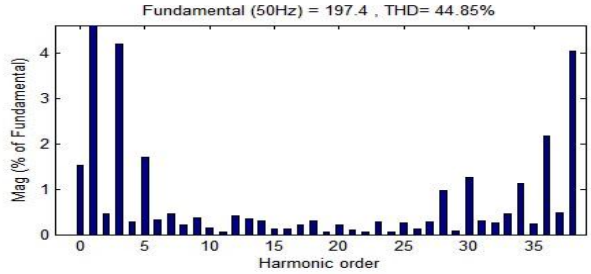

Fig.34 FFT plot for output voltage of COPWM strategy for R load

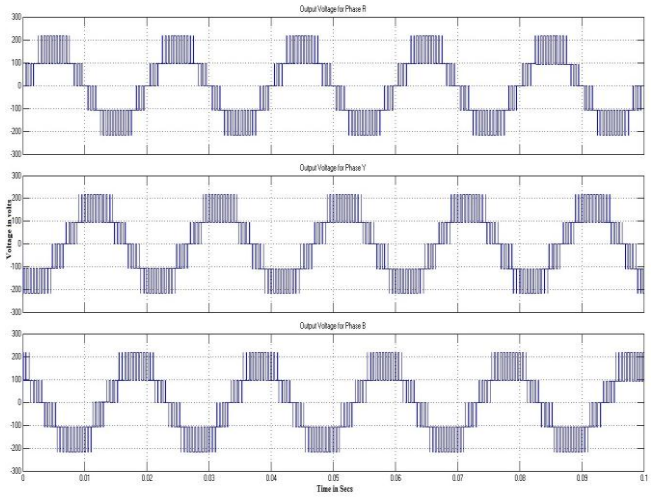

Fig.35 Output voltage generated by VFPWM strategy for R load

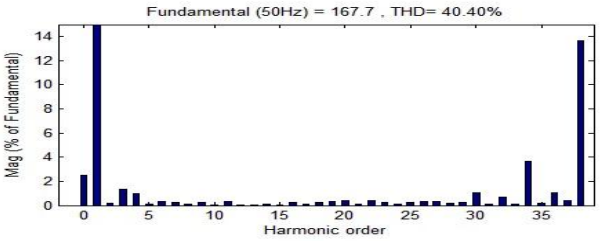

Fig.36 FFT plot for output voltage of VFPWM strategy for R load

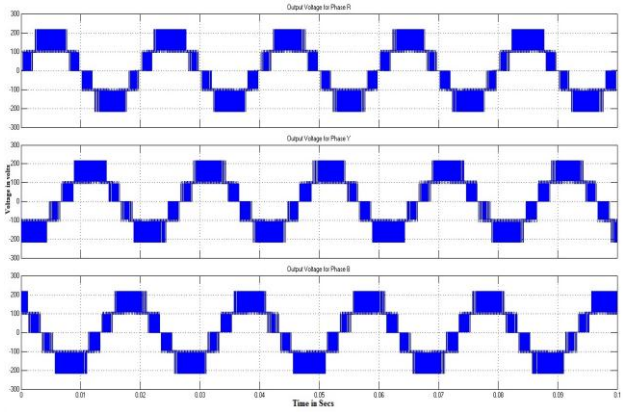

Fig.37 Output voltage generated by PSPWM strategy for R load

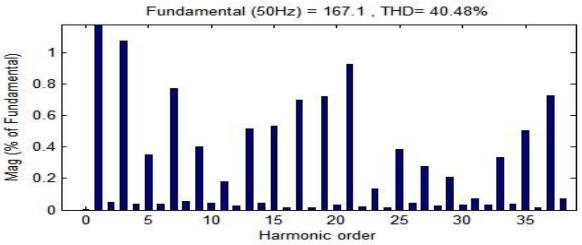

Fig.38 FFT plot for output voltage of PSPWM strategy for R load

TABLE IV
%THD FOR DIFFERENT MODULATION INDICES FOR IM LOAD

m_a	APOD	CO	PD	POD	VF	PS
1	28.33	32.75	27.83	27.75	27.85	27.86
0.9	35.4	39.51	34.98	34.89	34.85	33.89
0.8	40.39	46.01	40.14	39.92	40.1	39.64
0.7	43.89	55.76	43.78	43.6	44.16	42.85
0.6	45.09	66.1	45.11	45.14	45.16	45.48

TABLE V
%THD FOR DIFFERENT MODULATION INDICES FOR R LOAD

m_a	APOD	CO	PD	POD	VF	PS
1	28.56	32.73	28.1	28	28.12	28.24
0.9	35.65	39.46	35.28	35.16	35.14	34.55
0.8	40.67	44.85	40.47	40.21	40.4	40.48
0.7	44.27	55.49	44.21	44.04	44.62	43.76

0.6	45.88	65.88	45.94	46.01	46.01	46.13

0.6	10.4	2.45	10.17	10.45	9526.66	10.43

TABLE VI
VRMS FUNDAMENTAL FOR DIFFERENT MODULATION INDICES FOR IM LOAD

m_a	APOD	CO	PD	POD	PS	VF
1	147.5	151	147.7	147.7	148.3	147.7
0.9	131.8	137.2	132	132	132.9	132
0.8	116.1	122.2	116.2	116.4	117	116.3
0.7	100.3	104.3	100.3	100.2	102.1	100.1
0.6	84.81	85.75	84.82	84.64	85.74	85

TABLE VII
VRMS FUNDAMENTAL FOR DIFFERENT MODULATION INDICES FOR R LOAD

m_a	APOD	CO	PD	POD	PS	VF
1	150.4	154.2	150.6	150.6	150.7	150.6
0.9	134.4	140.1	134.6	134.6	134.8	134.6
0.8	118.5	124.9	118.5	118.7	118.2	118.6
0.7	102.4	106.9	102.4	102.2	102.7	102.1
0.6	86.56	87.98	86.53	86.33	85.4	86.7

TABLE VIII
CREST FACTOR FOR DIFFERENT MODULATION INDICES FOR IM LOAD

m_a	APOD	CO	PD	POD	PS	VF
1	1.414	1.414	1.413	1.415	1.414	1.413
0.9	1.414	1.414	1.414	1.414	1.414	1.414
0.8	1.413	1.413	1.414	1.414	1.413	1.414
0.7	1.414	1.414	1.413	1.412	1.415	1.414
0.6	1.414	1.414	1.414	1.414	1.415	1.414

TABLE IX
CREST FACTOR FOR DIFFERENT MODULATION INDICES FOR R LOAD

m_a	APOD	CO	PD	POD	PS	VF
1	1.414	1.413	1.414	1.414	1.414	1.414
0.9	1.414	1.413	1.414	1.414	1.414	1.414
0.8	1.414	1.414	1.414	1.414	1.414	1.413
0.7	1.414	1.414	1.414	1.414	1.414	1.414
0.6	1.413	1.414	1.414	1.414	1.413	1.414

TABLE X
FORM FACTOR FOR DIFFERENT MODULATION INDICES FOR IM LOAD

m_a	APOD	CO	PD	POD	PS	VF
1	37.27	8.2	36.75	37.73	708.89	39.58
0.9	26.35	6.03	25.85	26.67	731.82	25.8
0.8	19.05	4.63	19.71	19.29	1318.01	18.78
0.7	13.92	3.31	13.39	14.02	2919.64	13.7

TABLE XI
FORM FACTOR FOR DIFFERENT MODULATION INDICES FOR R LOAD

m_a	APOD	CO	PD	POD	PS	VF
1	52.02	8.75	50.45	52.34	2089.28	56
0.9	38	6.36	36.53	38.21	1581.78	36.67
0.8	29.21	4.59	30.32	29.16	14960.13	28.11
0.7	22.64	3.53	20.91	22.81	81443.29	22
0.6	20.73	2.64	17.24	18.18	1679.2	17.89

IV. CONCLUSION

In this work the simulation results of three phase five level bridge module type diode clamped multilevel inverter fed R Load and Induction Motor load with various modulating strategies are obtained through MATLAB/SIMULINK. The output quantities like phase voltage, THD spectrum for phase voltage, and torque-speed characteristics of induction motor are obtained. PSPWM produces less THD with IM load (Table IV). It is observed that PSPWM/PODPWM method provides output with relatively low distortion for R load (Table V). COPWM is also found to perform better since it provides relatively higher fundamental RMS output voltage for IM load and R load (Table VI and VII). Tables VIII to XI show the crest factor and form factor.

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