Clock Synchronization in Digital Circuits

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***Abstract*- There are different ways to operate digital circuits to achieve good propagation of data. In recent days most of the digital circuits are failing to synchronize the clock with data waves. The clock pulse must be given in proper time period, almost equal to the data propagation speed or arrival time of the data to the next stage. In the present paper a new method is proposed to synchronize the speed between data and clock pulses.**

Keywords: **Clock, Synchronization, Latches, Propagation delay.**

I. INTRODUCTION

In complex combinational circuits or sequential circuits the clock arrives at next stages before the data pulses arrives to the next stage. The clock pulse must be inserted to activate the digital circuits at any stage starting from first stage. But due to un-synchronization between clock pulse and data there is a chance of miss hitting in the next stages. This leads improper data transmissions in complex systems. It creates data losses in transmission.

In simple circuits contain fewer flip flops the problem may not arise. But the circuits with complex logic circuit between flip-flops may face these types of problems. Because the complex logic circuits cause some delay to propagate the data from one flip flop to other flip flop or from one stage to other stage. In the present paper flip flops and delay logics are considered to describe the problem.

Very first cotton described this problem as maximum rate propagation [1]. After that some solutions were derived to solve this problem by in traducing delay elements and splitting the stages into multiple stages [2][3]. Improper clock Synchronization leads to slow data propagation and loss of data [4][5]. The propagation delay must be less than the clock pulse applied to the circuit.

The clock signal is derived in the Me-synchronous pipelining [3] is

$$T_{clk.m} \geq (D_{\max}(f) - D_{\min}(f)) + T_h + T_s + 2\Delta_{clk}$$

The clock signal derived in the wave pipelining is [2]

$$T_{clk.w} \geq (D_{\max} - D_{\min}) + T_h + T_s + 2\Delta_{clk}$$

Where $T_{clk.m}$ = Mesycnronous clock pulse

D_{max} = maximum Propagation Delay

D_{min} = minimum Propagation Delay

T_h = Hold time

T_s = Setting Time

Δ_{clk} = Clock Skew

In the previous methods finding the exact delay values is difficult`. The delay values are different from one stage to other stage. So it increases the complexity in designing the circuit.

II. PROPOSED METHOD

In the proposed Method simple logic gates are taken to check the previous flip flop binary information. The logic gates create simple delay in producing the clock to the next stage. Until the logic gates identify the next binary bit from previous stage it will not allow the clock generator to pass the next clock pulse to the next stage of the circuit as shown in figure1.

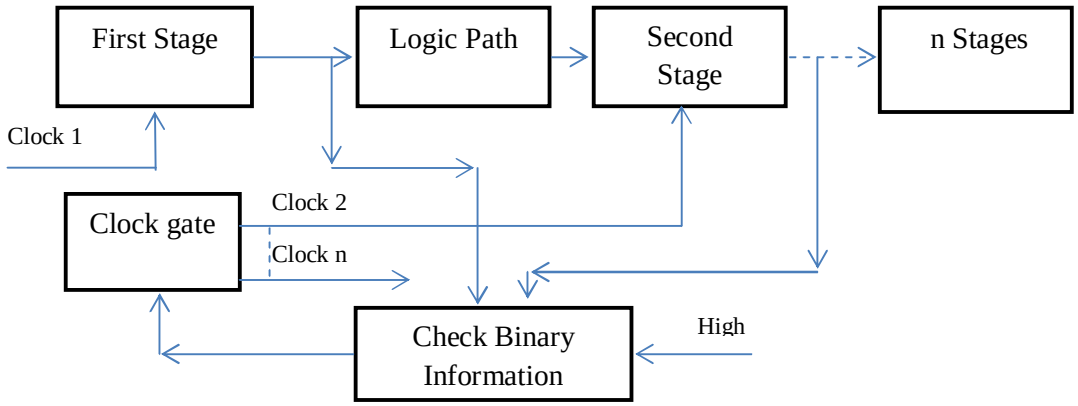
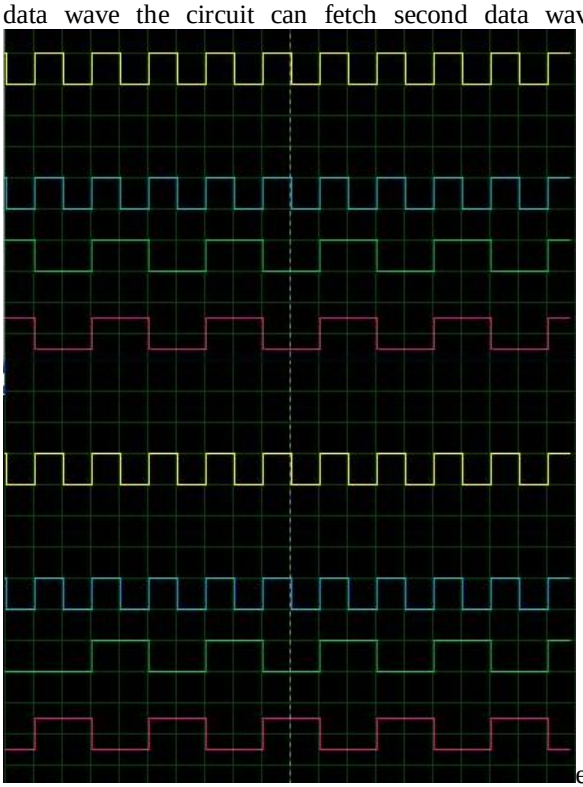


Figure 1 Block Diagram of Proposed Method

The first stage data will be verified through check binary information logic gates and the status will be forwarded to clock gate. Upon receiving the status the clock gate will be activated and then pass the clock pulses to the next stages, which will enable other stages and allows to receive the data from previous stages through logic circuit. Before receiving the clock pulses from the clock gate the next stages will be in high impedance state. The clock gate generates individual clock pulses on individual paths to next stages Such as clock 2 to second stage, clock 3 to third stage and so on up on receiving the status from Check binary information circuit block.

III. RESULTS

The circuit is implemented and tested in CAD tools. The results are analysed and compared with past methods. In the present method it is observed less delay time. Some results are shown in figure 2 . In the figure 2 the yellow colour pulse represents clock1 and blue colour represents clock 2. The input data is represented with green colour and output data is represented with pink colour. In this diagram the first green and pink colour waves represent the input and output of the first stage of the circuit. The second green and pink colour waves represent the input and output of second stage of the circuit. In the first stage the data input and output are in same phase. They appear at same clock pulse in the timing diagram. But in the second stage it is different. The second green and pink colours follow different clock phases unlike first green and pink colours. That means in the second phase the input and output appear in different phases of the clock. Because the data arrived at second stage input is after crossing logic circuit between two stages. So it took one clock pulse to come input pin of the second stage. And the clock pulse clock2 arrives after one clock pulse. So the output appears after one clock pulse after the input appears at second stage. That is the output will appear at second stage after two clock pulses after the first input appear at first stage. At the same time, while the second stage processing the first data wave the first stage receives the second data wave. That means while processing the one data wave the circuit can fetch second data wave.



etc

Fig 2: Some simulation results of data with 500Hz speed in two stage circuit

IV. CONCLUSION

In the present system data losses were minimized and achieved higher data rates. Clock synchronization is achieved with new logic circuit. When data arrives at output of the one stage, then only the clock pulse will be fed to the next stage of the circuit. That means the output will be passed from one stage to the next stage. In this context the clock width is reduced when compared to other methods. So the power consumption is also reduced in the proposed method.

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