

# Design of Logic Circuits Using Reversible Gates

K.V Manoj<sup>1</sup>, M.Amarnath Reddy<sup>2</sup>,

<sup>1</sup>M.tech Student, Specialization VLSI,

<sup>2</sup>M.tech, Assistant professor Of Department Of E.C.E.

<sup>1,2</sup>Department Of E.C.E, Sir c.v. Raman Institute of Technology And Sciences, Tadipatri-515411, Andhra Pradesh, India.

**Abstract:** Reversible logic has become one in all the promising analysis directions in low power dissipating circuit style within the past few years and has found its applications in low power CMOS style, cryptography, digital signal process, optical scientific discipline and engineering. This paper presents a quantum price economical reversible full adder gate and Reversible Decoder in engineering. This gate will work on an individual basis as a reversible full adder & Decoder unit and needs just one clock cycle. The planned gate may be a universal gate within the sense that it may be wont to synthesize any whimsical mathematician functions. To implement reversible logic gates we tend to are planning Full adder and Decoder circuit by mistreatment the T-Spice simulation and calculate the ability consumption with TSMC018 nm Technology

any economical reversible logic style ought to minimize the garbage's also as constant inputs.

Computing systems provide off heat once voltage levels amendment from positive to negative: bits from zero to 1. Most of the energy required to create that amendment is given off within the type of heat. instead of dynamical voltages to new levels, reversible circuit components can bit by bit move charge from one node to ensuing. This way, one will solely expect to lose a moment quantity of energy on every transition. Reversible computing powerfully affects digital logic styles. Reversible logic components square measure required to recover the state of inputs from the outputs. it'll impact instruction sets and high-level programming languages also. Eventually, these also will need to be reversible to supply optimum potency.

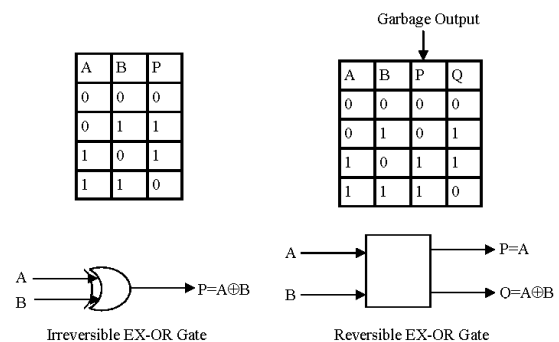
## I INTRODUCTION

Reversible logic has received nice attention within the recent years attributable to their ability to cut back the ability dissipation that is that the main demand in low power VLSI style. it's wide applications in low power CMOS and Optical informatics, polymer computing, quantum computation and engineering science. Irreversible hardware computation ends up in energy dissipation attributable to data loss

This paper presents a unique 4\*4 reversible gate particularly Peres Full Adder Gate (PFAG), that is, it's 4-input lines and 4-output lines. This gate is wont to understand any discretionary Boolean perform and thus universal. The hardware quality of this gate is a smaller amount compared to the present ones and needs just one clock cycle. The quantum realization value of this gate is simply eight and prepared to be used in current engineering science. Reversible logic style differs considerably from ancient combinatory logic style approaches. In reversible logic circuit the amount of input lines should be equal the amount of output lines, every output are used just the once and also the ensuing circuit should be acyclic. The output lines that don't seem to be used more square measure termed as garbage outputs. one in every of the foremost difficult tasks is to cut back these garbage's. Any reversible gate realizes solely the functions that square measure reversible. however several of the Boolean functions don't seem to be reversible. Before realizing these functions, we want to remodel those irreversible functions into reversible one. Any transformation formula that converts Associate in Nursing

Irreversible perform to a reversible one introduces input lines that square measure set to zero within the circuit's input aspect. These inputs square measure termed as constant inputs. Therefore,

## II. Irreversible & Reversible Logic Gates



### 2.1 MOTIVATION BEHIND REVERSIBLE LOGIC

High-performance chips cathartic massive amounts of warmth impose sensible limitation on however so much will we have a tendency to improve the performance of the system. Reversible circuits that conserve info, by world organization computing bits rather than throwing them away, can shortly supply the sole physically doable thanks to keep rising performance. Reversible computing will cause improvement in energy potency. Energy potency can basically have an effect on the speed of circuits like nano circuits and so the speed of most computing applications. to extend the movability of devices once more reversible computing is needed. {it can't'll} let circuit component sizes to cut back to atomic size limits and therefore devices will become additional moveable. though the hardware style prices incurred in close to future is also high however the facility

value and performance being additional dominant than logic hardware value in today’s computing era, the necessity of reversible computing can’t be unheeded.

2.2 REVERSIBLE LOGIC GATES

A reversible computer circuit is Associate in Nursing n-input n-output logic device with matched mapping. This helps to see the outputs from the inputs and conjointly the inputs is unambiguously recovered from the outputs. conjointly within the synthesis of reversible circuits direct fan-Out isn't allowed as one-to-many thought isn't reversible. but fan-out in reversible circuits is achieved mistreatment further gates. A reversible circuit ought to be designed mistreatment minimum variety of reversible logic gates. From the purpose of read of reversible circuit style, there square measure several parameters for crucial the quality and performance of circuits.

the quantity of Reversible gates (N): the quantity of reversible gates employed in circuit.

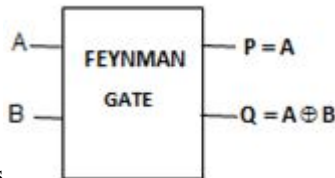
the quantity of constant inputs (CI): This refers to the quantity of inputs that square measure to be maintained constant at either zero or one so as to synthesize the given logical operate.

The number of garbage outputs (GO): This refers to the quantity of unused outputs gift in an exceedingly reversible logic circuit. One cannot avoid the rubbish outputs as these square measure terribly essential to realize changeableness.

III BASIC REVERSIBLE LOGIC GATES

3.1 Feynman Gate

Feynman gate may be a 2\*2 one through reversible gate as shown in figure one. The input vector is I(A, B) and also the output vector is O(P, Q). The outputs area unit outlined by P=A, Q=A B. Quantum price of a nuclear physicist gate is one. nuclear physicist Gate (FG) may be used as a repetition gate. Since a fan-out isn't allowed in reversible logic, this gate is helpful for duplication of the



desired outputs

Figure: 1 Feynman Gate

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Table:1 Truth table of Feymans gate

3.2 Double Feynman Gate (F2G)

Fig.2 shows a 3\*3 Double Feynman gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The outputs are defined by P = A, Q=A B, R=AC.

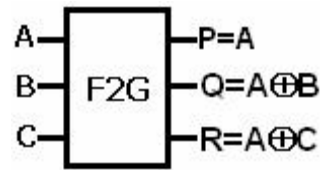


Figure: 2 Feynman Double Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

Table: 2 Truth table of double Feynman gates

3.3 Fredkin Gate

Fig 4 shows a 3\*3 Fredkin gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P=A, Q=A'B AC and R=A'C AB.

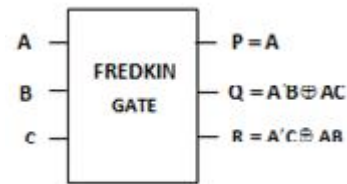


Figure: 3 Fredkin Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Table: 3 Truth table of fredkin gate

3.4 Peres Gate

Fig 5 shows a 3\*3 Peres gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P = A, Q = AB and R=AB C.

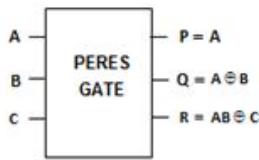


Figure: 4 Peres Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Table : 4 Truth table of peres gate

IV Full adder using two Peres Gates

A full-adder victimization 2 Peres gates is as shown in fig. The quantum realization of this shows that its quantum price is eight 2 Peres gates ar used. one 4\*4 reversible gate referred to as PFAG gate with quantum price of eight is employed to appreciate the multiplier factor

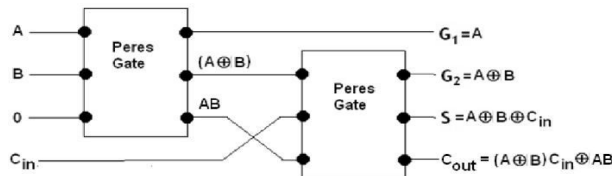


Figure: 5 Full adder using two Peres gates

4.1 Decoder circuit using F2G gates and FRG Gates

A decoder could be a device that will the reverse operation of associate degree encoder, undoing the encryption in order that the first info are often retrieved. constant methodology wont to cypher is sometimes simply reversed so as to decrypt. it's a combinatory circuit that converts binary info from n input lines to a most of 2n distinctive output lines.

Decoders ar the gathering of logic gates restored in an exceedingly specific approach such, for associate degree input combination, all outputs terms ar low except one. These terms ar the min terms. Thus, once associate degree input combination changes, 2 outputs can amendment. Let, there ar n inputs, therefore variety of outputs are 2n. There ar many styles of reversible decoders within the literature. To the simplest of out data, the styles from is that the solely reversible style that preserve parity too.

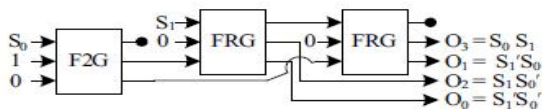


Figure: 6 Reversible Logic Decoder

V Applications:

Reversible computing could have applications in pc security and dealings process, however the most long profit are going to be felt alright in those areas that need high energy potency, speed and performance .it embody the world like

1. Low power CMOS.
2. Quantum pc.
3. Nano technology
4. Optical computing
5. Style of low power arithmetic and knowledge path for digital signal process (DSP).
6. Field Programmable Gate Arrays (FPGAs) in CMOS technology for very low power, high testability and self-repair

VI. Conclusion:

The reversible circuits type the essential structures of coming up with quantum computers. This paper presents the primitive reversible gates that ar gathered from the references and this paper shows the coming up with of complicated circuits mistreatment reversible gates. The paper will any be extended towards the digital style development mistreatment reversible logic circuits with pass junction transistor logic helps to form an occasional power circuits.

VII. References:

[1] Landauer, R., "Irreversibility and warmth generation within the computing process", IBM J. analysis and Development, 5(3): pp. 183-191, 1961.

[2] aeronaut, C.H., "Logical changeableness of Computation", IBM J. Research and Development, 17: pp. 525-532, 1973.

[3] Thapliyal H, M. B.Sshrinivas." a brand new Reversible TSG Gate and Its Application for coming up with economical Adder Circuits". Centre for VLSI and Embedded System Technologies International Institute of data Technology, Hyderabad, 500019, India

[4] Thapliyal H, M. B.Sshrinivas "Novel Reversible multiplier factor design mistreatment Reversible TSG Gate" pc Systems and Applications, 2006.

[5] L. Jamal, M. Shamsujjoha, and H. M. Hasan Babu, "Design of optimum reversible carry look-ahead adder with optimum garbage and quantum price," International Journal of Engineering and Technology, vol. 2, pp. 44–50, 2012.

[6] C. H. Bennett, "Logical changeableness of computation," IBM J. Res. Dev., vol. 17, no. 6, pp. 525–532, Nov. 1973. [Online]. Available: <http://dx.doi.org/10.1147/rd.176.0525>

[7] M. Nielsen and that i. Chuang, Quantum computation and quantum data. New York, NY, USA: university Press, 2000.

[8] M. P. Frank, "The physical limits of computing," Computing in Science and Engg., vol. 4, no. 3, pp. 16–26, May 2002. [Online]. Available: <http://dx.doi.org/10.1109/5992.998637>

[9] A. K. Biswas, M. M. Hasan, A. R. Chowdhury, and H. M. Hasan Babu, "Efficient approaches for coming up with reversible binary coded decimal adders," Microelectron. J., vol. 39, no. 12, pp. 1693–1703, Dec. 2008. [Online]. Available: <http://dx.doi.org/10.1016/j.mejo.2008.04.003>

[10] M. Perkowski, "Reversible computation for beginners," 2000, lecture series, 2000, Portland state university. [Online]. Available: <http://www.ee.pdx.edu/mperkows>

[11] S. N. Mahammad and K. Veezhinathan, "Constructing on-line testable circuits mistreatment reversible logic," IEEE Transactions on Instrumentation and mensuration, vol. 59, pp. 101–109, 2010.