Upgrading the Performance of VLSI Circuits using FinFETs

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***Abstract*—: In the world of integrated circuits, CMOS has lost it's credentialed during scaling beyond 32nm. The main drawback of using CMOS transistors are high power consumption and high leakage current. Scaling causes severe Short Channel Effects (SCE) which are difficult to suppress. As technology is scaled down, the importance of leakage current and power analysis for VLSI design is increasing since Short-channel effects cause an exponential increase in the leakage current and power dissipation. Multi-gate MOSFET technologies mitigate these limitations by providing a stronger control over a thin silicon body with multiple electrically coupled gates. Enormous progress has been made to scale transistors to even smaller dimensions to obtain fast switching transistors, as well as to reduce the power consumption. Even though the device characteristics are improved, high active leakage remain a problem. FinFET has become the most promising substitute to bulk CMOS technology because of reducing short channel effect and the similarity of the fabrication steps to the existing standard CMOS technology. FinFET device has a higher controllability, resulting relatively high *I*on/*I*off ratio. FinFET devices can be used to increase the performance by reducing the leakage current and power dissipation, because front and back gates both can be controlled.(independently or both simultaneously). In this paper, Dual-gate FinFET with shorted gates of either side is used for better performance to reduce the leakage and hence power consumption. In this work, the basic gates, combinational circuit and are modelled in HSPICE software using CMOS structures and FinFET structure are analysed and their performances like power consumption and speed are compared. Latch based on tied-gate FinFETs is proposed in this paper to simultaneously reduce the power consumption and the circuit area.**

***Keywords*— Short channel effects, FinFET, tied gate.**

I. Introduction

PLANAR transistor scaling in deep-sub micro meter CMOS technology has approached its limits at sub-22-nm nodes, owing to very poor electrostatic integrity, which is manifested as degraded short-channel behaviour and high leakage current[1][8]. Multigate field-effect transistors (FETs) overcome these problems because of tighter control of the channel potential by multiple gates wrapped around the body.[1][8][9]Amongst multigate FETs, FinFETs have emerged as the best candidate structures from a fabrication perspective[1][18][19][20] .The FinFET device structure consists of a silicon fin surrounded by shorted or independent gates on either side of the fin, typically on a silicon-on-insulator substrate. In the SG mode of operation, the two gates are biased together to turn on the device, providing maximum gate drive.

As devices get smaller further and further, the problem with conventional MOSFETs are increasing [1][8]. We are facing short channel effects problems such as VT roll off, drain induced barrier lowering (DIBL), increasing leakage current and so on. Solving one problem leads to another. To solve the problem several MOSFET has been introduced such as double gate, FinFET, Tri-gate, Fore-gate, all-around gate and so on [1][8]. We will discuss here the electrostatic characteristic of FinFET such as current – voltage curves. The distinguishing characteristic of the FinFET is that the conducting channel is wrapped by a thin silicon "fin", which forms the gate of the device. The thickness of the fin (measured in the direction from source to drain) determines the effective channel length of the device. It is very important to know the characteristics of MOSFET to work properly from this aspect we tried to discuss the qualitative feature of FinFET characteristics.[1]
Theory: All the MOSFET characteristics are expressed as functions of the values of the surface potential at the source and drain ends. In the threshold voltage approach separate solutions are available for different regions of MOSFET operation (Figure 1). For FinFET Figure 1 Device structure used in this study.(FinFET consists of a vertical Si fin controlled by self aligned double gate)

Linear Region: It is the region in which Ids, increases linearly with Vds, for a given Vg (> Vth). To a first approximation, Ids, in the linear region is given Idc = 2 µ Cox W/L {Vg -Vth - Vds/2} Vds where µ is mobility of the carriers in the channel (inversion) region, Cox is the gate oxide capacitance per unit area, W/L is device width to length ratio and Vth is threshold voltage.

Saturation Region: In this region Ids no longer increases as Vds increases. Once more to a first rough calculation, Ids in the saturation region is given by

$$I_{ds} = \mu C_{ox} \frac{W}{L} \frac{(V_g - V_t)^2}{2m}$$

where , $m = 1 + \frac{3\, t_{ox}}{x_d}$

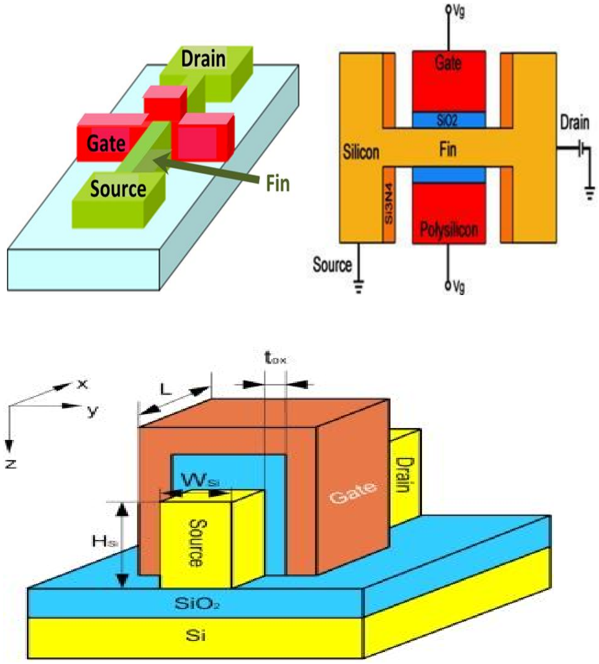


Figure 1. Schematic of a FinFET structure

Xd is the depletion layer thickness and is the oxide thickness showing that Ids, does not depend on Vds

Cut-Off Region. This is the region where Vg< Vth so that no channel subsist between the source and the drain, consequential in Ids=0.In fact for Vg< Vth, drain current follows an exponential decompose is referred to sub-threshold current. The low electron concentration results in low electric field along the channel and as a result the sub-threshold current is primarily owing to diffusion of carriers. The current in sub-threshold region is approximated as

$$I_{ds} = \mu \frac{W}{L} kT n_i t_{si} e^{\frac{q(v_g - \Delta\varphi)}{kT}} (1 - e^{-\frac{qV_{ds}}{kT}})$$

Δφ is the work function difference between the gate electrode and the almost intrinsic silicon body. The FinFET characteristics (input & output) are shown below.

Features of FinFET: Most important Features of FinFET are:(1). Ultra thin Si fin for suppression of short channel effects. (2) Raised source/drain to reduce parasitic resistance and (3) improve current drive. (4) Symmetric gates yield great performance, but can built asymmetric gates that target VT. (5) FinFETs are designed to use multiple fins to achieve larger channel widths. Source/Drain pads connect the fins in parallel. As the number of fins is increased, the current through the device increases. For eg: A 5 fin device 5 times more current than single fin device. (6) The main advantage of the FinFET is the ability to drastically reduce the short channel effect.

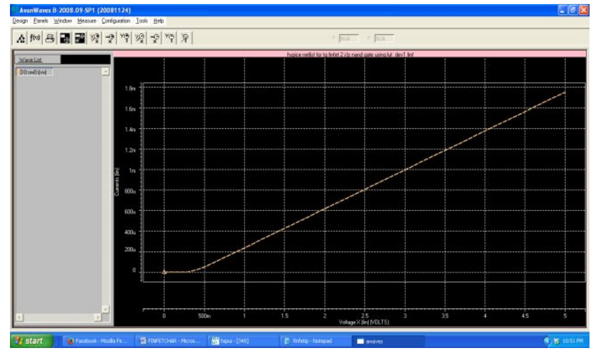


Figure.2. Transfer characteristics of FinFET

In spite of his double gate structure, the FinFET is closed to its root, the conventional MOSFET in layout and fabrication. The tied gate FinFET model used for simulation purpose is LUT_Dev1 & its specification is as follows:
Model files in LUT_Dev1 are for a tied-gate FinFET device with

1. Physical gate length = 4.905nm
2. Oxide thickness = 1.09nm (front and back)
3. Body thickness = 2.725nm
4. Fin height = 10.9nm
5. Source/drain doping = 1e20 /cm3
6. Source-side under lap = 1.09nm
7. Drain-side under lap = 1.09nm

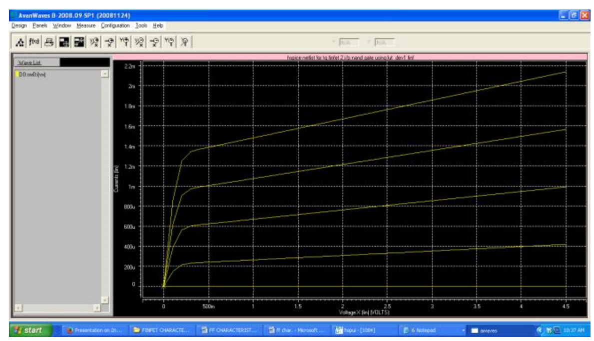


Figure. 3 Output characteristics of FinFET

Figure.2 Tell us there is no current flowing up to threshold voltage but after this voltage current start over drain current increasing. This is ideal condition. In practical situation current flow before threshold voltage reaching. Figure.3. Indicate increasing drain current with increasing drain voltage this condition is true up to pinch off voltage then there is no effect of drain voltage. From FinFET Characteristics, the value of ION (On current) will be 2.39e-04 since VGS=1.0 & VDS=0.45.
Ioff (leakage current) will be 2.18e-14 since Vgs=0.0 still current flowing at VDS=0.00 &

Isub (sub threshold current) will be 4.96e-09 since Vgs=0.0 still current flowing at VDS=0.45.

DIBL:d(Vth)/d(Vds)
Drain-induced barrier lowering or DIBL is one of the short-channel effects in MOSFETs in which threshold voltage of the transistor is reduced when drain voltages is increased. In this paper, the change in Vth is 5x10e-03 for a change in Vds of 0.1 volts. Therefore for a change of 1volt of Vds there is a change of 50mVolt of Vth. Hence DIBL is 50mV/Volt.

II. INVERTER USING FINFET & CMOS:

Below are the figures of CMOS inverter & Inverter using FinFET tied gate.

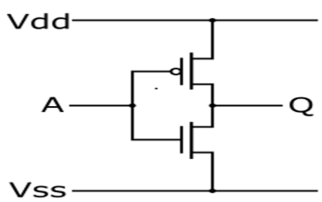


Figure.4.Static CMOS inverter

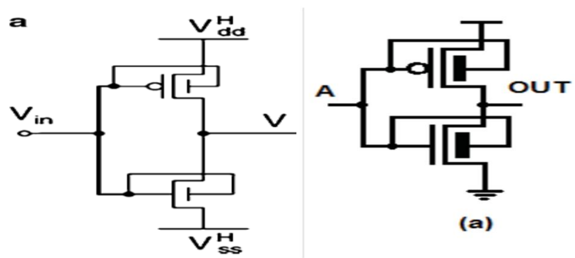


Figure.5. Inverter using FinFETs (tied gate)

CMOS inverters (Complementary MOSFET Inverters) are some of the most widely used and adaptable MOSFET inverters used in chip design. They operate with very little power loss and at relatively high speed. Else furthermore, the CMOS inverter has good logic buffer characteristics, in that, its noise margins in both low and high states are large. A CMOS inverter contains a PMOS and a NMOS transistor connected at the drain and gate terminals, a supply voltage VDD at the PMOS source terminal, and a ground connected at the NMOS source terminal, were VIN is connected to the gate terminals and VOUT is connected to the drain terminals.(See figure 4). It is important to notice that the CMOS does not contain any resistors, which makes it more power efficient that a regular resistor-MOSFET inverter. As the voltage at the input of the CMOS device varies between 0 and 5 volts, the state of the NMOS and PMOS varies accordingly. If we model each transistor as a simple switch activated by VIN, the inverter's operations can be seen very easily: The CMOS inverter is an important circuit device that provides quick transition time, high buffer margins, and low power dissipation: all three of these are desired qualities in inverters for most circuit design. It is quite clear why this inverter has become as popular as it is.

A. LOGIC GATES: A logic gate is an elementary building block of a digital circuit. Most logic gates have two inputs and one output. At any given moment, every terminal is in one of the two binary conditions *low* (0) or *high* (1), represented by different voltage levels. The logic state of a terminal can, and generally does, change often, as the circuit processes data. In most logic gates, the low state is approximately zero volts (0 V), while the high state is approximately five volts positive (+5 V).There are seven basic logic gates: AND, OR, XOR, NOT, NAND, NOR, and XNOR.[4][5].

NAND GATE using FINFETs:

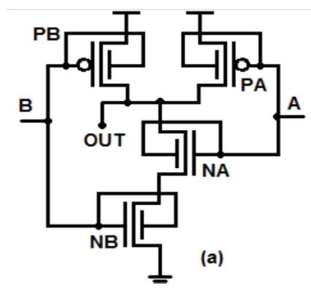


Figure.6.NAND Gate using FinFETs (Tied Gate)

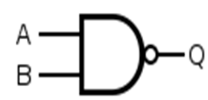


Figure.7. NAND Gate symbol

TABLE 1: TRUTH TABLE OF NAND GATE

Input A	Input B	Output Q
0	0	1
0	1	1
1	0	1
1	1	0

B. NAND Gate: The NAND Gate represents the complement of the AND operation. The symbol for the NAND gate consists of an AND symbol with a bubble on the output, denoting that a complement operation is performed on the output of the AND gate. The truth table and the graphic symbol of NAND gate is shown in the figure above. [4][5]

Universal Gates: NAND and NOR Gates are called Universal Gates because all the other gates can be created by using these gates. A universal gate is a gate which can implement any Boolean function without need to use any other gate type. The NAND and NOR gates are universal gates. In practice, this is advantageous since NAND and NOR gates are economical and easier to fabricate and are the basic gates used in all IC digital logic families. In fact, an AND gate is typically implemented as a NAND gate followed by an inverter not the other way around. Likewise, an OR gate is typically implemented as a NOR gate followed by an inverter not the other way around.[4][5]

C. COMBINATIONAL CIRCUITS: In combinational circuit the output at any instant of time depends only on the levels present at input terminals [4][5]. Combinational logic is used in computer circuits to perform Boolean algebra on input signals and on stored data. The combinational circuit does not use any memory. The previous state of input does not have any effect on the present state of the circuit..

D. HALF ADDER: Half adder is a combinational arithmetic circuit that adds two numbers and produces a sum bit (S) and carry bit (C) as the output [4][5]. If A and B are the input bits, then sum bit (S) is the X-OR of A and B and the carry bit (C) will be the AND of A and B. From this it is clear that a half adder circuit can be easily built using one X-OR gate and one AND gate. In this paper we are comparing performance of combinational circuit, half adder using FinFETs & others CMOS models.

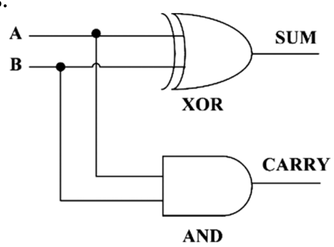


Figure.8.Half Adder

Inputs		Outputs	
A	B	Carry	Sum
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

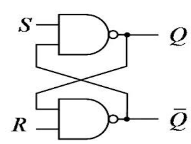
TABLE 2. TRUTH TABLE OF HALF ADDER

Below are the simulated waveform results which are half adder using FinFETs (Figure.11). First waveform is signal input A & second waveform is signal input B. Third waveform is output CARRY & fourth is output SUM. The waveforms are following the truth table of half adder. The waveforms below in figure.11 are shown for Half Adder using FinFET. The table no.6 below shows comparison of performance of Half Adder in terms of power dissipation & speed. The power dissipation of the circuit in case of FinFET is least & hence preferred over other CMOSs models. Also the time taken is less which means speed is also improved using FinFETs.

E. SEQUENTIAL CIRCUITS: In digital circuit theory, sequential logic is a type of logic circuit whose output depends not only on the present value of its input signals but on the past history of its inputs. That is, sequential logic has state (memory) while combinational logic does not. Virtually all circuits in practical digital devices are a mixture of combinational and sequential logic.[4][5]

F. S R LATCH using NAND gates USING FINFETs: The simplest way to make any basic single bit set-reset SR flip-flop is to connect together a pair of cross-coupled 2-input NAND gates as shown, to form a Set-Reset Bistable also known as SR NAND Gate Latch, so that there is feedback from each output to one of the other NAND gate inputs. This device consists of two inputs, one called the *Set*, S and the other called the *Reset*, R with two corresponding outputs Q and its inverse or complement Q (not-Q) as shown below.

TABLE 3:TRUTH TABLE & S R LATCH LOGIC DIAGRAM :

Symbol	S	R	Q	Q’
	0	0	RACE	RACE
	0	1	0	1
	1	0	1	0
	1	1	No change	No change

The waveforms below in fig.12 is shown for S-R Latch using FinFET The table below shows comparison of performance of S-R Latch in terms of power dissipation & speed. The power dissipation of the circuit in case of FinFET is least & hence preferred over other CMOS models. Also the time taken is less which means speed is also improved using FinFETs.

III. RESULTS: GRAPHS & TABLES

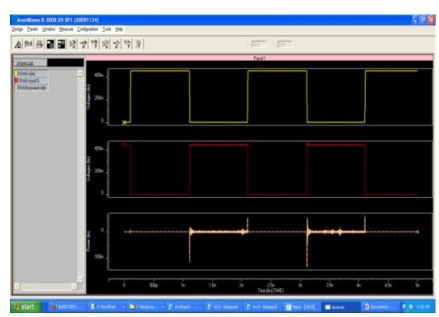


Figure.9: Inverter using FinFET

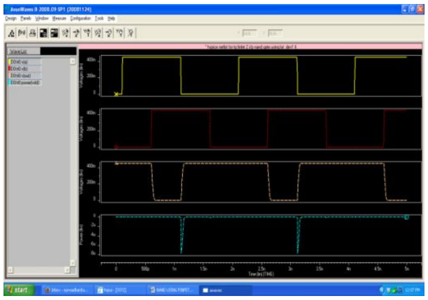


Figure.10: NAND Gate using FinFET

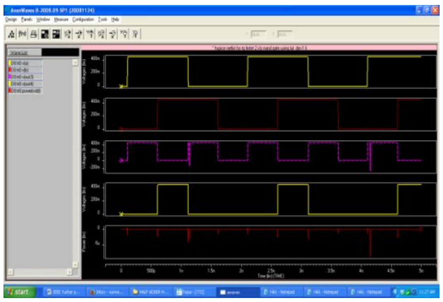


Figure.11: Half Adder using FinFETs

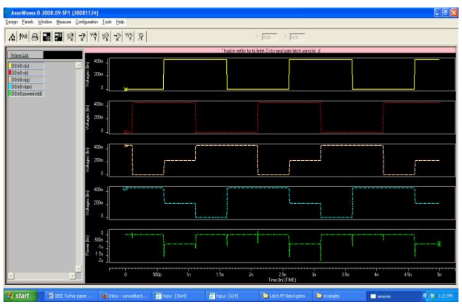


Figure.12:SR LATCH(NAND) using FinFETs

TABLE.4: NAME OF CIRCUIT: INVERTER USING DIFFERENT MODELS

	Total Power dissipation (watts)	Leakage power dissipation (watts)	Time taken (sec)
FinFET	1.846e-09	9.232e-18	5.34(s)
IBM	2.432e-07	1.216e-15	5.35(s)
TSMC	5.603e-07	2.802e-15	5.35(s)
PTM	1.992e-05	9.959e-14	5.35(s)
CMOS model level 1	2.176e-04	1.088e-12	6.40(s)

TABLE.5: NAME OF CIRCUIT: NAND GATE USING DIFFERENT MODELS

	Total Power dissipation (watts)	Leakage power dissipation (watts)	Time taken (sec)
FinFET	8.316e-08	4.158e-16	5.34(s)
IBM	1.852e-06	9.259e-15	7.38(s)
TSMC	5.975e-06	2.988e-14	5.35(s)
PTM	2.578e-03	1.289e-11	5.34(s)
CMOS model level 1	3.110e-06	1.555e-14	6.33(s)

TABLE.6: NAME OF CIRCUIT: HALF ADDER USING DIFFERENT MODELS

	Total Power dissipation (watts)	Leakage power dissipation (watts)	Time taken (sec)
FinFET	4.846e-08	2.423e-16	5.47(s)
IBM	2.269e-04	1.134e-12	5.34(s)
TSMC	2.791e-04	1.395e-12	5.34(s)
PTM	6.650e-03	3.325e-11	6.34(s)
CMOS model level 1	7.962e-05	3.981e-13	6.35(s)

TABLE.7: NAME OF CIRCUIT: S R LATCH USING DIFFERENT MODELS

	Total Power dissipation (watts)	Leakage power dissipation(watts)	Time taken (sec)
FinFET	2.015e-07	1.008e-15	5.34(s)
IBM	5.139e-04	2.569e-12	5.42(s)
TSMC	8.860e-04	4.430e-12	5.33(s)
PTM	2.790e-03	1.395e-11	6.41(s)
CMOS	1.497e-04	7.487e-13	5.33(s)

IV. CONCLUSIONS

We have seen in the above simulated waveforms & tables that by using FinFETs in VLSI circuits power dissipation can be reduced and speed can be improved. Using FinFETs total power dissipation, leakage power dissipation & time taken (elapse time) are least compared to other CMOS models. Hence use of FinFETs in VLSI circuits is essential.

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