Implementation of Three Level Integrated AC-DC Converter with Pulse Width Modulation

K. Deepak Singh[*1], Manish G Rathi[*2],

[*1]*EEE Department PG student*
PDA College of Engineering Gulbarga, Karnataka, India
[*2]*EEE department, Assistant Professor*
PDA College of Engineering Gulbarga, Karnataka, India

Abstract— **In this paper, implementation of three-level integrated ac–dc converter with pulse width modulation is presented. The proposed converter combines with the operation of the boost power factor correction and the three-level dc–dc converter. The converter is made to operate with two independent controllers which are combined in a single converter. Input controller does PFC and regulates dc bus, output controller regulates the output voltage. Converter operation is explained and power factor is improved in this paper. Finally the efficiency of the new converter is compared with that of previously proposed converter.**

*Keywords—***AC-DC converters, PWM (Pulse Width Modulation), Three level converters, PFC(power factor correction),single stage converters.**

I. INTRODUCTION

Advancement in the research of Power electronic converter is still increasing with the rapid demands in the industry. In search of better efficiency, cost, design flexibility, low harmonics in converters, many converters had been proposed so far. Besides multilevel converters plays a major role in increasing demands. Mostly the AC-DC converters are implemented with PFC to comply with harmonic standards like IEC 1000-3-2[1].Based on this; PFC methods are of two types namely passive and active methods. Passive methods are simple and inexpensive which uses L&C components to filter low frequency input current harmonics & shapes input current to improve power factor. But this makes the converter huge and bulky in size which is less preferred. Due to this active PFC are used nowadays..

Active PFC methods can be implemented either two stage or single stage approach. Two stage converters uses two controllers i.e. one controller for PFC and another controller for output regulation. This method gives poor efficiency in light loads, more losses &expensive too. But it is cost effective for higher power applications. In single stage converters it uses single controller for both PFC and regulation of output voltage. It is used for fast regulation of output voltage which works on steady state. On the analysis of previously proposed converters like voltage fed, current fed and resonant converters, some of their drawbacks are:

1) In current fed converters boost inductors are used at the input of full bridge converters. This gives close to unity power factor but it may lead to high voltage overshoots across the dc

bus voltage due to lack of energy store capacitors. Besides it also results in large low frequency 120 Hz ripple output voltage [13].

2) The resonant converters are good as overall but controlled by varying switching frequency [17],[18]. This makes difficult to design especially their magnetic components as it must operate with wide switching frequency.

3) In voltage fed single stage converters ,they have large energy storage capacitors connected across the primary of dc bus and it prevents voltage overshoots .It also prevents the 120 Hz component from output voltage. By doing so, it eliminates the problem faced by current fed and resonant converters. The converters are made to operate with an output inductor current to prevent the dc-bus voltage from becoming excessive. Still voltage fed converters may suffer from problems of excessive dc bus voltage under high input &low output load due to single controller. Doing so results in the need for components that can handle high peak currents and additional output filtering to remove ripple [12-14].

There is need of converter which solves previous problems like excessive dc bus voltage due to lack of dedicated controller, large output ripple, distorted input currents, design flexibility and in terms of cost factor. Considering all this a three level integrated converter has been proposed which uses the multilevel concept [15][16]. With multilevel topologies, the dc bus voltage can be allowed to reach higher levels that are possible with a two-level topology as the converter components are exposed to half the dc bus voltage and, thus, have half the voltage stress. Freeing up the allowable limit of dc bus voltage allows the aforementioned limitations on output and input currents to be eased so that the converter can be made to operate with an output current that has less ripple and an input current that is less distorted than that of a two-level converter.

.

II. PULSE WIDTH MODULATION

The proposed converter is made to operate with the PWM technique. PWM signals are pulse trains which are applied to the gate of switches to perform the operation of converter. The pulse trains are fixed frequency and magnitude and variable pulse width. There is one pulse of fixed magnitude in every PWM period. But the width of the pulses changes from period to period according to a modulating signal. When a PWM

signal is applied to the gate of a power transistor, it causes the turn on and turns off intervals of the transistor to change from one PWM period to another PWM period according to the same modulating signal& consequently working of converter starts. The frequency of a PWM signal must be much higher than that of the modulating signal, the fundamental frequency, such that the energy delivered to the load depends mostly on the modulating signal. The control of output voltage is done using pulse width modulation. The commonly used techniques are

1. Single pulse width modulation.
2. Multiple pulse width modulation.
3. Sinusoidal pulse width modulation.
4. Modified sinusoidal pulse width modulation.
5. Phase displacement control
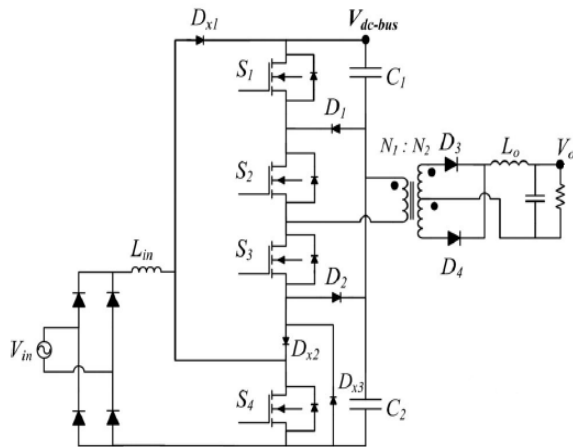
.Fig 1: Proposed converter

III. CONVERTER OPERATION

The input controller consists of boost inductor Lin, boost diode Dx1&switch S4 which is shared by multilevel dc-dc section. It performs PFC &regulates primary of dc bus capacitors by sending appropriate signals to S4 which is done by controlling D2& then adding the duty cycle of D2 to D1(D1&D2 are shown in fig 2). Besides regulation of dc bus voltage is done by sending gate signals to S1 to S4 by controlling duty cycle of D1.In short S4 perform two tasks (D1) participate in control of output voltage and other part (D2) regulate dc bus voltage. The switches S2 and S3 are ON for half a switching cycle, but are never ON at the same time. In the figure the diode rectifier bridge output is replaced by a rectified sinusoidal source (Vrec) and the thick lines represent the paths of current conduction.

The proposed converter has eight modes of operations:

1) Mode 1 (t0 ≤ t ≤ t1) [fig 3(a)]: During this mode, switches S1 and S2 are ON and energy from dc-bus capacitor C1 is transferred to the output load. In the output section, a positive voltage of (Vpri /n) –Vo (where n is the ratio of

primary to secondary transformer turns) is impressed across Lo and the current through it rises.

2) Mode 2 (t1 ≤ t ≤ t2) [fig 3(b)]**:** In mode 2, S1 and S2 remain ON and S3 turns ON. The energy from dc bus capacitor C1 is transferred to the output load. At the same time, the diode bridge output voltage (Vrec) is impressed across input inductor Lin so that the current flowing through this inductor rises.

3) Mode 3 (t2 ≤ t ≤ t3) [fig 3©]: In mode 3, S1 and S2 remain ON and S3 turns ON. The energy from dc-bus capacitor C1 is transferred to the output load. At the same time, the diode bridge output voltage Vrec is impressed across input inductor Lin so that the current flowing through this inductor rises voltage Vrec is impressed across input inductor Lin, so that the current flowing through this inductor rises.

4) Mode 4 (t3 ≤ t ≤ t4) [fig3 (d)]: In mode 4, S1 and S2 are OFF and S4 is ON. The current in the primary of the transformer charges capacitor C2 through the body diode of S3 and Dx3.

5) Mode 5 (t4 ≤ t ≤ t5) [fig 3(e)]: In mode 5, S3 and S4 are ON. Energy flows from capacitor C2 flows into the load while the current flowing through input inductor Lin continues to rise.

6) Mode 6 (t5 ≤ t ≤ t6) [Fig 3(f)]: In mode 6, S4 turns off. The current in input inductor flows thorough the diode Dx1 to charge the capacitors C1 and C2.The current in the transformer primary flows thorough the S3 and D2.This mode ends when the inductor current reaches zero. Also during this mode, the load inductor current freewheels in the secondary of the transformer.

7) Mode 7 (t6 ≤ t ≤ t7) [Fig 3(g)]: In mode 7, the load inductor current freewheels in the secondary of the transformer. This mode ends when the switches S3 turns off.

8) Mode 8 (t7 ≤ t ≤ t8) [Fig 3(h)]: In mode 8, S3 is OFF and the current in the primary of the transformer charges capacitor C1 through the body diodes of S1 and S2.Finally, converter re-enters Mode 1.
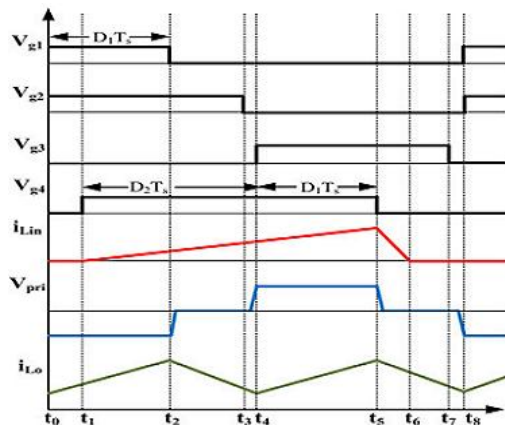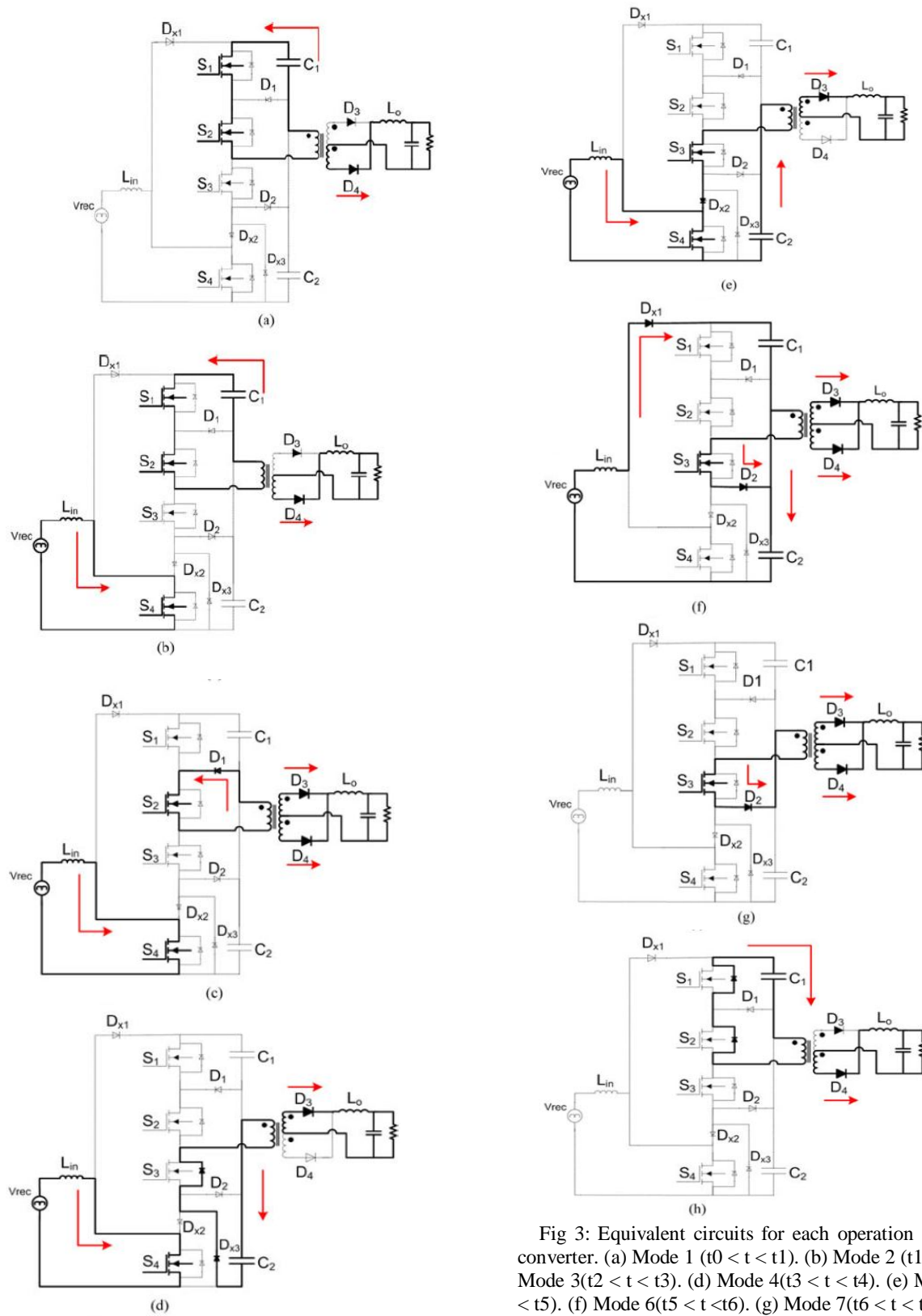

Fig 2: Waveforms explaining of operation of converter.

Fig 3: Equivalent circuits for each operation stage for the converter. (a) Mode 1 (t0 < t < t1). (b) Mode 2 (t1 < t < t2). (c) Mode 3(t2 < t < t3). (d) Mode 4(t3 < t < t4). (e) Mode 5(t4 < t < t5). (f) Mode 6(t5 < t <t6). (g) Mode 7(t6 < t < t7). (h) Mode 8 (t7 < t < t8)

IV.SIMULATION DIAGRAM OF PROPOSED CONVERTER

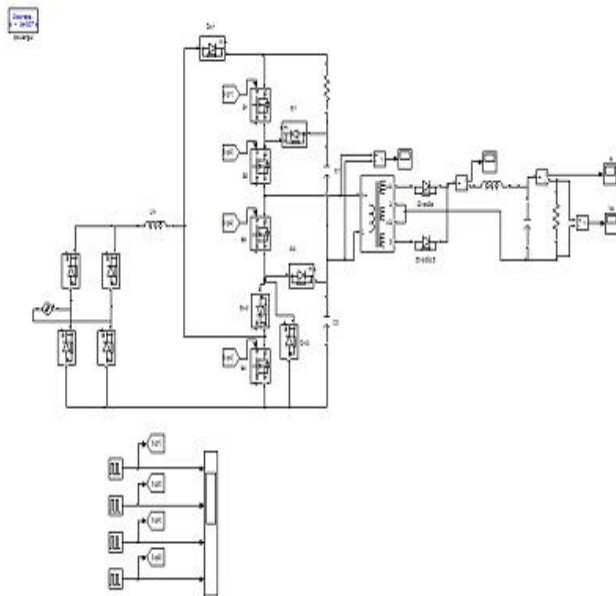Fig 4: Simulation diagram of Converter.

.

V.RESULTS AND DISCUSSION

It is assumed that the input current is discontinuous, the decoupling of the input controller and output controller can occur because the crossover frequencies of the two loops are very different. The crossover frequency of the input controller is much lower than that of the output controller, which converts the intermediate dc-bus voltage into the desired output voltage. As the two crossover frequencies are far apart, it is therefore possible to consider the design of one controller to be separate from that of the other. Since the two controllers are decoupled, the standard designs for an ac–dc boost converter controller and a dc–dc full-bridge converter controller can also be used.

The proposed converter has the following advantages:

1) Reduced cost: The converter is cheaper than a conventional two-stage converter. Replacing a switch and its associated gate drive circuitry with four diodes reduces cost considerably even though the component count seems to be increased.

2) Better performance: The proposed single-stage converter can operate with a better input power factor for universal input line applications than a single-controller, single-stage because it does have a dedicated controller for its input section that can perform PFC and regulate the dc-bus voltage. The presence of a second controller also allows the converter to operate with better efficiency and with less output ripple as each section.

.3) Improved light-load efficiency: The proposed converter can be designed so that it has a conventional dc-bus voltage of 400 V. As the converter is a multilevel converter, a 400 V dc bus means that each switch will be exposed to a maximum voltage of 200 V. Doing so results in 75% reduction in turn on losses when the converter is operating under light-load conditions.

4) Increased design flexibility: As converter is a multilevel converter, it can also be operated with high dc-bus voltage (800V), standard dc-bus voltage (400V),or any dc-bus voltage 400V<V_{bus}<800.There is flexibility in the level that the dc-bus voltage is set means that there is considerable flexibility in the design of the converter. But it will have lower heavy-load efficiency because of increased conduction losses as switch *S*4 must conduct both the input current and the full-bridge current. As a result, when determining whether to use the proposed converter versus a conventional two-stage converter, the main tradeoff that needs to be considered is lower cost and improved light-load efficiency versus heavy-load efficiency.
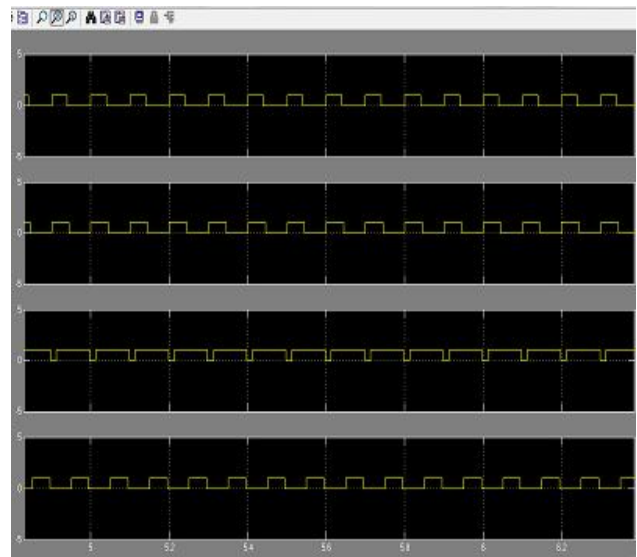

Fig 5: PWM used in simulation circuit. (S1, S2, S4 & S3)

Value for Output Inductor (Lo):

$$L_{o,\min} \geq \frac{V_o^2}{0.5\,P_{o,\max}}\frac{1-D_m}{2}\frac{T_{\mathrm{SW}}}{2}.$$

Value for Inductor (Lin):

.

$$L_{\mathrm{in},\max} < \frac{[\![(V_{\mathrm{bus},\min})]\!]^2 * D_{\max} * (1-D_{\max})^2}{2P_{o,\max}f_{\mathrm{SW}}}$$

Where, fSW= switching frequency,
        D=duty cycle,
Po= output power,Tsw=switching time,Vo=output voltage,
V bus=dc bus voltage.

The output waveforms based on the simulation results are given as following of the converter can be made to operate in an optimal manner.
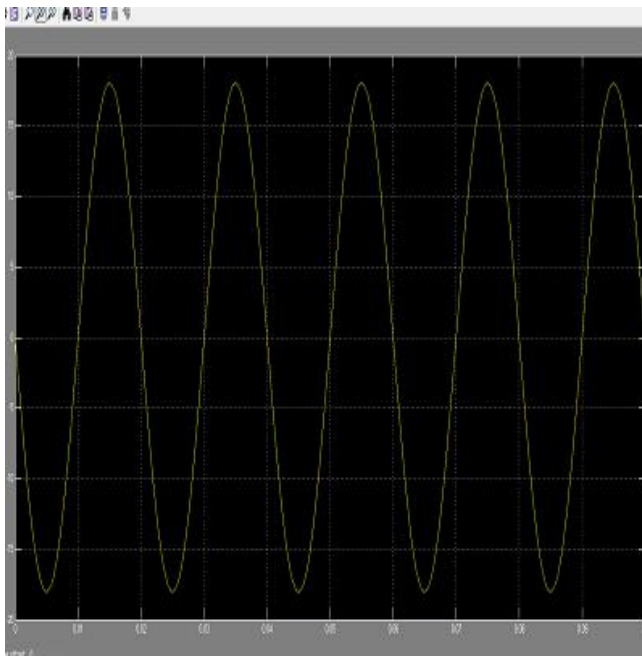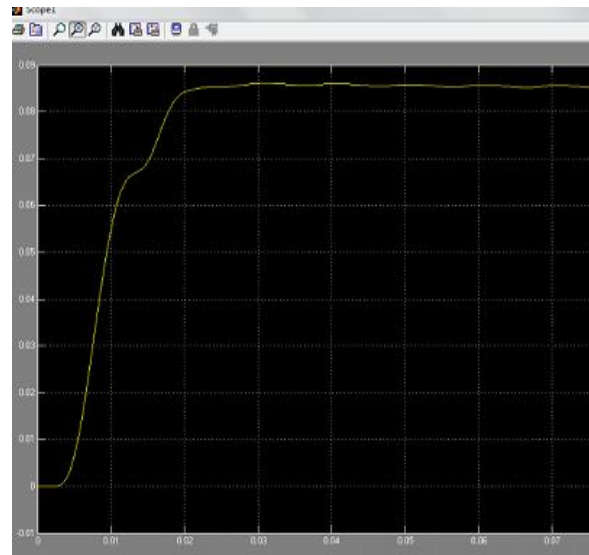
Fig 6: Input current waveforms.
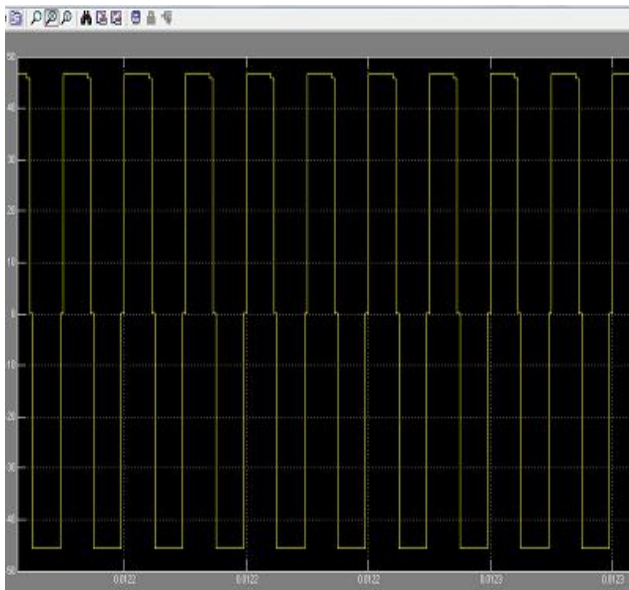
Fig 8: Output current after filtering

Fig 7: Three level output at of inverter (at the primary of transformer)
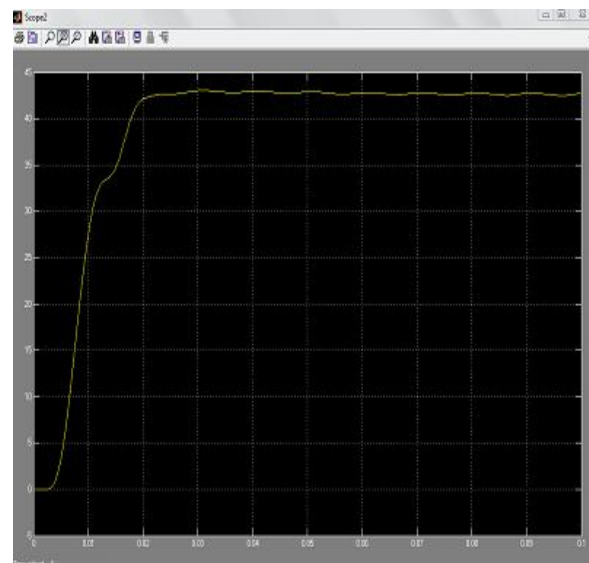
Fig 9: Output voltage

VI. CONCLUSION

A new single-stage ac–dc converter is proposed in the paper. This converter is operated with two controllers, one controller that performs input PFC and a second controller that regulates the output voltage. The specific feature of this converter is that it combines the performance of two-stage converters with the reduction of cost of single-stage converters. Besides design complexity also much reduced unlike resonant converters. This converter provides constant output voltage with improved power factor. This allows for greater flexibility in the design of the converter and ultimately improved performance.Experimental results that confirm the feasibility of the converter.

REFERENCES

[1] D. D. C. Lu, D. K. W. Cheng, and Y. S. Lee, "Single stage AC–DC power-factor-corrected voltage regulator with reduced intermediate bus voltage stress," Proc. Inst. Elect. Eng.—Elect. Power Appl., vol. 150, no. 5, pp. 506–514, Sep. 2003.

[2] Comparison Between CCM Single-Stage And Two-Stage Boost PFC Converters* Jindong Zhang1, Milan M. Jovanoviü2, and Fred C. Lee1.

[3] H. S. Athab and D. D.-C. Lu, "A high-efficiency ac/dc converter with Quasi-active power factor correction," *IEEE Trans. Power Electronic*, vol. 25, no. 5, p. 1103-1109, May 2010.

[4] J.-Y. Lee, "Single-stage AC/DC converter with input-current dead-zone control for wide input voltage ranges," IEEE Trans. Ind. Electron., vol. 54,no. 2, pp. 724–732, Apr. 2007.

[5] D. D.-C. Lu, H. H.-C. Iu, and V. Pjevalica,"A single-stage AC/DC converter with high power factor, regulated bus voltage, and output voltage," IEEE Trans. Power Electron., vol. 23, no. 1, pp. 218–228, Jan. 2008.

[6] H. Ma, Y. Ji, and Y. Xu, "Design and analysis of single-stage power factor correction converter with a feedback winding," IEEE Trans. Power Electron., vol. 25, no. 6, pp. 1460–1470, Jun. 2010.

[7] H. S. Athab and D. D.-C. Lu, "A high-efficiency ac/dc converter with quasi-active power factor correction," IEEE Trans. Power Electron.,vol. 25, no. 5, p. 1103-1109, May 2010.

[8] J. M. Kwon, W. Y. Choi, and B. H. Kwon, "Single-stage quasi-resonant flyback converter for a cost-effective PDP sustain power module," IEEE Trans. Ind. Electron., vol. 58, no. 6, pp. 2372–2377, Jun. 2011.

[9] H. J. Chiu, Y. K. Lo, H. C. Lee, S. J. Cheng, Y. C. Yan, C. Y. Lin,T. H. Wang, and S. C. Mou, "A single-stage soft-switching fly back converter for power-factor-correction applications," IEEE Trans. Ind. Electron.,vol. 57, no. 6, pp. 2187–2190, Jun. 2011.

[10] H. Athab and D. Lu, "A single-switch ac/dc fly back converter using a CCM/DCM quasi-active power factor correction front-end," IEEE Trans. Ind. Electron., vol. 59, no. 3, pp. 1517–1526, Mar. 2012.

[11] N.Golbon and G.Moschopoulos, "A low-power ac–dc single-stage converter with reduced dc bus voltage variation," IEEE Trans. Power Electron.,vol. 27, no. 8, pp. 3714–3724, Jan. 2012.

[12] P. K. Jain, J. R. Espinoza, and N. Ismail, "A single-stage zero-voltage zero-current-switched full-bridge DC power supply with extended load power range," IEEE Trans. Ind. Electron., vol. 46, no. 2, pp. 261–270, Apr. 1999.

[13] G. Moschopoulos, "A simple AC–DC PWM full-bridge converter with integrated power-factor correction," IEEE Trans. Ind. Electron., vol. 50, no. 6, pp. 1290–1297, Dec. 2003.

[14] P. Das, S. Li, and G. Moschopoulos,"An improved AC–DC single-stage full-bridge converter with reduced DC bus voltage," IEEE Trans. Ind. Electron., vol. 56, no. 12, pp. 4882–4893, Dec. 2009.

[15] M. S. Agamy and P. K. Jain, "A three-level resonant single-stage power factor correction converter: analysis, design, and implementation industrial electronics," IEEE Trans. Ind. Electron., vol. 56, no. 6, pp. 2095–2107,Jun. 2009.

[16] Mehdi Narimani,student member,IEEE,&Gerry Moschopoulos,Senior Member ,IEEE, —A Three level integrated AC-DC Converter,.IEEE trans.Vol.29,No.4,april 2014.

[17] M. S. Agamy and P. K. Jain, "A variable frequency phase-shift modulated three-level resonant single-stage power factor correction converter," IEEE,Trans. Power Electron., vol. 23, no. 5, pp. 2290–2300, Sep. 2009.

[18] M. S. Agamy and P. K. Jain, "An adaptive energy storage technique for efficiency improvement of single-stage three-level resonant AC/DC converters," IEEE Trans. Power Electron., vol. 47, no. 1, pp. 176–184, Sep.2011.