Area Efficient Low Power Compressor Design Using GDI Technique

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***Abstract*— Compressors are major components of the present multiplier designs. In multipliers maximum amount of power is consumed during the partial product addition. For higher order multiplication, a huge number of adders or compressors are used to perform the partial product addition. Using compressor adders, that can add four, five , six or seven bits at a time, the number of full adders and half adders can be reduced and thus area and power consumed also gets reduced. These compressor adders are designed by merging binary counter property with compressor property. In this paper, designs of 4:3, 5:3, 6:3, 7:3 compressors based on Gate Diffusion input technique have been presented. The designs are synthesized and analysed using Cadence Virtuoso tool in 180nm technology. When compared with CMOS based compressors, the proposed compressors show reduction in area and power ranging from 38.8% to 65.26% and 33.3% to 40% respectively**.

Keywords—**Compressor, low-power, Gate diffusion input technique, multiplier, binary counter.**

I. INTRODUCTION

With the increasing demand for portable equipments, the need for area and power efficient VLSI circuits is increasing day by day. The digital signal processors (DSPs), FIR filters and image processors are the most widely used processing units in the complex VLSI circuits. Multipliers are the main element of all these processing units.

A multiplier is typically composed of three stages – partial product generation stage, partial product addition stage and final addition stage.

In the first stage, multiplicand and multiplier are multiplied bit by bit to generate partial products. The second stage is the most important stage as it is the most complicated and determines the speed and power consumption of overall multiplier. The addition of the partial products contributes most to the overall delay, area and power consumption due to which the demand of high speed and low power adders is continuously increasing.

Compressor adders have been widely employed in many high speed power and area efficient multipliers [1][2][3]. In the partial product addition stage, compressors contribute to the reduction of the partial products by reducing the number of adders at the final stage and also contribute to the reduction of critical path which is important to maintain the circuit's performance.

Conventional CMOS design technique is best in terms of output logic level. Both logic-1 and logic-0 are transferred correctly at the output but at the expense of large area and high power consumption.

In CMOS circuits, power dissipation primarily occurs during device switching. Whenever input signal rises or falls, a very large current starts flowing suddenly between VDD and GND. This large current leads to very high power consumption. In order to reduce to power dissipation and area, Gate diffusion input technique is used in compressor designs presented in this paper. Top level designs of compressors are presented in [1]

Section II deals with the compressor basics. Section III deals with the Gate diffusion input technique in detail. Section IV describes the compressor designs implemented using GDI technique. Section V deals with the performance evaluation and results. Section VI presents the conclusion and future work.

II. COMPRESSOR BASICS

Compressor adders are formed by combining the property of a binary counter with that of a compressor. In a 4:3 compressor, if a, b , c, d are the inputs and out2, out1, out0 are outputs then out2,out1 and out0 provides the count of the number of 1's at inputs a, b, c ,d. The counter property of 4:3, 5:3, 6:3 and 7:3 compressors is illustrated in Tables I, II , III and IV.

TABLE I
COUNTER PROPERTY OF 4:3 COMPRESSOR

Inputs	Outputs			Binary Equivalent
	Out2	Out1	Out0	
All inputs are zero	0	0	0	0
Any one input is 1	0	0	1	1
Any two inputs are 1	0	1	0	2
Any three inputs are 1	0	1	1	3
All four inputs are 1	1	0	0	4

TABLE II
COUNTER PROPERTY OF 5:3 COMPRESSOR

Inputs	Outputs			Binary Equivalent
	Out2	Out1	Out0	
All inputs are zero	0	0	0	0
Any one input is 1	0	0	1	1
Any two inputs are 1	0	1	0	2
Any three inputs are 1	0	1	1	3
Any four inputs are 1	1	0	0	4
All five inputs are 1	1	0	1	5

TABLE III
COUNTER PROPERTY OF 6:3 COMPRESSOR

Inputs	Outputs			Binary Equivalent
	Out2	Out1	Out0	
All inputs are zero	0	0	0	0
Any one input is 1	0	0	1	1
Any two inputs are 1	0	1	0	2
Any three inputs are 1	0	1	1	3
Any four inputs are 1	1	0	0	4
Any five inputs are 1	1	0	1	5
All six inputs are 1	1	1	0	6

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TABLE IV
COUNTER PROPERTY OF 7:3 COMPRESSOR

Inputs	Outputs			Binary Equivalent
	Out2	Out1	Out0	
All inputs are zero	0	0	0	0
Any one input is 1	0	0	1	1
Any two inputs are 1	0	1	0	2
Any three inputs are 1	0	1	1	3
Any four inputs are 1	1	0	0	4
Any five inputs are 1	1	0	1	5
Any six inputs are 1	1	1	0	6
Any seven inputs are 1	1	1	1	7

III. GATE DIFFUSION INPUT TECHNIQUE

Using GDI technique, implementation of a wide range of complex logic functions is possible using only two transistors. GDI technique is based on the use of a simple cell which looks like standard CMOS inverter as shown in fig.1, but there are some important differences [4]:

(1) GDI cell consists of 3 inputs. G (common gate input of nMOS and pMOS), P (input to the source/drain of pMOS) and N (input to the source/drain of nMOS).
(2) N or P (respectively) is connected to bulks of both nMOS and pMOS, so it's biasing can be done arbitrarily at contrast with CMOS inverter.

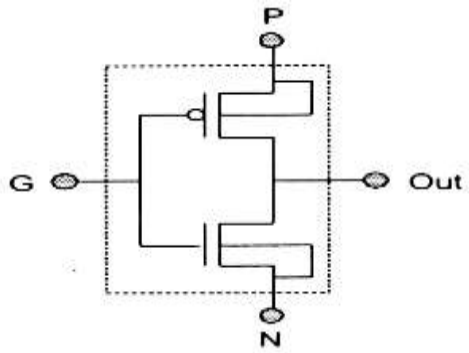

Fig. 1 Basic GDI cell

GDI technique is suitable for design of efficient low-power circuits. It uses a reduced number of transistors as compared to CMOS. At the same time, it improves logic level swing and static power characteristics and allows simple top-down design by using small cell library.

Table V shows how a simple change of the input configuration of the simple GDI cell corresponds to very different Boolean functions [4].

TABLE V
FUNCTIONS IMPLEMENTED USING GDI TECHNIQUE

N	P	G	OUT	FUNCTION
0	B	A	A'B	F1
B	1	A	A'+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A'B+AC	MUX
0	1	A	A'	NOT

These functions are very complex when implemented in CMOS logic and require 6-12 transistors. But the same functions are very easy to implement using GDI method and require only two transistors per function.

Here one important thing to be noted is that all the functions are possible in standard p-well CMOS process but can only be successfully implemented in twin-well CMOS or SOI technologies.

Both F1 and F2 form complete logic families. They allow realization of any possible two-input logic function. But F1 is the only GDI function that can be realized in a standard p-well CMOS process, because the bulk of any nMOS is constantly and equally biased. When N input is at high logic level and P input is at low logic level, the diodes between NMOS and PMOS bulks to Out are directly polarized and there is a short between N and P which results in static power dissipation and Vout~0.5 VDD. This is a drawback for OR, AND, and MUX implementations in regular CMOS with V_{BS}=0 configuration. The effect can be reduced if the design is implemented in floating-bulk SOI technologies [5], where a full GDI library can be implemented. But here, floating-bulk effects have to be considered

IV. PROPOSED DESIGN OF HIGHER ORDER COMPRESSORS

The top level designs of higher are used in [3]. Here the logic block for parallel addition is replaced by two or three bit Carry look ahead adders. Table VI shows the components used in the compressors presented in this paper. In the present work, each and every basic cell used to design compressors is implemented using GDI technique.

TABLE VI
Components used in compressors

Compressor	Components Used
4:3 compressor	2 GDI half adders, 2 bit GDI carry look ahead adder
5:3 compressor	1 GDI full adder , 1 GDI half adder, 2 bit GDI carry look ahead adder
6:3 compressor	2 GDI full adders, 2 bit GDI carry look ahead adder
7:3 compressor	1 GDI full adder, a 4:3 GDI compressor, 3 bit GDI carry look ahead adder

Figure 2,3 4 and 5 show the how these components shown in Table2 are connected to make 4:3, 5:3 , 6:3 and 7:3 compressors respectively.

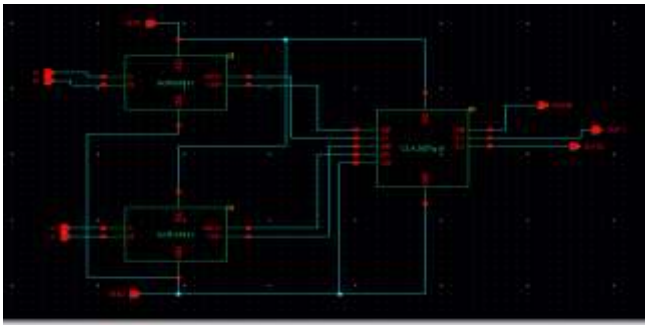

Fig. 2 Schematic of 4:3 compressor

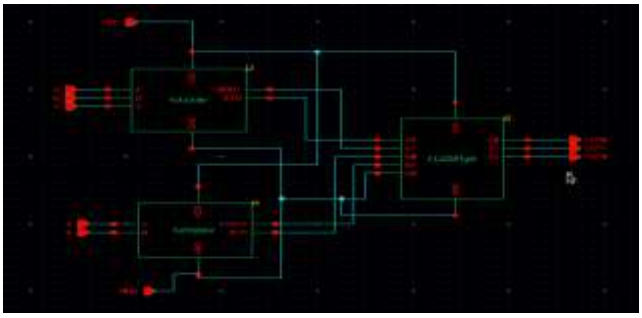

Fig. 3 Schematic of 5:3 compressor

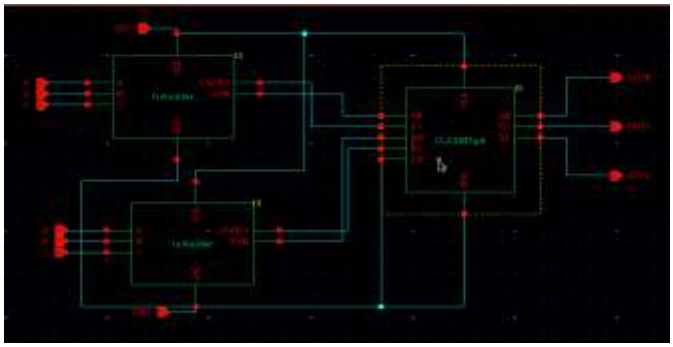

Fig. 4. Schematic of 6:3 compressor

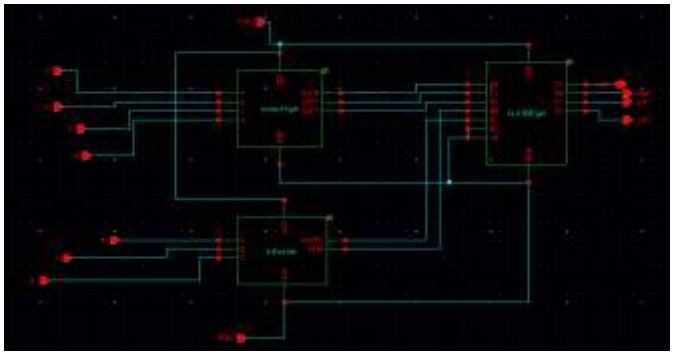

Fig. 5 Schematic of 7:3 compressor

The output waveforms of GDI based 4:3 5:3, 6:3 and 7:3 compressors are shown in figures 6,7 ,8 and 9 respectively.

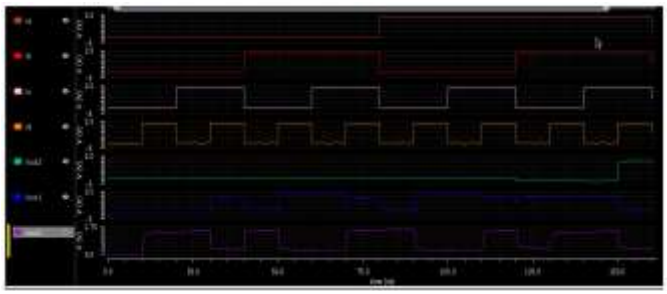

Fig. 6. Output waveform of 4:3 compressor

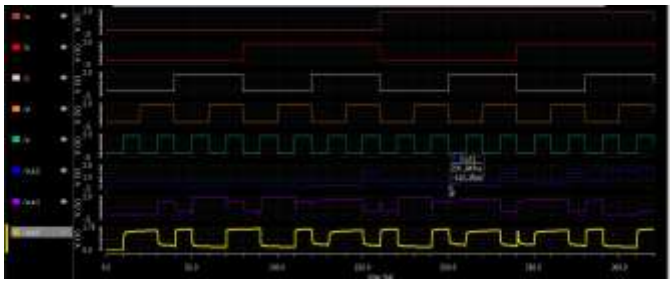

Fig. 7. Output waveform of 5:3 compressor

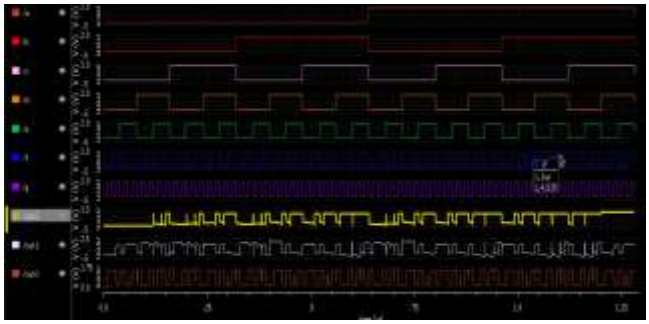

Fig. 8. Output waveform of 6:3 compressor

Fig.9 Output waveform of 7:3 compressor

V. PERFORMANCE EVALUATION AND COMPARISON

Compressor designs, presented in this paper, are implemented on Cadence Virtuoso tool at 180nm technology using both GDI technique and conventional CMOS technology. The designs are simulated on cadence spectre at 100MHz using 1.8 V supply voltage. Fig. 10 and 11 illustrate the comparative performance of the designed compressors in terms of area and
Power dissipation.

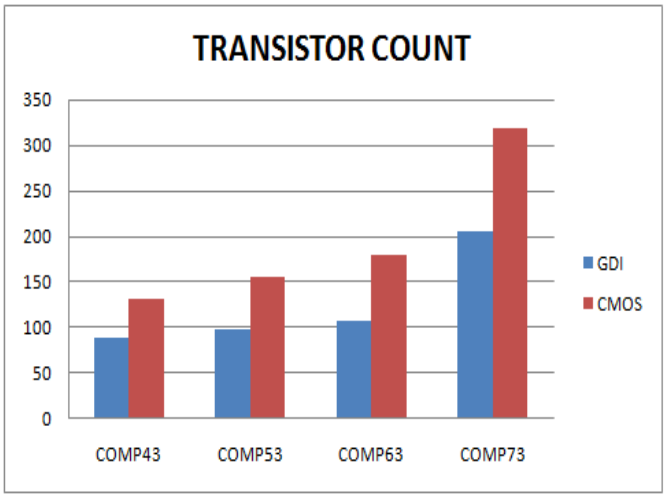

Fig. 10. Transistor count comparison

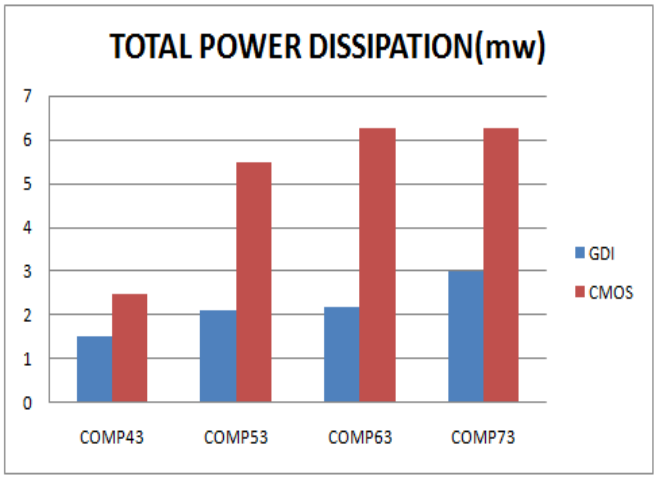

Fig. 11 Comparison of total power consumption

Comparison shows that compressors designed using GDI technique is better than those designed using CMOS technique. Results show that there is reduction in area and power ranging from 38.8% to 65.26% and 33.3% to 40% respectively with a very slight improvement in speed.

VI. CONCLUSION

A power efficient GDI technique has been used to design compressor adders. The use of GDI technique reduces the number of transistors required and the total power consumption. The transistor level implementation of compressors using GDI technique is easier as compared to that with CMOS technique. These low power, area efficient compressors can be used in multipliers during partial product addition stage. With the use of compressors, the number of stages for partial product addition can be reduced to a great extent. The compressors presented can be utilized in processors used in handheld devices.

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