A Full swing Ex-OR/Ex-NOR Gate Circuit Using Pass Transistor Logic with Five Transistors

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Abstract **-- The Ex-OR/Ex-NOR gates are the basic building blocks of various digital system applications like adder, comparator, and parity generator/checker and encryption processor. This paper proposes a 5T full swing pass transistor based Ex-OR/Ex-NOR circuit using new 3T full swing pass transistor Ex-OR gate. The new Ex-OR with three transistors is proposed by modifying the existed 3T cross coupled Ex-OR gate to get full output voltage swing. Then one bit full adder, 4-bit ripple carry adder and 8-bit ripple carry adder are constructed with use of the proposed 5T full swing Ex-OR/Ex-NOR circuit. All the proposed and existing circuits are simulated and compared with Cadence Spectre 180nm CMOS technology with the supply voltage of 0.6V to1.8V. The simulation results show that the proposed circuits achieve a full output voltage swing for all the input combinations with high speed. And the proposed full adder and ripple carry adder circuits have better Power Delay Product than the existing circuits.**

Keyword: Propagation Delay, Power Dissipation, Output voltage swing, PDP, Ex-OR/Ex-NOR, Full adder, Ripple carry adder.

I. INTRODUCTION

In the electronic world, most of the VLSI circuits have been designed by the CMOS Technology. It has become captivating because it reduces the complexity of the circuit and easy to realize the circuit that has excellent noise margins and the most important advantage is low power consumption and has the disadvantage of slow switching speed and CMOS devices can easily be destroyed by the static electricity. Due to this reason a number of researchers has proposed different logic styles like CPL (Complementary pass transistor logic), DPL (Double pass transistor logic), and PTL (Pass transistor logic) etc. CPL is used to perform the logic verification and to comprehend the static and high performance digital system designs. In CPL logic only nMOS transistors are used and the logic at the output is varied from 0 to (Vdd-Vth), i.e. the circuits are unable to get full swing at the output. In order to avoid this problem, static CMOS transistors are to be used at the following gates, which leads to the static power dissipation and degrades the performance of the device as so, some intermediate buffers have to be used to get full swing at the output as a result delay of the circuit increases gradually with the addition of number of stages in the circuit. To avoid the delay problem in CPL, a pMOS transistor has to be connected in parallel with nMOS to produce a full swing (Vdd) at the output. Hence we are using both pMOS and nMOS it is called Double pass transistor logic (DPL) and its drawbacks are large area and high power. To overcome the drawback of DPL, PTL has been developed for low power applications and the advantage is either pMOS or nMOS can be used to implement the logic design. In PTL the supply rails can be replaced by providing the inputs which results in reduction of number of transistors. In this paper all the logic circuits has been implemented by PTL. The arithmetic and logic operations like full adders, compressors, parity checkers are implemented by using Ex-OR/Ex-NOR gates. Generally the 1-bit full adders are the basic building blocks for many operations like multiplication and division. The number of arithmetic operations in multipliers are very high so the delay is more in the critical path which influence the overall performance of the system, so optimized design and analysis is required for the Ex-OR and Ex-NOR gates, will enhance the performance of 1-bit full adder which in turns increases the performance of ripple carry adders, multipliers etc in larger designs.

In this paper we proposed a new full swing pass transistor based Ex-OR/Ex-NOR gate using 5 transistors. The proposed circuit is compared and evaluated with existing circuits [1-3]. And then 1-bit full adder, 4-bit ripple carry adder and 8-bit ripple carry adder is constructed using the proposed 5T Ex-OR/Ex-NOR circuit. The

proposed circuits achieved the less power, more speed, full output voltage swing and less area.

II. CONVENTIONAL EX-OR/EX-NOR CIRCUITS

The PTL based Ex-OR/Ex-NOR gate with six number of transistors [1] has full output voltage swing for all the input combinations which was proposed by D.RadhaKrishnan et. al, in 2001. And it has better driving capability and full output voltage swing by using Vdd and Gnd voltages at the source terminals of pMOS $T_3$and nMOS T_4 transistors. This circuit schematic and its input/output wave forms are shown in Fig.1 and Fig.2 respectively. In 2003, Elgamel et.al proposed the improved version of circuit [1] but it requires two extra transistors when compared to circuit [1]. This schematic is shown Fig.3. In this circuit the two extra transistors form a forward and backward feedback between the Ex-OR and EX-NOR to get better PDP, higher noise immunity and to rectify the signal degradation problem. And this circuit gives full swing output, is shown in Fig.4. All these can be achieved with the proposed circuit with 5 transistors only.

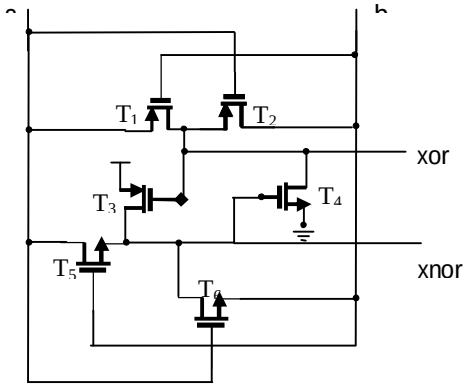

Fig.1: Conventional 6T Ex-OR/Ex-NOR Circuit

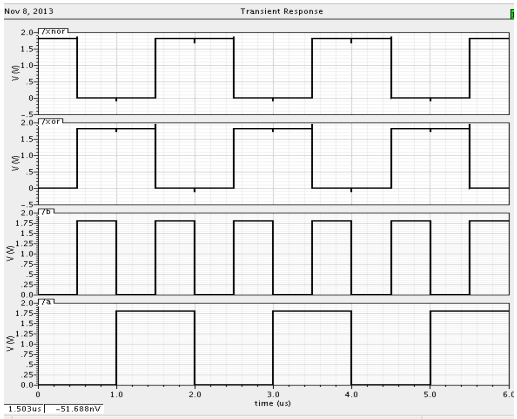

Fig.2: Input & Output waveforms of Conventional 6T Ex-OR/Ex-NOR Circuit

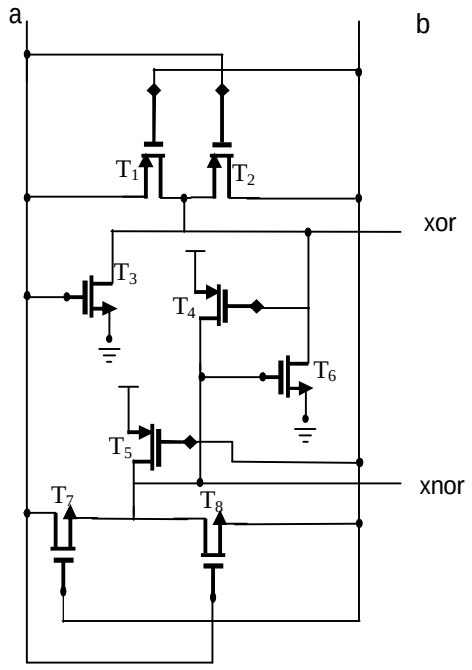

Fig.3: Conventional 8T Ex-OR/Ex-NOR Circuit

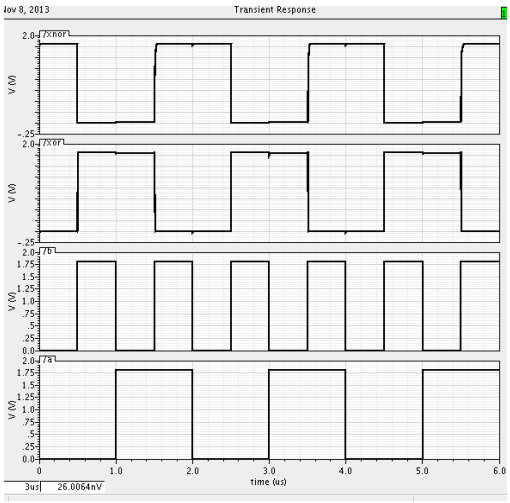

Fig.4: Input & Output waveforms of Conventional 8T Ex-OR/Ex-NOR Circuit

A minimum five transistor PTL based Ex-OR/Ex-NOR gate was proposed by Rajiv Kumar et.al in 2011, is shown in Fig.5. This has less delay and better power delay product than [1] and [2] but it suffers from signal degradation problem for Ex-OR logic. From Fig.6, it is shown that the output for Ex-OR is lacked from full voltage swing for some combination of inputs. This problem is eliminated in the proposed circuit with the same area and better PDP.

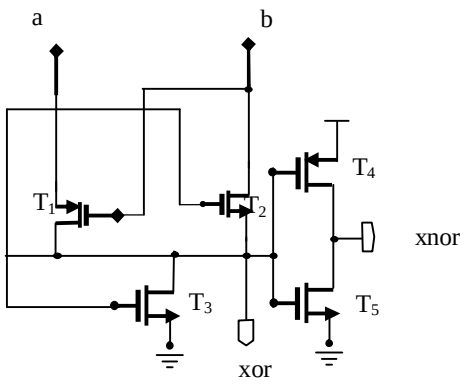

Fig.5: Conventional 5T Ex-OR/Ex-NOR Circuit

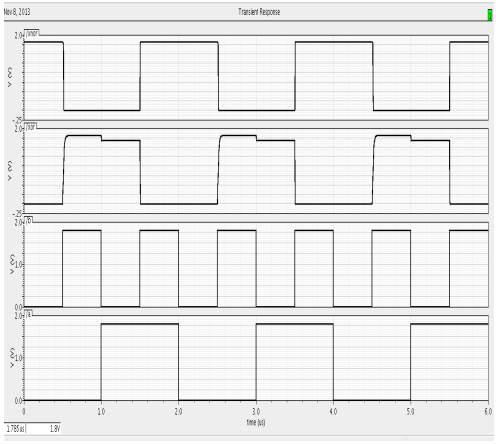

Fig.6: Input & Output waveforms of Conventional 5T Ex-OR/Ex-NOR Circuit

III. PROPOSED EX-OR/EX-NOR CIRCUIT

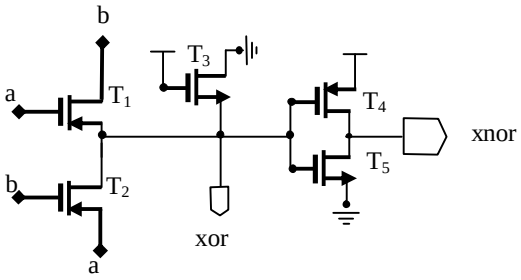

Fig.7: Proposed5T Ex-OR/Ex-NOR Circuit

In this paper we proposed low-voltage Ex-OR/Ex-NOR gate using five transistors. The schematic of proposed 5T Ex-OR/Ex-NOR circuit is shown in Fig.7. The proposed Ex-OR/Ex-NOR gate is based on the concept of pass transistor logic and Static CMOS Inverter. The Pass transistor design uses small transistor count and operates with very low-power and results high-performance. In this proposed circuit two input Ex-OR gate is designed by using three transistors T_1, T2 and T_3. When the input 'a' is logic 0 and 'b' is logic'0' all the three transistors are in ON condition then the strong logic 0 is generated at the output through T_3 nMOS transistor. For the input 'a' logic '0' and B logic '1' the transistor T_2 is in OFF condition and T_1 is in ON condition, then logic '1' is passed to the output though the PMOS pass transistor T_1. And when 'a' is logic '1' and 'b' is logic' 0'then the output is logic '1'which is passed from T_2. When both the inputs are at logic '1' the transistors T_1 and T_2 are in OFF condition, and the transistor T_3 is in ON condition so, logic '0' is passed to the output. Hence this proposed pass transistor based Ex-OR gate achieves full output voltage swing for all the input combinations with use of only three transistors. This full swing Ex-OR output is applied as an input to the static CMOS inverter which is the combination of T_4 and T_5 transistors and it generates inverted output which is acted as an Ex-NOR output. In the conventional circuit-3, output is weak logic '0' for 'a' and 'b' logic '0' combination because a pMOS device passes a weak logic '0'. This weak logic '0' problem is eliminated in the proposed circuit by passing output logic '0' through nMOS transistor T3 which passes a strong logic '0'. And in the conventional circuit-3, because of weak logic '0' at the output of Ex-OR, it may generate the weak logic '1' at the output of inverter which is acting as a Ex-NOR output. This problem is also eliminated in the proposed circuit. So the proposed circuit gives full output voltage swing when compared to the conventional circuit-3 with same number of three transistors. The proposed circuit is achieving the same full swing output as conventional circuits [1-2] with five transistors instead of eight and six transistors. And this proposed circuit gives less power consumption, high speed with small area when compared to the conventional circuits [1] and [2]. The transient response of the proposed 5T Ex-OR/Ex-NOR gate is shown in Fig.8.

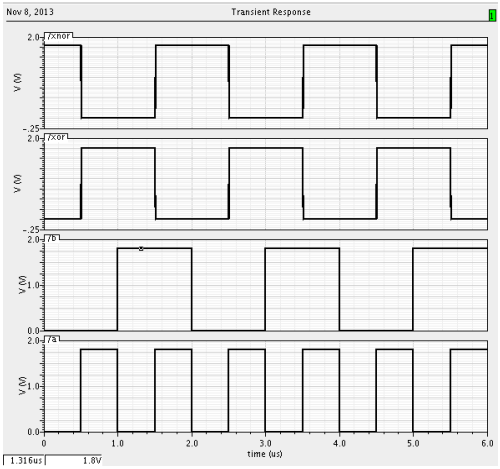

Fig.8: Input & Output waveforms of Proposed 5T Ex-OR/Ex-NOR Circuit

IV. SIMULATION RESULTS

All the proposed and existing Ex-OR/Ex-NOR gates are simulated using Spectre Cadence in the voltage range of 0.6V to 1.8V using 180nm CMOS technology. Simulation is performed at varying supply voltages to show the effect of different voltages to the output swing of Ex-OR/Ex-NOR circuits. Here the transient results are shown with the voltage of 1.8V. The transient analyses of the circuits were performed with a load capacitance of 10fF to 50fF. Fig. 8 shows the simulated results of Proposed new Ex-OR/Ex-NOR circuit of Fig.7. In Fig. 8, the results show that there is good output for all the input combinations of A and B for both Ex-OR/Ex-NOR logics.

The quantitative analysis of number of transistors, delay, power dissipation and PDP are shown in Table I and Table II. This table shows that the delay of the proposed 5T Ex-OR/Ex-NOR gate is lesser than the circuit [1][2][3] and power is lesser than the [1] ,[2] and it is approximately same as the [3]. And this table shows that PDP is better for proposed Ex-OR/Ex-NOR circuit when compared to circuit [1],[2] and [3]. The delay Vs Voltage characteristics of the conventional circuits [1-3] and proposed Ex-OR circuits are shown in Fig.9. The delay Vs Voltage characteristics of the conventional circuits [1-3] and proposed Ex-NOR circuits are shown in Fig.10. These figures show that the delay is less for the proposed circuit. The Power Vs Voltage characteristics of the all [1-3] and proposed circuits are shown in Fig.11. This figure shows that the power of [1-2] is more than proposed circuit. And power for the circuit [3] and proposed is approximately same. The PDP Vs Voltage characteristic of the all Ex-OR[1-3] and proposed Ex-OR circuits are shown in Fig.12 and Fig.13 shows the PDP Vs Voltage characteristic of the all Ex-NOR[1-3] and proposed circuits. And these two figures show that the proposed five transistor PTL based EX-OR/Ex-NOR circuit is better in PDP than the conventional [1-3] circuits. This is achieved because of the implementation with the new Ex-OR gate.

TABLE I
Quantitative Analysis of, Delay, Power Dissipation and PDP for Ex-NOR Gate

Voltage/ Design	Parameter	1.8 V	1.2V	0.8V	0.6V
Conventional -8T		437	722	1021	1174
Conventional -6T	Delay	354	631	943	1098
Conventional -5T		313	586	881	1023
Proposed -5T		171	384	754	936
Conventional -8T		12.427	5.74	2.717	1.6212
Conventional -6T		12.13	5.69	2.67	1.6
Conventional -5T	Power Dissipation	10.952	4.9	2.28	1.3302
Proposed -5T		10.9	5.18	2.576	1.665
Conventional -8T		0.00543	0.00414	0.00277	0.0019
Conventional -6T		0.00429	0.00350	0.00251	0.00175
Conventional -5T	Power Delay product (fJ)	0.00342	0.00287	0.00201	0.00163
Proposed -5T		0.00186	0.00198	0.00194	0.00155

TABLE II
Quantitative Analysis of, Delay, Power Dissipation and PDP for Ex-OR Gate

Voltage/Design	Parameter	1.8V	1.2V	0.8V	0.6V
Conventional -8T		390	599	900	1104
Conventional -6T		268	548	874	1021
Conventional -5T	Delay	250	498	850	999
Proposed -5T		99	250	499	799
Conventi		12.427	5.74	2.717	1.6212

onal -8T					
Conventional -6T	**Power Dissipation**	12.13	5.69	2.67	1.6
Conventional -5T		10.952	4.9	2.28	1.3302
Proposed -5T		10.9	5.18	2.576	1.665
Conventional -8T		0.00484	0.00343	0.00244	0.00178
Conventional -6T	**Power Delay product (J)**	0.00325	0.00310	0.00233	0.00163
Conventional -5T		0.00275	0.00240	0.00194	0.00132
Proposed -5T		0.00108	0.00130	0.00129	0.00128

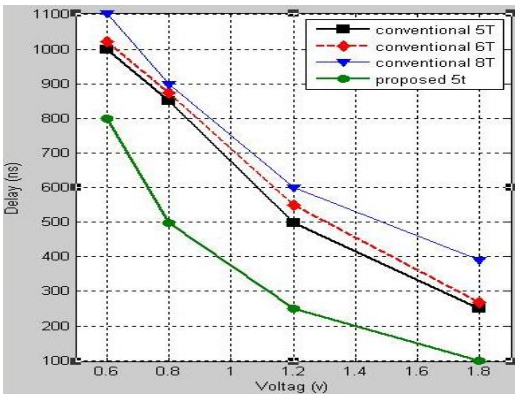

Fig.9: Delay Vs Voltage of Ex-OR Circuit

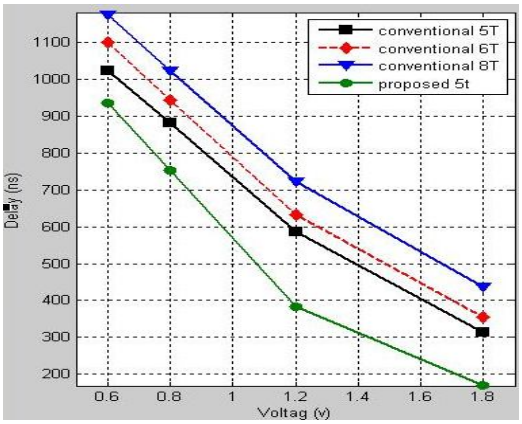

Fig.10: Delay Vs Voltage of Ex-NOR Circuit

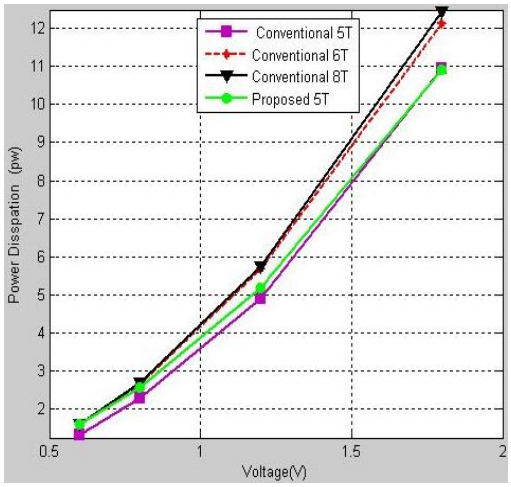

Fig.11: Power Vs Voltage of Ex-OR/Ex-NOR Circuit

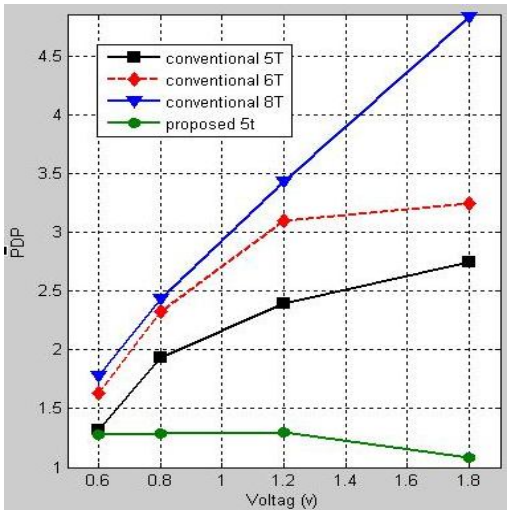

Fig.12: PDPVs Voltage of Ex-OR Circuit

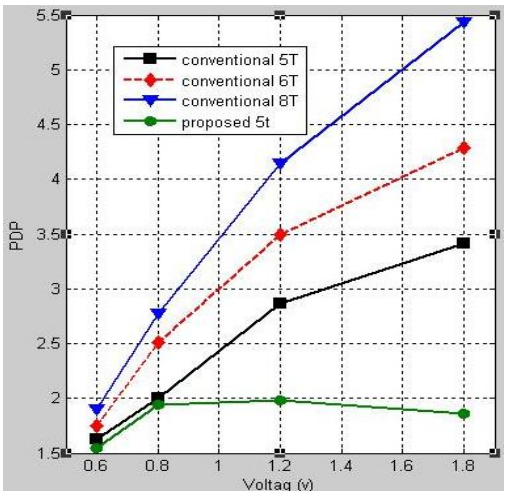

Fig.13: PDP Vs Voltage of Ex-NOR Circuit

V. IMPLEMENTATION OF 1-BIT FULL ADDER, 4-BIT RIPPLE CARRY ADDER AND 8-BIT RIPPLE CARRY ADDER

A 1-bit full adder is constructed with the proposed new 5T Ex-OR/Ex-NOR circuit and four transmission gates. That circuit schematic is shown in Fig. 14. The constructed full adder logic is represented in the following equations.

$$\text{Sum} = (A \oplus B).\overline{C} + (\overline{A \oplus B}).C$$

$$\text{Carry} = C(A \oplus B) + B.\overline{(A \oplus B)}$$

The transient response of this 1-bit full adder is shown in Fig.15. A 4-bit and 8-bit ripple carry adder is constructed with this 1-bit full adder circuit shown in Fig.16 and Fig.18 respectively. And the transient response of Fig.16 is shown in Fig.17. The quantitative analysis of 1-bit full adder and 8 bit ripple carry adder shown in the table III and table IV.

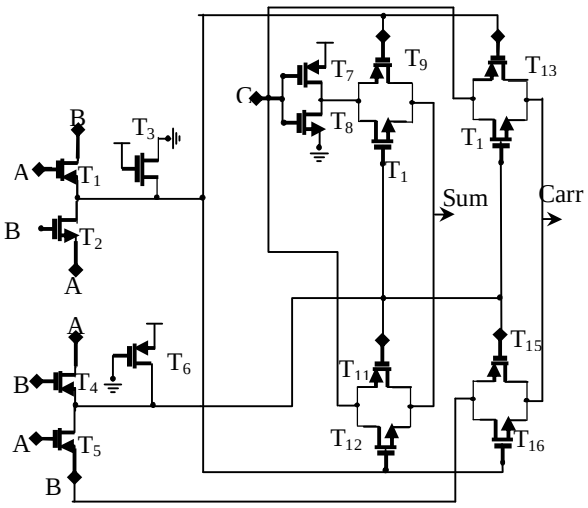

Fig.14: 1- bit full adder circuit

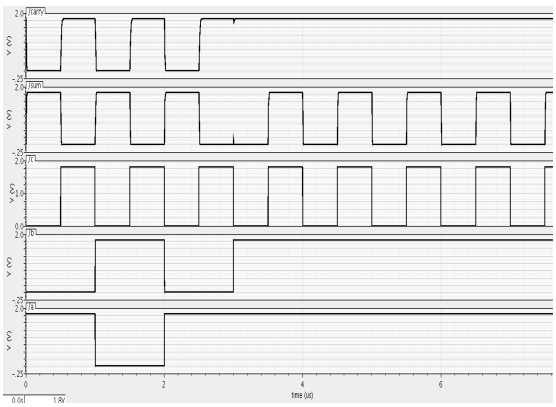

Fig.15:Input & Output wave forms of 1-bit full adder

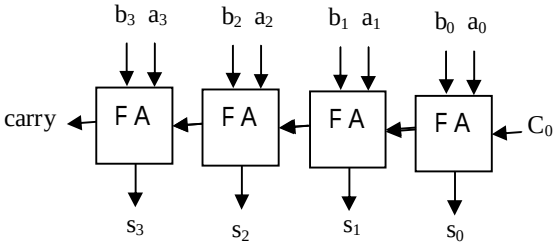

Fig.16: 4-bit ripple carry adder

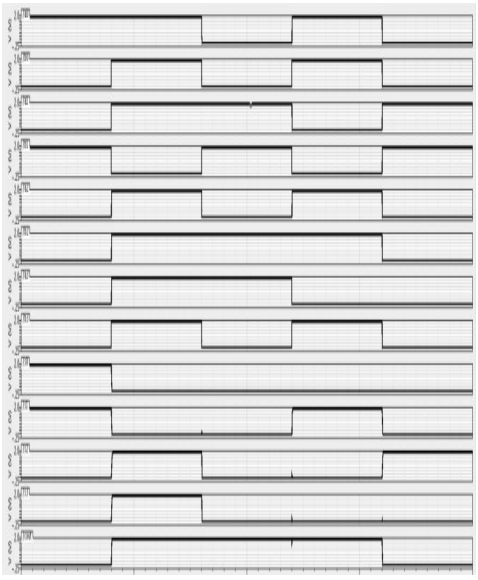

Fig.17: Input & Output waveforms of 4-bit ripple carry adder

Table II
Comparison of transistors count for 1-bit Full Adders

Serial Number	Circuit	No. of Transistors
1.	Constructed 1-bit Adder	14
2.	CMOS 1- bit Full Adder[5]	28
3.	CPL 1-bit Full Adder[6]	32
4.	BBL-PT 1-bit Full Adder[7]	23
5.	Current Sink Inverter 1-bit Full Adder[4]	23
6.	Current Source Inverter 1-bit Full Adder[4]	23

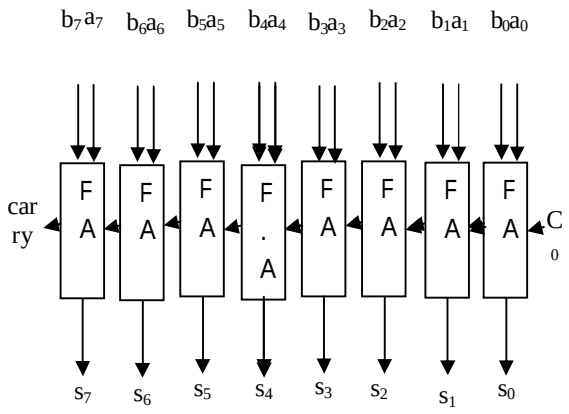

Fig.18: 8-bit ripple carry adder

CONCLUSIONS

This paper presents a five transistor Pass transistor logic based Ex-OR/Ex-NOR circuit with a full-swing voltage output in 180nm CMOS process for low voltage application. The proposed circuit has a good driving capability with good output signal in all input combinations for both Ex-OR and Ex-NOR logics and better performance and better PDP especially in low supply voltage. So these are the better choice for low-voltage application with requirement of small area and better PDP

Table III
Comparison of transistors count for 8-bit Ripple Carry Adders

S.No	Circuit	No. of Transistors
1.	Constructed 8-bit ripple carry Adder	112
2.	8-bit RC Adder using CMOS 1-bit Full Adder[5]	224
3.	8-bit RC Adder using CPL 1-bit Full Adder[6]	256
4.	8-bit RC Adder using BBL-PT 1-bit Full Adder[7]	184
5.	8-bit RC Adder using Current Sink Inverter 1-bit Full Adder[4]	184
6.	8-bit RC Adder using Current Source Inverter 1-bit Full Adder[4]	184

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