

Comparative Analysis of 1-Bit Adiabatic Full Subtractor Designed in 45nm Technology

Nikhil Deo¹, Rusni Kima Mangang²

Department of Electronics and Communication Engineering
North Eastern Regional Institute of Science and Technology

Abstract— This paper presents a comparative analysis of a 1-bit adiabatic full subtractor designed in 45nm technology node. Adiabatic logic is a low power digital circuit design technique which is much more power efficient than CMOS logic. We designed 1-bit full subtractor using 2N2N2P and DCPAL adiabatic logic styles which are two of the popular adiabatic logic styles. We found that the full subtractor designed using DCPAL saves much more power than 2N2N2P adiabatic logic style, also we simulated our circuits at two different frequencies of 100MHz and 300MHz.

Keywords— Adiabatic logic, 2N2N2P, DCPAL, low power

I. INTRODUCTION

Over the last decade power conservation has been a big issue for the researchers in almost every field of science and technology. Different approaches and solutions have been proposed which would result in low power dissipation. In the field of VLSI, due to rise in demand for portable consumer devices, ubiquitous computing devices and bio-medical devices, the need for computation to be more power efficient in a wide range of technologies is increasing, also due the shrinking of the feature size the traditional power reduction techniques are not effective as new problems like leakage current are also proving to be a major source of power dissipation hence designers have to develop new circuit topologies and design styles for low power integrated circuits.

Depending on the application, there are various methods at different abstraction levels that can be used to reduce the power dissipation in VLSI circuits, these can range from basic techniques based on fundamental physics, such as reducing power supply voltage, reducing the switching capacitance or using high threshold voltage (V_{th}) transistors (to reduce leakage); to advance techniques such as Power-gating or power down modes. For digital IC design many low power design techniques have been proposed from time to time one of them which is suitable for ultralow power applications and is thus gaining attention is Adiabatic logic. A number of different adiabatic logic styles have been proposed in past, some of the popular logic styles are ECRL [1], 2N2N2P [2], PFAL [3], DCPAL[4] etc. Adiabatic logic can be 50-80% more power efficient than compared to CMOS logic. Adiabatic logic is primarily effective in minimizing the switching power dissipation, some of the logic styles can even asymptotically achieve zero switching power dissipation. Earlier only switching power dissipation was the primary concern in low power design but with aggressive scaling of technology nodes and supply voltage another component

known as leakage power dissipation has come into picture. It can account for almost 30-40% of total power dissipation in circuits designed nanometer technology. There are various components of leakage current, but in nanometer technology the major components are subthreshold leakage, reverse-bias PN-junction leakage and gate oxide leakage.

II. SOURCES OF POWER DISSIPATION

With the increase of transistor count and clock frequency power dissipation has become a major concern in CMOS design. For reliability and proper circuit operation of portable device, peak power consumption is certainly an area of concern. But time averaged power consumption is more critical parameter as it is directly related to weight and volume of the battery required for circuit operation for a given amount of time [5].

In CMOS digital circuits, there are three main components of average power dissipation;

- a) Switching power dissipation
- b) Short-circuit power dissipation
- c) Leakage power dissipation

and can be expressed as:

$$P_{avg} = P_{switching} + P_{short-circuit} + P_{leakage} \quad (1)$$

A) SWITCHING POWER DISSIPATION

Switching power dissipation arises in digital CMOS circuits during the charging of the output node capacitance through the power supply or discharging of the node capacitance to ground. A CMOS logic gate during the switching process can be represented by its PMOS network, NMOS network, and the total load capacitance at its output node.

B) SHORT-CIRCUIT POWER DISSIPATION

Short-circuit power dissipation occurs when a logic gate (e.g inverter) is driven by an input voltage with finite rise and fall times and hence both the PMOS and NMOS transistors in the circuit conducts simultaneously for a short duration during switching, forming a direct conducting path between power supply and ground.

C) LEAKAGE POWER DISSIPATION

Leakage power dissipation occurs due to nonzero subthreshold and reverse leakage currents that flows through NMOS and PMOS transistors even when they are not switching. As the transistor size is shrinking and operating

voltage is decreasing the magnitude leakage current is increasing.

III. ADIABATIC LOGIC

Adiabatic logic is a low power digital circuit design technique. The term “adiabatic” is a Greek term that has historically been associated with the thermodynamics, A thermodynamic process in which there is no transfer of heat in or out of a system is said to be Adiabatic process. In context of Electronics system “process” refers to the transfer of charge between various nodes in a circuit. A fully adiabatic system can asymptotically reach zero dissipation if the process is carried out slowly. The term “Adiabatic” in the field of digital circuit design appears to be used in a paper presented at the workshop on Physics and Computation in the year 1993 [6].

In static CMOS logic during the switching process the output node capacitances are charged and discharged from 0V to V_{DD} by a step voltage of very short rise and fall time. During the switching process energy dissipated in switching transistor is given by $\frac{1}{2}C_L V_{DD}^2$, where C_L is load capacitance and V_{DD} is constant voltage supply Fig. 1.

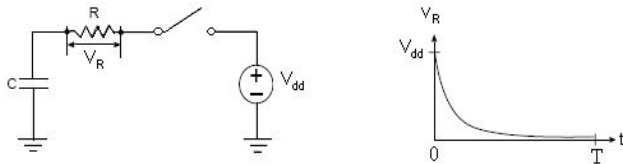


Fig. 1 CMOS logic switching process

We can say $\frac{1}{2}C_L V_{DD}^2$ is the lower limit for switching power dissipation in CMOS logic, but adiabatic logic can lower this limit further. Adiabatic logic uses an oscillating voltage supply which is generally called power clock (PCLK) as shown in Fig. 2, now instead of a step voltage the capacitances are charge and discharged by a voltage ramp so that voltage drop across the switching transistors is minimum which results in flow of lower average current through the resistive transistors which results in lower switching power dissipation.

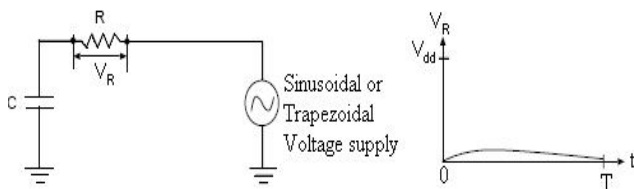


Fig. 2 Adiabatic switching principle

The oscillating voltage supply can be sinusoidal, trapezoidal or triangular in nature. Also there are many different adiabatic logic styles such as ECRL, PFAL, 2N-2N2P, DCPAL, CAL of which first five use trapezoidal supply whereas CAL use sinusoidal power clock.

IV. ADIABATIC 1-BIT FULL SUBTRACTOR

Logic Equation for 1bit Full subtractor can be described as shown below. For the three inputs X, Y and B (borrow), we

get two output first is Difference (Dout) and second is borrow (Bout).

$$D = X \oplus Y \oplus B \quad (2)$$

$$Bout = Xbar.B + Xbar.Y + Y.B \quad (3)$$

A. 1-bit full subtractor in 2N2N2P logic style

2N2N2P is a variant of 2N2P (also known as ECRL) logic family and belongs to the quasi-adiabatic logic family. The general structure of 2N2N2P is shown in Fig. 3.

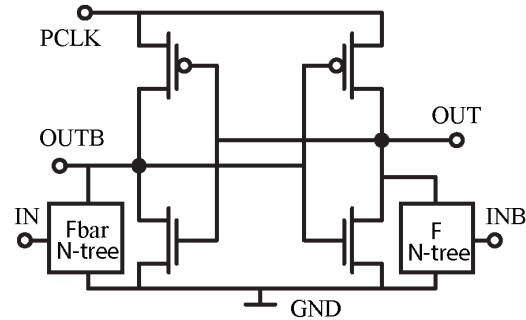


Fig. 3 General structure of 2N2N2P Adiabatic logic

This logic style like other adiabatic logic styles uses differential logic, so the logic circuit computes both the actual logic function and its complement, so it requires complimentary inputs and generates complementary outputs. The cross-coupled PMOS transistors are powered with the trapezoidal power clock supply (PCLK).

This adiabatic logic family which is derived from ECRL reduces the coupling effect. The primary advantage of 2N-2N2P [2] over ECRL is that the cross-coupled NMOS transistors result in non-floating outputs for large part of the recovery phase. Fig. 4 shows the power clock timing for a 2N2N2P inverter.

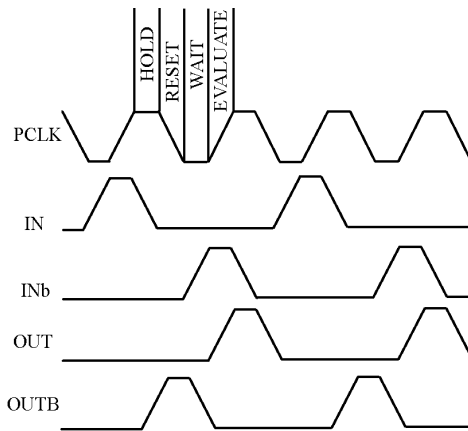


Fig. 4 PCLK, input and output timing of 2N2N2P inverter.

The Difference and borrow circuits of a 1-bit full subtractor designed in 2N2N2P are shown in Fig. 5 and Fig. 6, this structures of full subtractor is based on the structure of the full adder designed in [7].

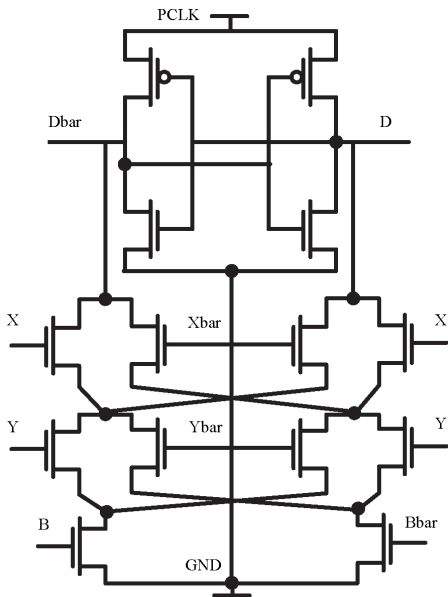


Fig. 5 Difference output (Dout) circuit for 2N2N2P logic

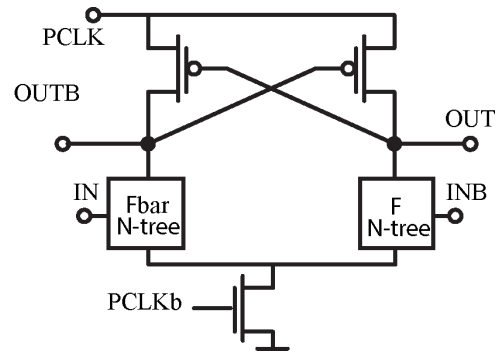


Fig. 7 General structure of DCPAL logic

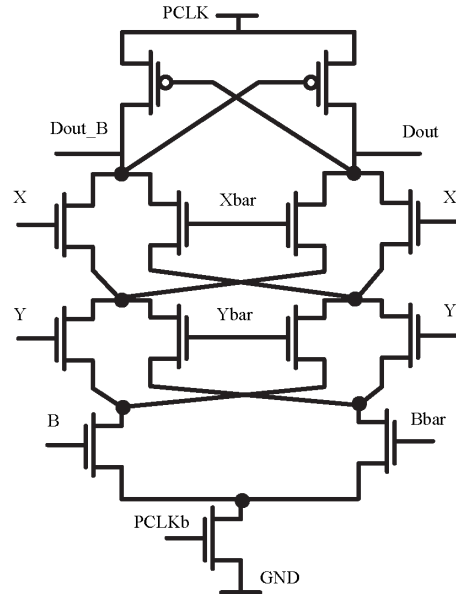


Fig. 8 Difference output (Dout) circuit of DCPAL logic

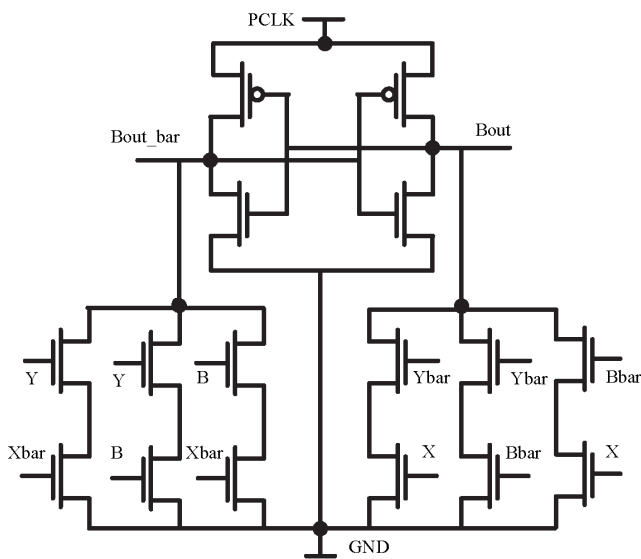


Fig. 6 Borrow output (Bout) circuit of 2N2N2P logic

B. 1-bit full subtractor in DCPAL logic style

DCPAL adiabatic logic also has cross coupled PMOS transistors and NMOS logic functional blocks in the pull-down network as shown in Fig. 7. A footer NMOS transistor is connected between the common source terminal of logic tree and the ground terminal this feature enables the pre-resolving of the inputs [4]. The power-clock PCLK and the pre-resolving clock (PCLKb) source are complement of each other. Here also Fig. 8 and Fig. 9 shows the Difference and borrow circuits for 1- bit full subtractor designed in DCPAL.

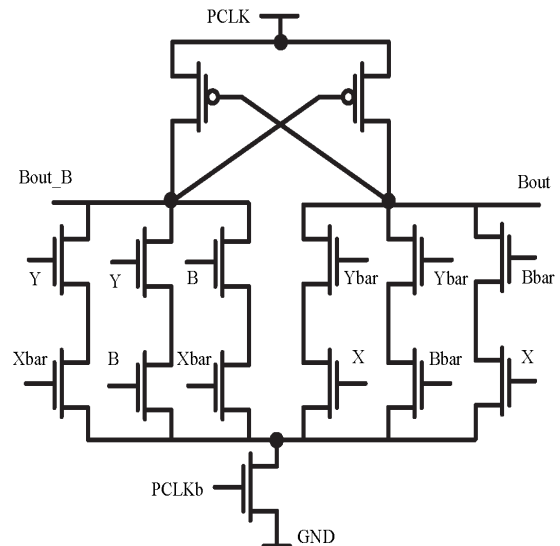


Fig. 9 Borrow output (Bout) of DCPAL logic

V. SIMULATION RESULTS

All the circuits were designed in 45nm technology, all the signals applied were of amplitude of 1V. The transistor size of NMOS is 160nm/45nm and for PMOS 180nm/45nm.

Fig. 10 shows the simulated signal waveform for 2N2N2P difference circuit of Fig. 5. Also Fig. 11 shows the simulated waveforms of 2N2N2P borrow circuit of Fig. 6.

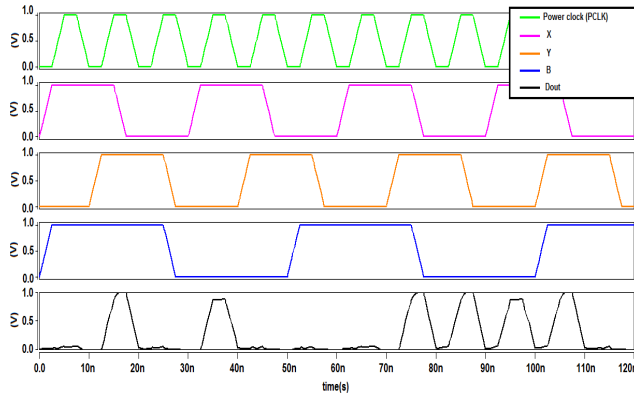


Fig. 10 Simulated output of 2N2N2P difference circuit.

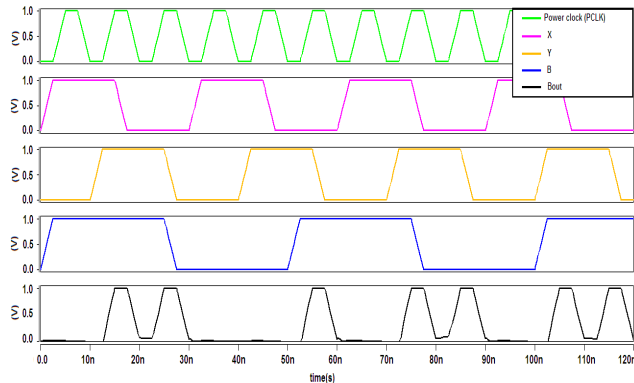


Fig. 11 Simulated output of 2N2N2P borrow circuit.

TABLE I
AVERAGE POWER DISSIPATION

	100MHz	200MHz
2N2N2P (Difference)	5.3155E-06	6.13E-06
DCPAL (Difference)	5.5348E-07	6.31E-07
2N2N2P (Borrow)	4.5168E-07	5.01E-07
DCPAL (Borrow)	4.2045E-07	4.88E-07

Table 1 shows the average power dissipation for 10 cycles under two different power clock frequency of 100MHz and 200MHz also it is shown in Fig. 12.

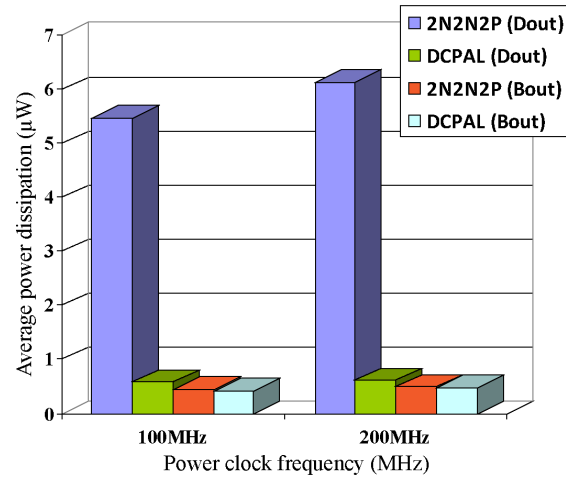


Fig. 12 Average power dissipation (µW) in 2N2N2P and DCPAL circuits

VI. CONCLUSION

We designed and simulated 1-bit full subtractor using 2N2N2P and DCPAL logic styles in 45nm technology, we obtained the average power dissipation for these circuits and found that a 1-bit full subtractor designed using DCPAL saves more power than the one designed using 2N2N2P.

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