Area Efficient Carry Select Adder (AE-CSLA) using Cadence Tools

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Abstract – **To perform fast addition operation, CSLA is one of the fastest adders used in many data-processing processors. Analyzing the structure of Regular CSLA (R-CSLA) and Modified CSLA (M-CSLA), there is a scope to reduce the area further. This work uses a simple gate level modification and a modified XOR gate is proposed to be used in the circuit. Based on this modification, 16-bit Area Efficient CSLA (AE-CSLA) is designed which provides 32% reduction in area when compared with R-CSLA and 12.5% reduction in area when compared with M-CSLA. This work is implemented in CADENCE VIRTUOSO using 180nm CMOS process technology.**

Keywords – **Binary to Excess-1 converter (BEC), Carry Select Adder(CSLA), Multiplexer(MUX), Ripple Carry Adder(RCA), Exclusive OR(XOR).**

I. INTRODUCTION

Digital adders perform the operation of addition. Designing a low power and area efficient digital adder circuit is the significant area of today's VLSI research. Ripple Carry Adder (RCA) has least complicated circuit but this type of adder is not good for practical use because the speed of addition in RCA is limited by the carry signal that ripples through the adder. In RCA, the sum for each bit position requires a carry from previous stage. Carry Select Adder (CSLA) alleviates the problem of carry propagation delay and therefore performs the faster addition operation [1].

In CSLA, multiple carries are generated simultaneously at different stages and then the carry is selected to generate the correct sum output. Since CSLA uses pair of RCA's, one with carry-in of 0 and other with carry-in of 1, it reduces the carry propagation delay but causes the more area consumption and makes the CSLA less area efficient [1].

To make CSLA as an area efficient adder, a technique of an add-one circuit was introduced. Therefore in Modified CSLA, Binary to Excess-1 Converter (BEC) is used instead of RCA with Cin=1 and multiplexer is used to select the correct sum output [2] [3] [4].

The basic idea of this work is to use Modified Binary to Excess-1 Converter (BEC) instead of RCA with Cin=1 and a simple gate level modification is done for designing a modified XOR gate which reduces the area of the circuit considerably. This paper is organized as follows: In section II and III, modified XOR gate and modified BEC is explained respectively. Section IV and section V explains the regular CSLA and the proposed CSLA respectively and the area evaluation of each block is done. Implementation results are analyzed in section VI.
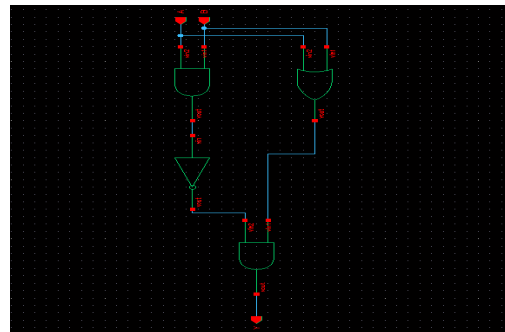

Fig 1: Modified XOR gate

II. MODIFIED XOR GATE

The main idea of this work is to do the gate level modification by modifying the basic XOR gate. As from the fig 1, there is one gate reduction in modified XOR gate. As RCA's and BEC make use of XOR gates in their circuits, so the total gate count of CSLA can be considerably reduced by using modified XOR gate.
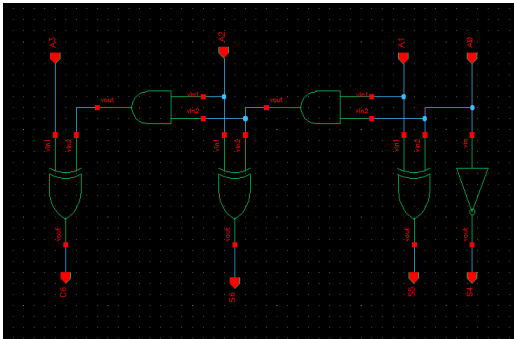
Fig 2: Modified BEC

III.   MODIFIED BEC

BEC (Binary to Excess-1 converter) is used to replace the RCA with Cin=1 so as to reduce the area consumption of CSLA. To replace n-bit RCA, an n+1 bit BEC is required. The structure of modified BEC is shown in fig 2. In BEC circuit, modified XOR gates are used to reduce the area and gate count. The MUX is to select either the RCA output or BEC output depending on the value of previous carry inputted to the select line of MUX.
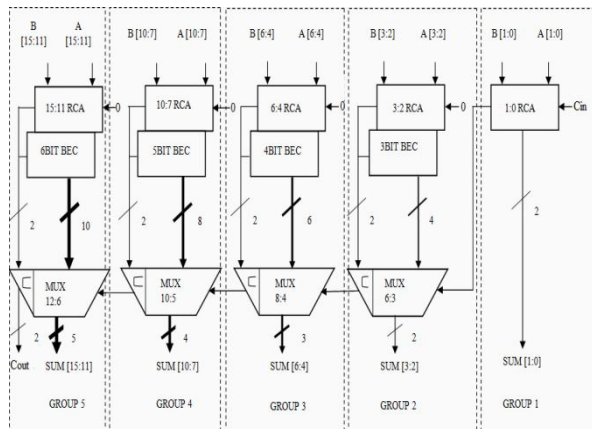

Fig 3: Modified CSLA (M-CSLA)

IV.   AREA EVALUATION OF MODIFIED CSLA

The structure of 16-bit CSLA is shown in fig 3. As from the figure, the circuit of CSLA is divided into 5 groups. Area evaluation of each group is calculated below:-

- **Group 1**- It has one 2-bit RCA which consists of 2 FA's. The area count for group-1 is as follows:-
  Full adder = 26 (2*13)

Total gate count = 26

- **Group 2**- It consists of 1 FA, 1 HA, 3-bit BEC and a 6:3 MUX. The area count for group 2 is as follows:-
  Full adder =13 (1*13)
  Half adder =6 (1*6)
  BEC =12 (XOR=10, AND=1, NOT=1)
  MUX =12 (3*4)
  Total gate count = 43

- **Group 3**- It consists of 1 HA, 2 FA's, 4-bit BEC and a 8:4 MUX. The area count for group 3 is as follows:-
  Full adder =26 (2*13)
  Half adder =6 (1*6)
  BEC =18 (XOR=15, AND=2, NOT=1)
  MUX =16 (4*4)
  Total gate count = 66

Similarly gate count for group 4 and group 5 is calculated and the total gate count shown in table 1.
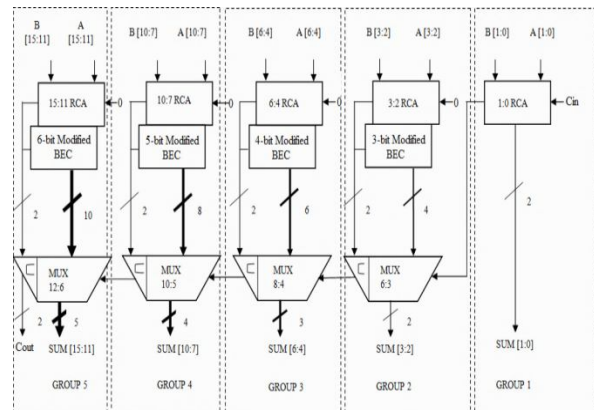

Fig 4: Area efficient CSLA
(AE-CSLA)

V.   AREA EVALUATION OF AREA EFFICIENT CSLA

In this paper, modified XOR gate with reduced gate count is used. The structure of modified 16- bit CSLA is shown in fig 4. Area evaluation of each group is calculated below:-

- **Group 1**- It has one 2-bit RCA which consists of 2 FA's. The area count for group-1 is as follows:-
  Full adder = 22 (2*11)
  Total gate count =22

- **Group 2**- It consists of 1 FA, 1 HA, 3-bit BEC and a 6:3 MUX. The area count for group 2 is as follows:-
  Full adder = 11 (1*11)
  Half adder = 5 (1*5)
  BEC = 10 (XOR=8, AND=1, NOT=1)
  MUX = 12 (3*4)
  Total gate count = 38

- **Group 3**- It consists of 1 HA, 2 FA's, 4-bit BEC and an 8:4 MUX. The area count for group 3 is as follows:-
- Full adder = 22 (2*11)
- Half adder = 5 (1*5)
- BEC = 15 (XOR=12, AND=2, NOT=1)
- MUX = 16 (4*4)
- Total gate count = 58

Similarly gate count for group 4 and group 5 is calculated and the total gate count is shown in table 1.

Groups	Regular CSLA	Modified CSLA	Area Efficient CSLA
Group 1	26	26	22
Group 2	57	43	38
Group 3	87	66	58
Group 4	117	89	78
Group 5	147	112	98
TOTAL	434	336	294

Table 1: Gate Count Comparison for various CSLA's

VI. IMPLEMENTATION RESULTS

The design proposed in this paper has been successfully tested and synthesized in CADENCE VIRTUOSO 5.0 software using library of 180nm technology. The schematic diagram of 16-bit Modified CSLA is shown in fig 5 and the corresponding Sum (S15 to S0) and Carry outputs are shown in fig 6, fig 7 & fig 8.
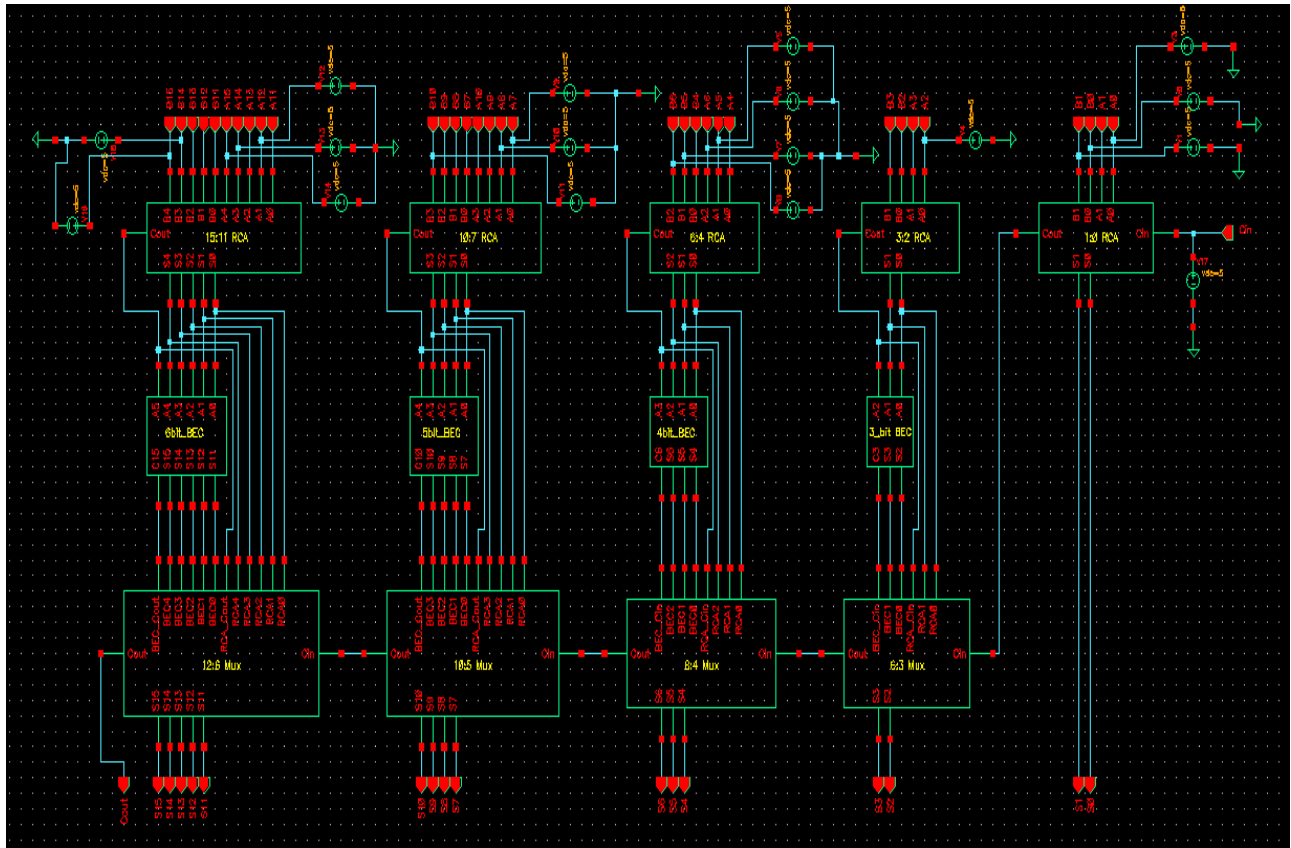

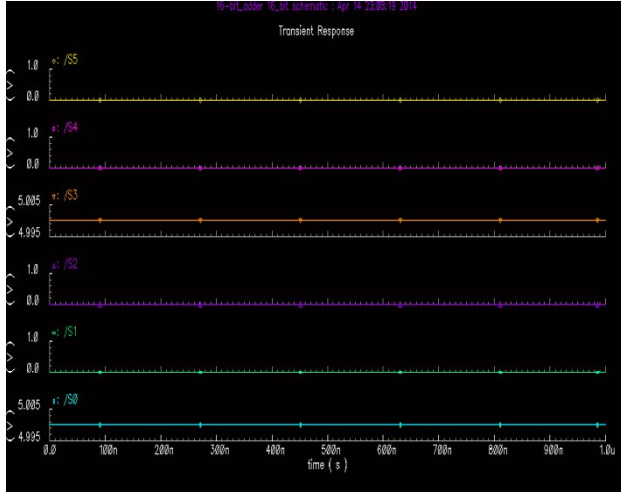Fig 5: Schematic view of 16-bit AE-CSLA
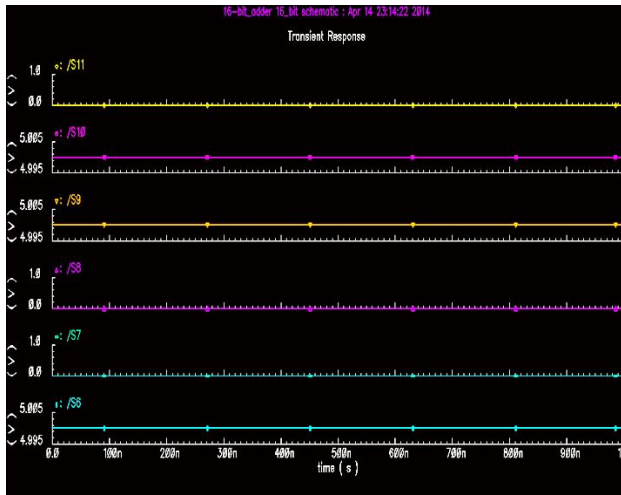
Fig 6: Simulation Waveform (S0 to S5)

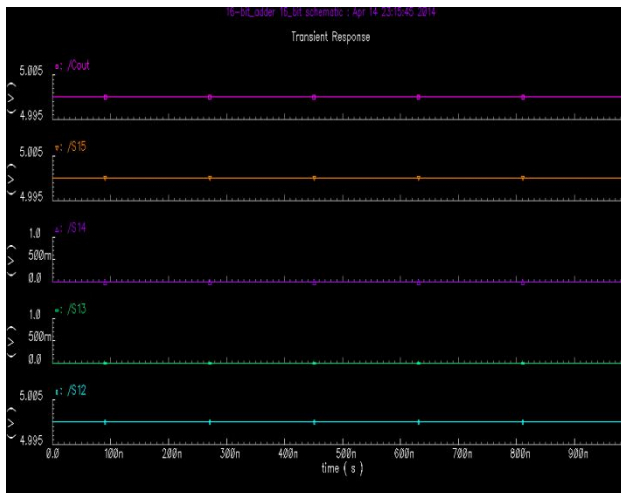Fig 7: Simulation Waveform (S6 to S11)

Fig 8: Simulation Waveform (S12 to S15 and Cout)

VII. CONCLUSION

A simple approach of modified XOR is proposed in this paper to reduce the total gate count of CSLA architecture. This reduction in total gate count is very beneficial in terms of area consumption of CSLA circuit. Therefore the area efficient CSLA (AE-CSLA) has simple and modified circuit as compared to previous CSLA's. The 16-bit addition operation of CSLA is simulated using CADENCE VIRTUOSO 5.0. The implementation of 32-bit/ 64-bit AE-CSLA would be interesting and better results can be obtained than Regular CSLA and Modified CSLA.

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