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Original Article

A Novel NCL Threshold Gate Implementation for Low Power Asynchronous Designs using FinFETs

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Abstract - Recent advancement in CMOS-based synchronous designs suffers from the unmanageable clock and power-related issues. Beyond 22nm technology, CMOS devices exhibit poor short channel control and unreliable performance. However, the FinFET device is a reliable alternative for CMOS at a deep submicron scale, offering better gate control, lower short channel effects, and excellent electrostatics. In contrast to the Synchronous design style, the Null Convention Logic-based asynchronous design paradigm offers faster operating speed, comparable power efficiency, and reduced EMI, with a modular design approach in complex systems (SoCs). This paper presents an implementation of CMOS and FinFET-based NCL threshold gates in 16nm technology. The proposed research demonstrates an average 21% power improvement and an average 33% speed improvement for FinFET-based NCL threshold gates over their CMOS counterpart. Also, the proposed NCL gate structure exhibits a 16.5% improvement in speed compared to its semi-static variant and an average 7.2% power improvement compared to its static variant.

Keywords - *FinFETs, Null Convention Logic, Multi-rail Logic, Quasi Delay-Insensitive circuits, Self-timed Design.*

1. Introduction

In the past few decades, the semiconductor industry has witnessed tremendous advancement in downscaling the on-chip device dimensions due to increasing market demands for better performance. Following Moore's prediction, device dimensions have reached tens of nanometers today. Such downscaling of transistor size is essential for better performance. However, reduction in active areas leads to multiple drawbacks like increased short channel effects, larger parasitic, Non-reliability issues, and increased variability in Process-Voltage-Temperature. Such device scaling is necessary for high-performance designs, but it will raise multiple short-channel effects. Which ultimately diminishes gate control over current conduction within the device. [13] A highly doped source or drain region can handle such short channel effects, but it will make it difficult to set up desired threshold voltage. [18]

To handle such challenges concerning device scaling, a new device architecture named FinFET has gained widespread popularity. FinFET is a multi-gate transistor architecture that supports superior scalability of planner devices. It exhibits performance improvement compared to the existing conventional planar-bulk CMOS technology. Beyond the 22 nm technology node, FinFETs can be considered the most reliable alternative to the bulk MOSFETs because of their better sub-threshold slope, less leakage power, minimal short-channel effects, and similarity to the conventional manufacturing process for CMOS technology. [6]

In addition to this, the synchronous design paradigm faces more challenges in terms of Clock management and increased power consumption for deep sub-micron technology. [18, 19] Over the past few years, asynchronous designs have shown noticeable performance as a strong alternative to the synchronous design style. This clock-less design methodology abolishes all clock-related problems like Skew, jitter, clock routing, strict timing constraints, etc. Removal of the global clock eliminates the need for complex clock routing networks and clock drivers, resulting in lower power consumption. [8]

The research demonstrates FinFET and CMOS-based Null Convention Logic gates implementations in 16nm technology. For various NCL gate designs, the proposed structure is compared with its static and semi-static variants concerning area utilization (No. of transistors), Avg. Power consumption and propagation delay. This comparative analysis will help designers decide tradeoffs between power, speed, and area to achieve performance improvement. The idea behind the proposed work is to deal with the current challenges of the semiconductor industry by incorporating the advantages of Multi-gate FinFET and NCL-based asynchronous circuits.

There are five primary sections of the paper. Section II will briefly explain about fundamentals of NCL and FinFET devices. Section III includes 16 nm implementations of CMOS and FinFET-based NCL gates for static and semi-static variants and the proposed structure. Simulation results and their analysis is carried out in section IV. The conclusion and recommendations for future work are covered in Section V.

2. Background

2.1. FinFET Devices

FinFET is a non-planar, multi-gate transistor fabricated on an SOI substrate. As shown in Fig. 1, in contrast to planar MOSFET, a "fin" shaped structure is grown over the channel region between source and drain. The lateral thickness of the fin from source to drain region defines the device channel length.

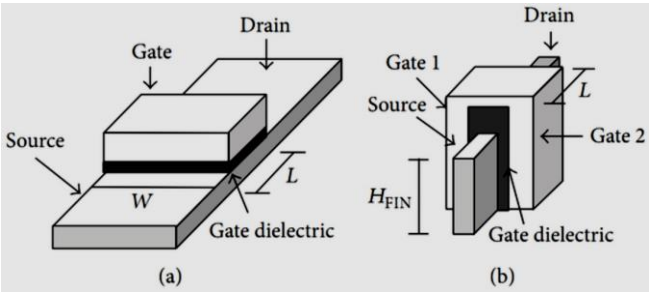


Fig. 1 Structural difference of (a) Planar MOSFET and (b) Multi-gate FinFET

For triple gate FinFET, the third gate is fabricated on top of the fin. The minimum channel width of dual-gate FinFET is derived from the height of the fin (H_{in}) and thickness of the fin (T_{fin}) as below.

$$W_{min} = 2 \times H_{fin} + T_{fin} \quad (1)$$

For larger channel width, multiple fins are grown over the channel region.

The Gate terminal is placed above the active region in planar CMOS to control current conduction between the source and drain region. On the other hand, the FinFET gate surrounds the channel region, which provides superior current control between source and drain. [2]

Dual-gate FinFETs (DG) are categorized as Shorted-Gate FinFETs and Independent-Gate FinFETs. As shown in Fig. 2(a), shorting both the front and back gate enhances the drive strength and channel control. However, that will result in more power consumption. [6]

IG FinFET is formed by growing an epitaxial oxide layer on top of the fin to isolate both vertical gates, as shown in Fig. 2(b). Such an arrangement facilitates the operation of both gates independently. This results in overall area reduction for the circuit. [3] A single IG FinFET can function like two MOSFETs in parallel. IG FinFET offers better timing performance due to a reduction in parasitic.

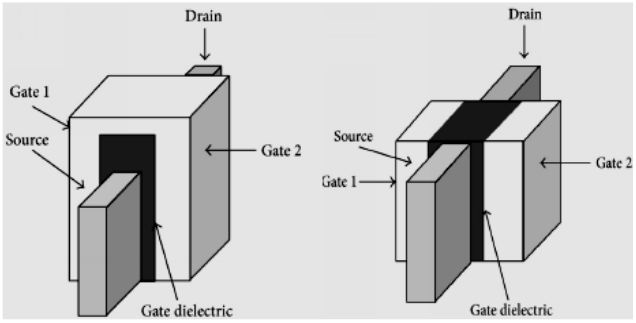


Fig. 2 FinFETs (a) Shorted Gate (SG) (b) Independent Gate (IG)

2.2. NCL Designs

NULL convention logic is largely used in clock-less design style, following the Quasi Delay-Insensitivity concept. In contrast to synchronous design, an NCL-based circuit offers much less power dissipation, improved noise immunity, minimal Electromagnetic interference, and better reusability of modules. [12] According to the International Technology Roadmap for Semiconductors-2009 report, clockless circuits will fill over half of the available chip area by 2024.

In NCL circuits, each signal transition will correspond to the occurrence of the relevant event. The switching power dissipation is greatly reduced due to this inherent delay insensitivity. As a result, for low-power VLSI, NCL designs are preferred. [11, 20, 23] Different timing issues like clock skew, hazards, and racing conditions cause various functional errors. NCL design style can deal with all such issues efficiently. The increased design complexity with clocked digital circuits is causing design challenges. NCL, on the other hand, ensures reliable circuit performance while lowering design costs and risks. [10, 21]

In NCL designs, each path follows a dual-rail convention, which means it will carry data and control information. [22] This control information will provide event synchronization in the absence of a clock. Logic implementation with NCL gates is similar to Boolean logic. Delay-insensitivity signifies that the NCL circuit will function similarly regardless of the availability of inputs. All paths in the NCL circuit follow valid transitions only due to its correct-by-constructions concept. That eliminates the necessity of detailed STA. Multi-rail logic implementations demonstrate similar delay-insensitive behavior. [7] In dual-rail logic, each signal D has dual representations with D_0 and D_1. Signal D can attain one of

the values from {NULL, DATA0, DATA1}. As per Table 1, DATA0 signal value can be indicated by (D_0= 1, D_1= 0) which is equivalent to logic '0'. Similarly, logic '1' is equal to DATA1 state (D_0= 0, D_1= 1). Void state is indicated as NULL value (D_0= D_1= 0). That means Signal D hasn't attained its final value yet. It is invalid to assert both the rails at the same time. [9]

Table 1. Dual rail logic

	DATA 0	DATA 1	NULL	Invalid
D0	1	0	0	1
D1	0	1	0	1

NCL circuits are built using Threshold gates. These threshold gates have in-built state holding capabilities. NCL gate is termed as THmn gate. Fig. 3 shows its symbol. Here, m indicates the gate threshold value while n is no inputs, with n > m > 1. Threshold value m ensures that minimum m inputs must be asserted out of n inputs to assert the gate output. Similarly, after achieving output SET, all inputs must return to NULL before output returns to NULL. Such state holding capability is achieved with the hysteresis phenomenon in NCL gates. [9]

Fig. 3 NCL Gate

All inputs are indicated on the left side curved part, as seen in the THmn threshold gate symbol. The tapering end on the right side of the gate symbol denotes an output. The numeric value within the gate symbol denotes the threshold value, m. THmn gates are non-weighted threshold gates. While weighted threshold gates can be shown as $THmnWw_1w_{2..}w_K$. Here, w_1, w_2, ..w_K indicates integer weights for each input K. [1] For each K, $1 < K < n$, $1 \leq w_K \leq m$. The weighted gate shown in Fig. 3 is TH34w2.

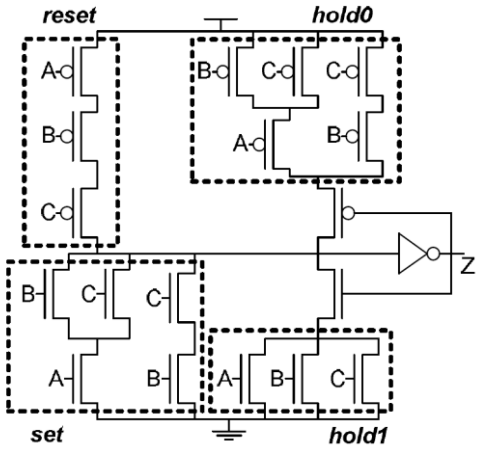
2.3. Transistor-based implementation of NCL gate

For proper functioning of NCL-based circuits, each NCL gate needs to reset all inputs before its output gets reset after each set condition. [14] There are different transistor-based NCL gate implementations, like Static and Semi-static. Hysteresis behavior in each variant is achieved with a different arrangement of transistors. The static version of Each NCL gate has its own set of equations for different output states like SET, RESET, Holding '0', and Holding '1'. As the name suggests, the SET equation specifies how gate output is asserted, while the equation for HOLD1 indicates the condition for output to stay asserted after it is sent. Performing OR operations between all inputs achieves such HOLD1. This is common for all threshold gates. Similarly, HOLD0 keeps output de-asserted until the gate receives asserted inputs equal to a threshold value. While in semi-static NCL gates, there is no HOLD0 or HOLD1 block. But the output is held stable using an inverter loop. [5, 24]

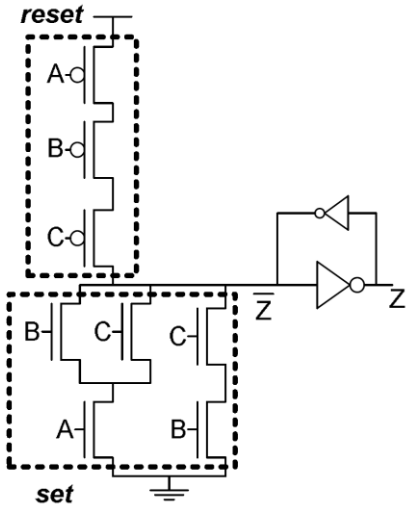
Fig. 4 shows CMOS-based Static and semi-static variants of the TH23 threshold gate. [15] This gate with a threshold value equal to 2 ensures that any of its 2 inputs must be set before output gets asserted. This condition can be achieved with equation [A•B+A•C+B•C], while the HOLD1 equation [A+B+C] ensures that output will not be de-asserted until all inputs are de-asserted. Similarly, RESET and HOLD0 blocks complement HOLD1 and SET blocks, respectively. For any given NCL gate, its Boolean formula is summarized as follows,

$$Z = SET + (Z^{-} \bullet HOLD1) \quad (2)$$

Here, Z^{-} denoted the prior output.



(a)



(b)

Fig. 4 TH23 gate (a) Static design (b) Semi-static design

Various dynamic and differential implementations for CMOS-based NCL gates are discussed in [1]. Such designs are delay-sensitive. Muller C-element is functionally equivalent to the NCL TH22 gate. [25] Different static and semi-static designs for CMOS-based Muller C-element are discussed [16, 24].

2.4. Fundamental NCL gates

For synchronous circuits, there are 7 gates available for Boolean logic implementation. Similarly, NCL designs are formulated using 27 fundamental threshold gates. Table 2 lists all such NCL gates with their Boolean functions and no. of transistors required for its static/semi-static implementation. Any login function with four variables can be synthesized with these gates. Note that each rail of the NCL signal refers to a distinct variable. If gate output depends on two input variables, its logic implementation is possible with four literals. [26]

Table 2. Details of basic NCL Gates [8]

NCL Gate	Boolean Function	Transistor Count (static)	Transistor Count (semi-static)
TH12	A + B	6	6
TH22	AB	12	8
TH13	A + B + C	8	8
TH23	AB + AC + BC	18	12
TH33	ABC	16	10
TH23w2	A + BC	14	10
TH33w2	AB + AC	14	10
TH14	A + B + C + D	10	10
TH24	AB + AC + AD + BC + BD + CD	26	16
TH34	ABC + ABD + ACD + BCD	24	16
TH44	ABCD	20	12
TH24w2	A + BC + BD + CD	20	14
TH34w2	AB + AC + AD + BCD	22	15
TH44w2	ABC + ABD + ACD	23	15
TH34w3	A + BCD	18	12
TH44w3	AB + AC + AD	16	12
TH24w22	A + B + CD	16	12
TH34w22	AB + AC + AD + BC + BD	22	14
TH44w22	AB + ACD + BCD	22	14
TH54w22	ABC + ABD	18	12
TH34w32	A + BC + BD	17	12
TH54w32	AB + ACD	20	12
TH44w322	AB + AC + AD + BC	20	14
TH54w322	AB + AC + BCD	21	14
THxor0	AB + CD	20	12
THand0	AB + BC + AD	19	13
TH24comp	AC + BC + AD + BD	18	12

3. NCL Gate implementation with FinFET

CMOS-based synchronous circuits currently drive the semiconductor industry. Both CMOS technology scaling and timed techniques, on the other hand, have nearly reached their limits. [27] CMOS-based synchronous design methodology cannot cope with the increasing demand for high operating frequency and device miniaturization. [4] As stated in section III, the unique design approach with NCL eliminates rigorous timing analysis for high-speed applications. Furthermore, despite technology scaling, FinFET technology can lower energy usage. Combining FinFET technology for NCL-based asynchronous design will resolve most of today's critical design challenges. [16,28]

CMOS and FinFET-based implementation of the proposed NCL gate structure demonstrates performance improvement compared to its static and semi-static variants. Simulation results for performance parameters such as delay time, no. of transistors, and average power consumption are listed for FinFET and its CMOS counterpart.

TH22 gate is shown in Fig. 5 to illustrate the proposed structure and its static and semi-static NCL architecture. The encircled region differentiates the SET/RESET module and its HOLD1/HOLD0 module. NCL TH22 gate depicted behavior similar to Muller C-element. State holding in a semi-static structure is achieved with back-to-back connected inverters. The forward-path inverter is strong compared to the feedback path inverter. Static TH22 gate requires 10 transistors while Semi-static TH22 gate needs 8 transistors. Its comparable SG-FinFET structure can be derived by replacing n-channel and p-channel MOSETS with N-type and P-type FinFET devices. No. of transistors in FinFET-based structure can further be reduced by using IG-FinFET.

Fig.5(c) illustrates the generic structure of the proposed implementation. The SET block provides the threshold gate functionality. This will set output Z to '1'. When all inputs are switched to null, the RESET block puts Z to '0'. The back-to-back connected inverters hold the past logic whenever the SET or RESET block is inactive. [29]

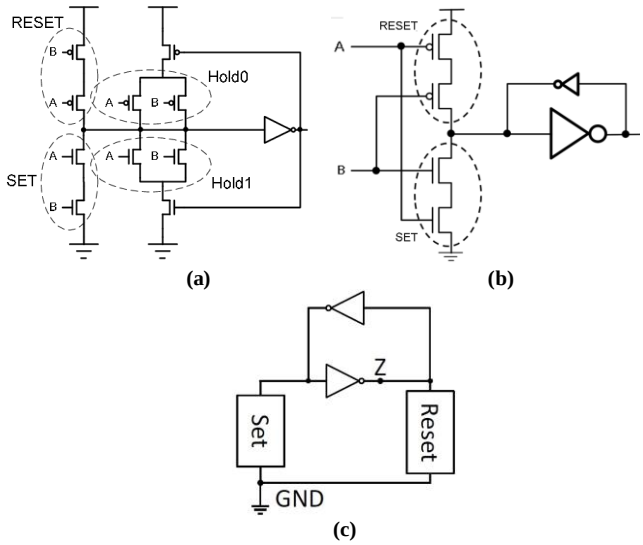


Fig 5. TH22 gate (a) Static (b) Semi-static (c) Proposed

4. Simulation Results

SPICE level simulation is carried out for static, semi-static, and proposed variants of different NCL gates with CMOS and FinFET. 16 nm Predictive Technology Models are used to perform this simulation. [17] The Width to Length ratios of all devices is set to unity for a fair comparison, except for the string inverter in the semi-static

case. Transistors within strong inverters of semi-static designs have *(W/L)* more than unity to facilitate it with state holding capabilities. On the other hand, a weak feedback inverter can also serve the purpose. An inverter can be designed by adding multiple pairs of n and p-channel MOSFETs

.

The output of each gate structure is connected to 5 femto farad load capacitance. Common technology parameters used for all designs are as follows.

V_{DD} = 0.85 Volts, Temperature = 25 ˚C,
Oxide Thickness, t_{ox} = 1.5 nm

Table 3. Performance comparison between different NCL Gate implementations with CMOS and FinFET devices

Device	NCL Gate	TpHL (pS)			TpLH (pS)			Avg. Power (uW)			Leakage Power (uW)			No. of Transistor		
		Static	Semi-static	Proposed	Static	Semi-static	Proposed	Static	Semi-static	Proposed	Static	Semi-static	Proposed	Static	Semi-static	Proposed
CMOS	TH22	91.49	278.8	241.9	135.5	104.2	141.28	0.776	1.915	0.654	0.7592	1.894	1.25	12	8	8
	TH23	97.27	228.7	221.7	130.2	66.71	97.85	0.784	1.702	0.67	0.7623	1.682	0.895	20	12	12
	TH33	98.29	39.48	41.23	138.8	48.75	79.52	0.413	1.14	0.336	0.4021	1.84	1.25	16	10	10
SG-FinFET	TH22	27.14	50.94	37.8	27.46	28.22	36.56	0.594	1.022	0.512	0.97	1.666	1.01	12	8	8
	TH23	30.69	77.41	47.54	28.86	29.91	27.89	0.638	1.181	0.63	1.042	2.034	1.54	20	12	12
	TH33	33.99	76.05	61.25	33.45	34.71	31.56	0.324	0.582	0.345	0.4947	1.005	0.57	16	10	10

Propagation delay, power dissipation, and on-chip area occupied (no. of transistors) are critical performance parameters for the comparative analysis.

Static implementation using CMOS/FinFET is considered a reference for all such comparisons. A uniform simulation setup is maintained for all structures.

Both τ_{pHL} and τ_{pLH} are calculated instead of average propagation delay. Output SET condition is achieved by setting all inputs simultaneously to '1'. Similarly, each input returns to '0' simultaneously between each set of conditions. The average value is considered for power consumption and propagation delay over all possible set conditions for each gate. For example, in the TH23 gate, all three set conditions are triggered with a particular set of inputs. Table 3 and Fig. 6 summarize simulation results and compare performance parameters.

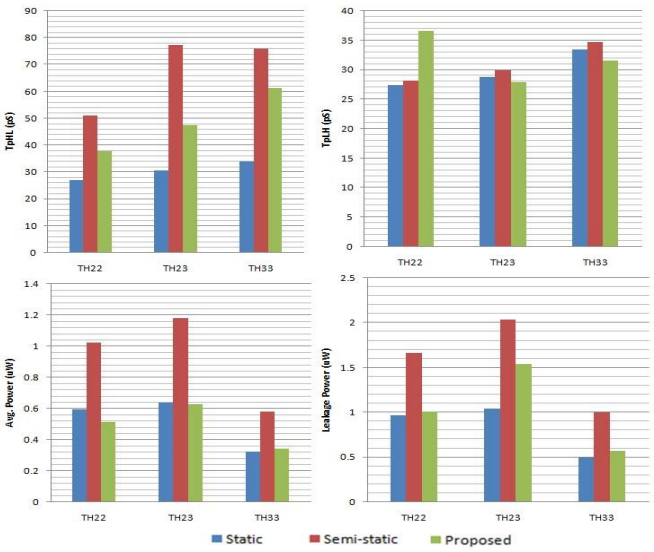
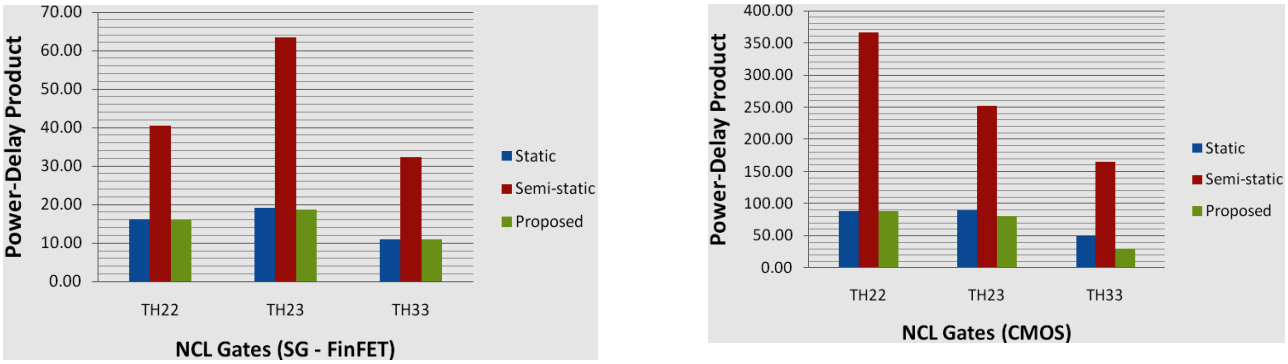


Fig 6 Parameter Comparison of FinFET based Threshold Gate implementations

The simulation results show that semi-static designs consume approximately 17% more average leakage power for CMOS/FinFET devices than static designs. This is due to the excess power required for the inverter loop. In terms of Average propagation delay per operation, Semi-static designs are 17% lower than their static counterparts. No. of transistors are less in semi-static designs due to removing HOLD0 and HOLD 1 block. Overall improvement in area utilization depends on transistor sizes in the inverter loop. The proposed NCL gate structure exhibits a 16.5% improvement in speed compared to its semi-static variant and an average 7.2% power improvement compared to its static variant. The power-delay product for respective CMOS and FinFET implementation is compared for different threshold gates as per Table 4 and Fig 7.

Table 4 PDP Comparison Between Different NCL Gate Implementations With CMOS And FinFET Devices

Device	NCL Gate	Power-Delay Product		
		Static	Semi-static	Proposed
CMOS	TH22	88.13	366.72	88.00
	TH23	89.21	251.39	80.94
	TH33	49.04	164.29	30.37
SG-FinFET	TH22	16.24	40.45	15.96
	TH23	19.02	63.37	18.74
	TH33	10.95	32.28	10.80



(a) **(b)**

Fig 7 PDP Comparison of (a) FinFET and (b) CMOS based Threshold Gate implementations

5. Conclusion

Various NCL gates are designed in 16 nm technology for the proposed structure and their static and semi-static versions using CMOS and SG-FinFETs in this work. The simulation results show that Semi-static designs consume more power and are slower in terms of speed of operation. No. of transistors are relatively less in semi-static designs. On the other hand, Semi-static designs are preferred for better noise susceptibility. The size of the gates has a big impact on the performance of semi-static designs. In this study, optimum-sized transistors were considered for all semi-static designs to ensure their correct functionality. Their sizing can be increased to get higher performance. Compared to CMOS NCL gates, FinFET-based gates consume approximately 21% less power. Also, propagation delay analysis shows that FinFETs are relatively 33% fast in terms of speed of operation. The proposed structure is more power-efficient than its semi-static version and offers less propagation delay than its static version. The designer may further achieve optimal performance with proper device sizing.

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