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Original Article

Investigation of Duty Cycle Distortion in Clock Channels with Infinisim Clockedge Technology

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Abstract *- Infinisim has developed a dynamic clock analysis tool, clock edge Simulated Program with Integrated Circuit Emphasis (SPICE) provides accurate results at very high speed and full-chip capacity. The real-time adaptive simulation technology of RASER makes the simulation fast and accurate. Clock edge overcomes the limitations of Static Timing Analysis (STA) and provides the designer with accurate timing analysis, accurate power and leakage data, and On-Chip Variation (OCV) analysis. For accurate analysis of jitters in clock edges, Infinisim clock edge uses SPICE models instead of the .libs method. Earlier days, Prime Time (PT) was used with .libs to calculate the Jitter and delay. This investigation calculates the Duty Cycle Distortion (DCD) of clock sources using Infinisim clock edge. From the final observed results, it was found that the duty cycle is not to be varied as in the case of clock edge by synopsis prime time tool, and the results were found for only 50% duty cycle; hence the analysis also did not as accurate as clock edge.*

Keywords *- Duty Cycle Distortion, Placement, and Routing (PnR), On Chip Variation, Node Based Framework (NBF), Static Timing Analysis, Prime Time, Infinisim Clock edge.*

1. Introduction

Static timing analysis is a simulation method of computing the expected timing of digital circuits without the need to simulate the full circuit. High-performance integrated circuits have been traditionally characterized by the clock frequency they operate. Delay calculations must be incorporated into the inner loop of timing optimizers at various design phases, such as logic synthesis, layout (PnR), and in-place optimizations performed late in the design cycle [1-2]. In the latest decades, the transmission data rate has been hastily improved due to the fast enhancement in all communication methods with VLSI. The main bottleneck to enhancing the rate of data transmission and its lengths is Jitter [3]. Synopsis prime time STA tool provides a signoff solution for timing, Signal Integrity (SI), power, and aware variation analysis. Primetime deals with the interpolation principle to calculate the delay models of each cell [4-6]. Interpolation uses .lib files, which contain information like each cell's input transition and output capacitance. The above parameters calculate the delay of each cell. But in the case of infinisim clock edge, it uses SPICE models, in which the delay for each cell is calculated mathematically. At 28nm technology nodes and below, STA proves overly pessimistic, and OCV leads to unacceptably large guard banding [7-9]. The rest of the article is organized as section II, discussing the infinisim NBF flow. Section III presents the infinisim clock edge analysis results, and Section IV with concluding remarks.

2. Node-Based Framework

The framework based on the node with different parameters like infinisim clock edge, node-based frame workflow, details of duty cycle distortion, and the methodology adopted is as follows.

2.1 Infinisim Clock Edge

Clock edge is a high-performance SPICE simulation tool optimized for clock network analysis [10-12]. The tool runs clock network analysis by performing tracing, netlist annotation, test bench generation, simulation, and data post-processing integrated into a fully-automated flow. The clock edge is fully integrated into the NBF flow. Reports and histograms of various parameters like Insertion Delay, Slew, Duty Cycle, and R2R check [13-15]. Clock edge provides accurate duty cycle information. Each clock from the whole circuit can be simulated separately for 45%, 50%, and 55% duty cycles. The functional failures of the clock at design speed, specific nets with duty cycle error, and specific nets failing to reach rail to rail power supply voltages can be identified [16-18].

2.2 Node Based Framework Flow

The node-based framework is a technology where the whole circuit is divided into certain corners; the simulation and analysis are done at that part on behalf of the entire circuit. Each corner will have Cx (Standard Cell) and Mx (Memory Cell) voltages, temperature, and process conditions. In NBF, all necessary inputs are given, like lib files, corner files, netlist files, and constraints files, to load the necessary runs. Once the run is started, the flow tracer generates all the reports and dumps them in the particular directory. The run can be done for one corner and multiple corners as well. Fig. 1 shows the flow tracer window for a single corner run. Once the run is completed, the reports and session logs will be generated.

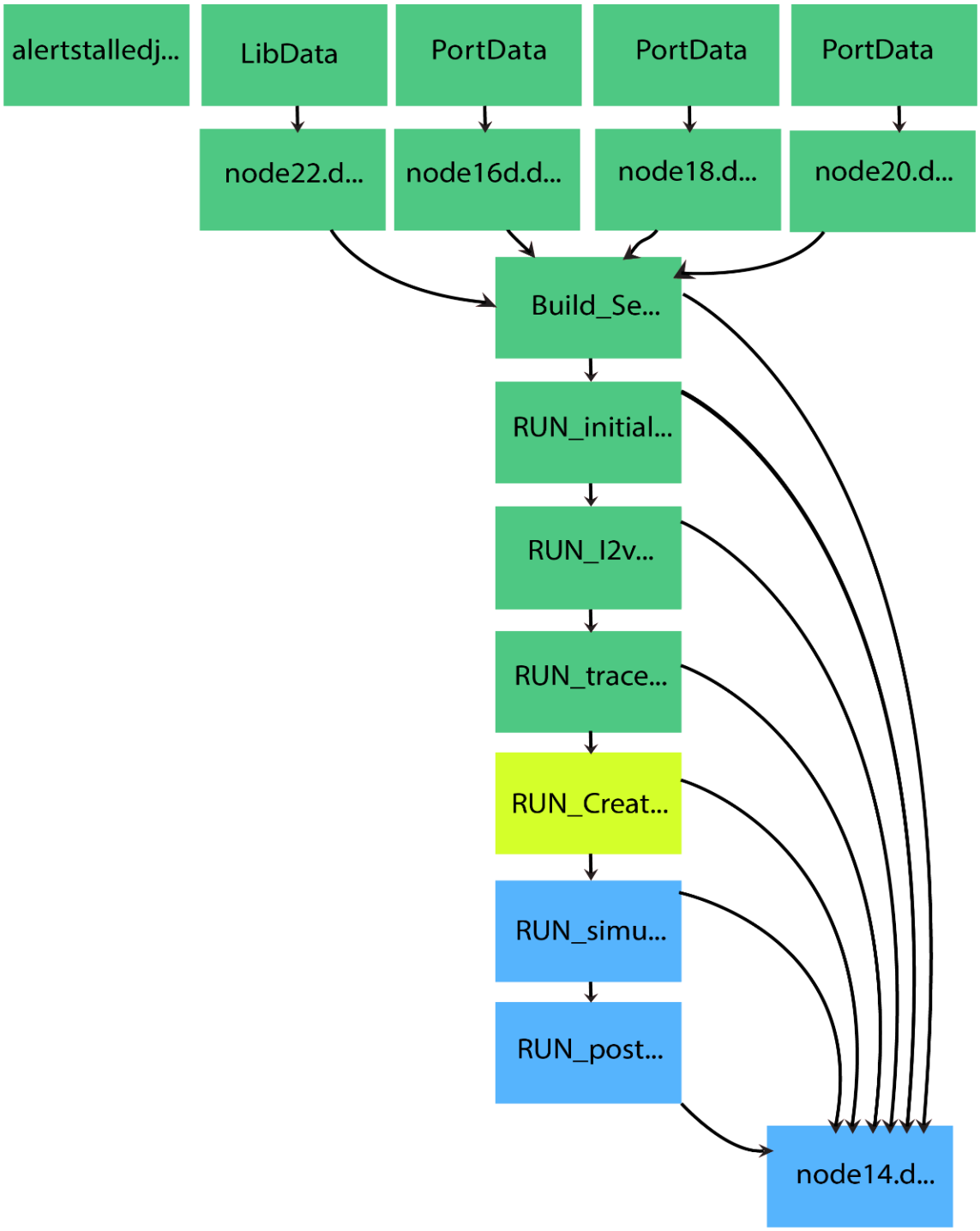

Fig. 1 Node Based Framework Flow

2.3 Duty Cycle Distortion

Duty cycle distortion is the major contributor to the deviation of the cross point of the eye diagram of a signal from its ideal position. This is only stated to the deviance of the signal relative duty cycle to its normal value. The main reasons for duty cycle distortion are signal sampling clock in DC is dissimilar, the signal decision verge level differs from its ideal voltage value, and the rising and falling signal edges are always asymmetrical. Duty cycle distortion in any block is the distortion of the duty cycle of the input waveform to the block [19, 20]. To maintain the same duty cycle of the input waveform in the output of the block, there is a need to have some delay for the rising and falling edge, and the duty cycle gets distorted if there is a difference in delay between the rising and the falling edge. The example of DCD is shown in Fig. 2.

$$DCD = rise_{delay} - fall_{delay}$$

For an input waveform with a 50% duty cycle, the above expression can be derived to

$$DCD = \frac{pulse\ with\ high - pulse\ with\ low}{2 * period}$$

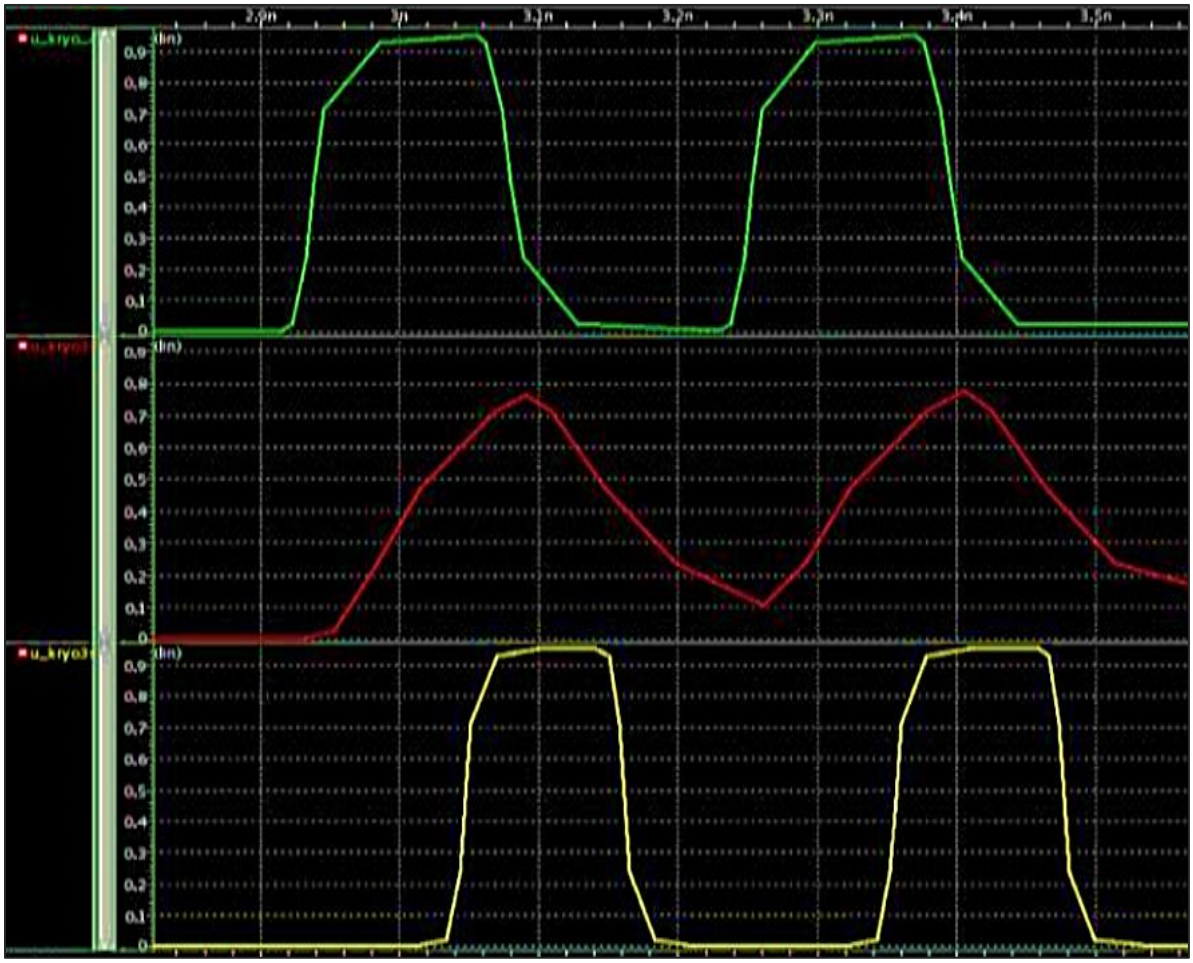

Fig. 2. Duty Cycle Distortion

2.4 Methodology

In infinisim clock edge, a particular clock pulse from the whole circuit is taken, analyzed for different duty cycles of 45%, 50%, and 55% in a particular corner. The outputs are generated both in text and jpeg format. The information given as inputs for the clock edge in the design shell is shown in Fig. 3.

-clock_name_list	CLKM1_lpass_q6ss_rcg_clk
-clocl_period_list	1.1
-corner	func_1.215v_ss_125c_rcw_ptsi
-data_files	
-email	
-input_clock_delay_time	0.1n
-input_clock_fall_time	0.01n
-input_clock_num_cycles	4
-input_clock_rise_time	0.01n
-name	clockedge_domain1
-num_cpu	10
-prcn_dc_list	45,50,55

Fig. 3. Inputs in Design Shell

3. Results and Discussions

One particular clock source is taken in a particular corner in the entire circuit. The duty cycle distortion analysis is done for the clock source by fixing the duty cycle as 45% and 50%, respectively.

3.1 Duty Cycle Distortion

The duty cycle percentage of all the leaf cells of a particular clock source is shown in Fig. 4. The original duty cycle of this clock is taken as 45%, and hence the buffers connected to the clock source should have a 45% duty cycle, and inverters will have a 55% duty cycle. But as the stages increase, there will be slight duty cycle variations for each cell. For buffers 40% - 50% variations are acceptable and for inverters 50% - 60% variations are acceptable. The clock source with a 45% duty cycle is taken for analysis, and the duty cycle distortion for each stage is calculated, and the results are shown in Fig. 4. As the buffers present in the paths are very large compared to inverters, the duty cycle points are very high, between 45% to 50%.

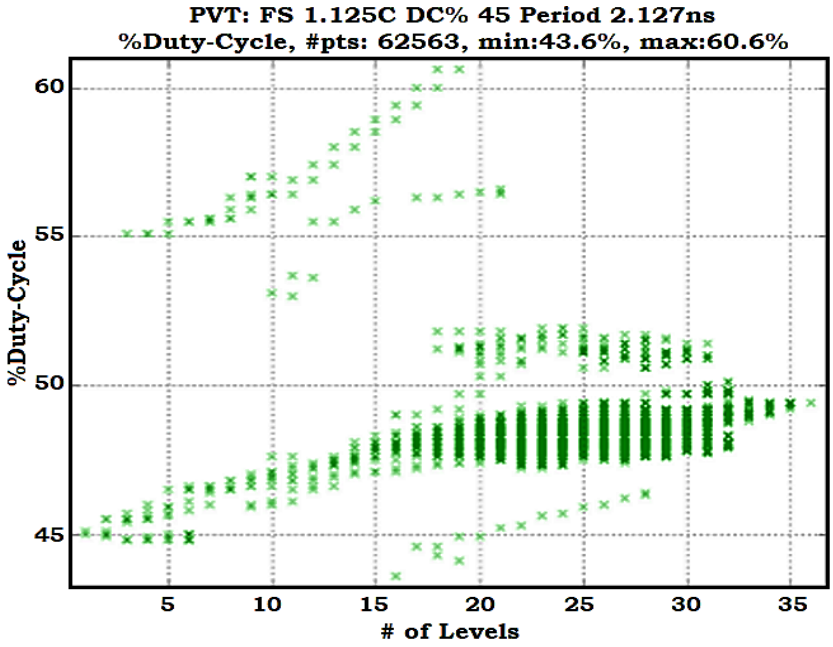

Fig. 4 DCD for 45% DC

Similarly, for a clock source with a 50% duty cycle, the maximum allowable range is 45% - 55%. The simulation is done for the same clock source, and by fixing the duty cycle values like 50%, the analysis is done, and the results are generated, as shown in Fig. 5.

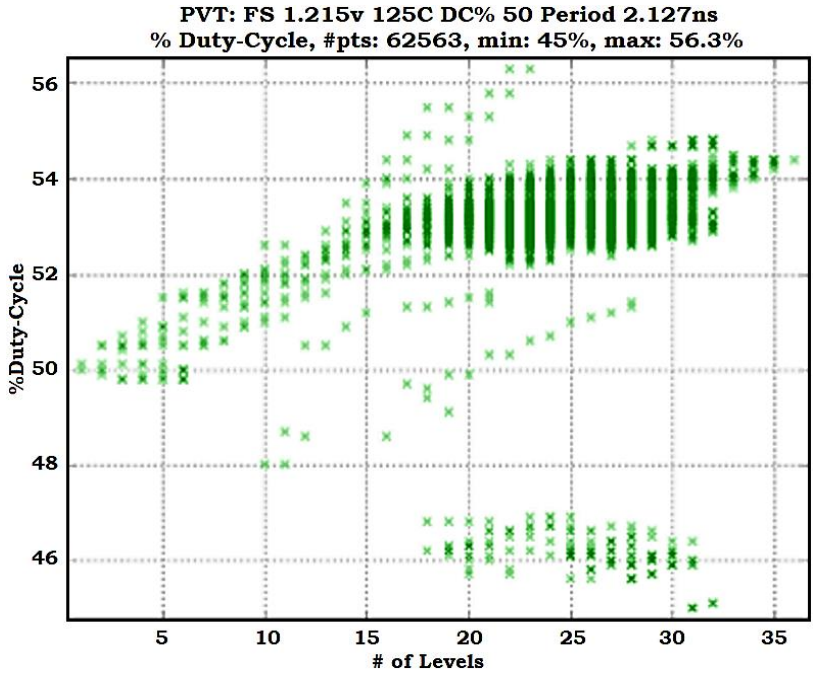

Fig. 5 DCD for 50% DC

3.2 Maximum and Minimum Voltage Variations

Here a corner with Cx and Mx voltages as 1.215V is used. Hence the maximum R2R voltage will be 1.215V, and the minimum voltage will be 0V. The max and min voltages violations at each stage are captured using clock edge and are shown in Fig. 6 and Fig. 7, respectively. The minimum of the maximum voltage and the maximum-minimum voltage can be identified exactly. The level at which the error is occurring also can be identified in the reports and the output diagram. The modifications can be made exactly hence providing accuracy.

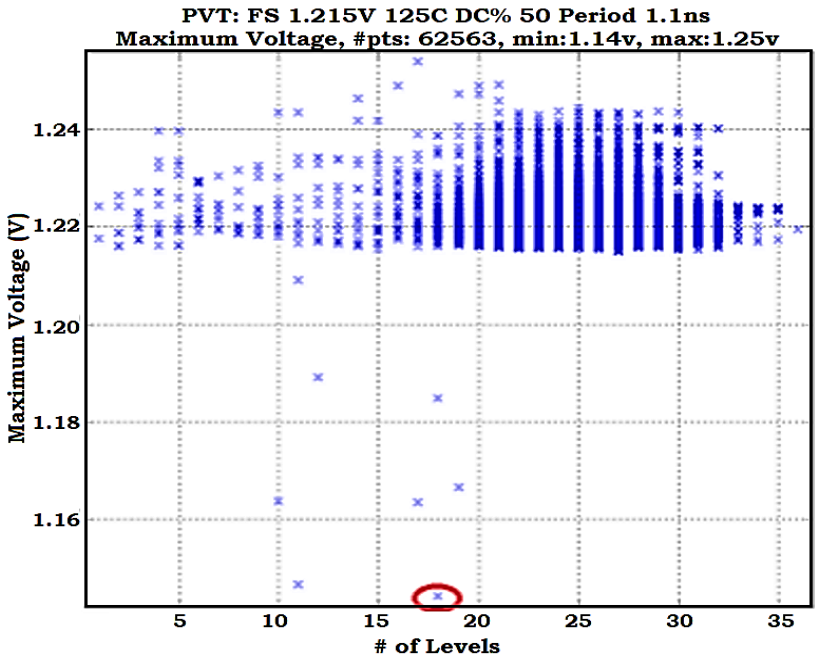

Fig. 6 Maximum Voltage Violations

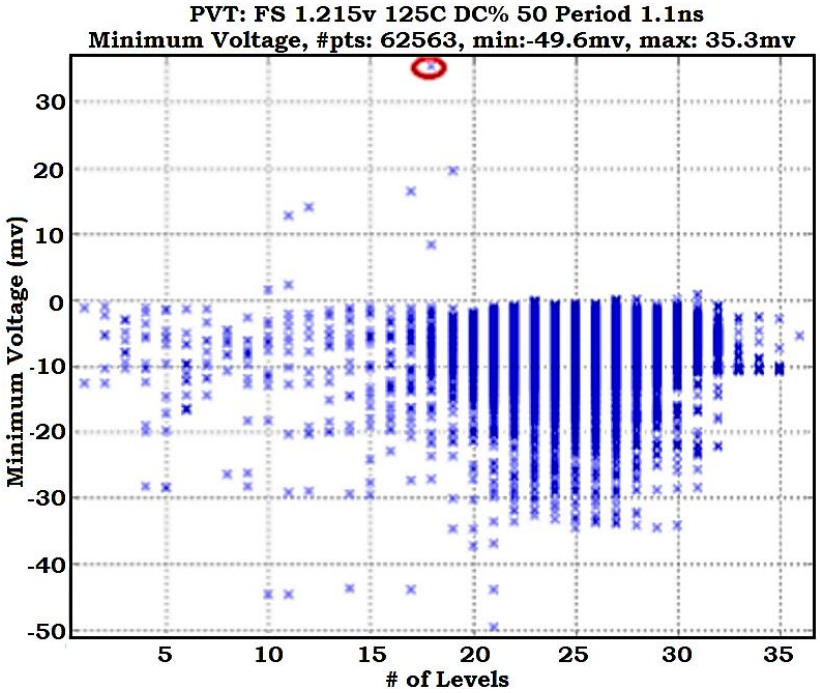

Fig. 7 Minimum Voltage Violations

The accuracy of the clock edge is very high since it uses fully SPICE simulations. The speed is optimized for multi- CPU for object vector cell analysis. The capacity of this simulation is high and can be used to simulate 100+ million devices.

3.3 Clock Edge Timing Reports

The timing reports of the clock source with DC 45% and 50% are shown in Table 1 and Table 2, respectively. These tables present the duty cycle, % duty cycle, time taken to reach maximum voltage and minimum voltage, rail to rail voltage (max and min), frequency of the clock source, and the direction of the pulse. From Table 1, it was observed that the maximum frequency of 7.33 occurred in the point of Pin 1 with 55.1% of the duty cycle. There are no major changes in maximum rail to rail voltage and minimum rail to rail voltage for all pinpoint levels.

Table 1. Timing Reports of CS with DC 45%

Point	DC	%DC	Rising-R2R	Falling-R2R	Max-R2R (v)	Min-R2R(v)	Freq. (GHz)	dir
clkin	9.57E-10	45	9.50E-12	9.50E-12	1.215	0	52.6	r
PIN 1	9.57E-10	45	6.70E-11	6.94E-11	1.217	-0.0011	7.33	r
PIN 2	9.60E-10	45.1	1.13E-10	9.53E-11	1.224	-0.0127	4.8	r
PIN 3	9.58E-10	45	2.00E-10	1.93E-10	1.215	-0.0011	2.55	r
PIN 4	9.68E-10	55.5	1.15E-10	1.01E-10	1.218	-0.0055	4.62	f
PIN 5	9.58E-10	55.1	1.93E-10	1.85E-10	1.215	-0.0011	2.64	f
PIN 6	9.67E-10	45.5	1.28E-10	1.11E-10	1.218	-0.0052	4.19	r
PIN 7	9.50E-10	45.1	1.14E-10	9.59E-11	1.224	-0.0127	4.76	r
PIN 8	9.54E-10	44.9	5.25E-11	3.77E-11	1.226	-0.1023	11.1	r
PIN 9	9.67E-10	55.1	1.25E-10	1.13E-10	1.217	-0.0030	10.7	f
PIN 10	9.68E-10	45.5	1.63E-10	1.40E-10	1.220	-0.0061	3.3	r

Similarly, from Table 2, it was observed that the maximum frequency of 7.31 has occurred in the Pinpoint of 1 with 50% of the duty cycle. There are also no major changes in maximum rail to rail voltage, which only falls between 1.215 to 1.226 volts. Also, the minimum rail-to-rail voltage falls between 0 to 0.1022 volts for all pinpoint levels.

Table 2. Timing Reports of CS with DC 50%

Point	DC	%DC	Rising-R2R	Falling-R2R	Max-R2R (v)	Min-R2R(v)	Freq. (GHz)	dir
clkin	1.06E-09	50	9.50E-12	9.50E-12	1.215	0	52.6	r
PIN 1	1.06E-09	50	6.73E-11	6.94E-11	1.217	-0.0013	7.31	r
PIN 2	1.07E-09	50.1	1.13E-10	9.53E-11	1.223	-0.0125	4.8	r
PIN 3	1.06E-09	50	2.00E-10	1.93E-10	1.216	-0.0022	2.55	f
PIN 4	1.07E-09	50.5	1.15E-10	1.01E-10	1.218	-0.0055	4.62	f
PIN 5	1.06E-09	50	1.93E-10	1.85E-10	1.215	-0.0011	2.64	r
PIN 6	1.07E-09	50.5	1.28E-10	1.11E-10	1.218	-0.0052	4.2	r
PIN 7	1.07E-09	50.1	1.14E-10	9.59E-11	1.224	-0.0127	4.76	r
PIN 8	1.06E-09	49.9	5.25E-11	3.77E-11	1.226	-0.1022	11.1	f
PIN 9	1.07E-09	50.5	1.25E-10	1.13E-10	1.217	-0.0030	4.21	r
PIN 10	1.07E-09	50.5	1.63E-10	1.40E-10	1.219	-0.0062	3.3	r

3.4 Final Summary Results

The summary gives the total pins that are valid for the simulation, out of which it also gives the information on any incomplete or missed pin values. It also results in the overall minimum and maximum values of slew, DC, %DC, R2R voltages, frequency, etc. The overall summary of the whole simulation for a clock source with a 50% duty cycle is presented in Table 3. The results show that the duty cycle has not been varied as in the case of clock edge with synopsis prime time tool. Results for 50% duty cycle were only observed, and the analysis is not as accurate as clock edge.

Table 3. Summary of the Entire Simulation with 50% and Duty Cycle

Point	Level	Slew Rise	Slew Fall	DC	%DC	Rising-R2R	Falling-R2R	Max-R2R	Min-R2R	Freq. GHz
Valid	62564	62564	62564	62564	62564	62558	62558	62564	62564	62564
Incomplete	0	0	0	0	0	0	0	0	0	0
Missing	0	0	0	0	0	6	6	0	0	0
Min_Value	0	4.25E12	3.57E12	4.44E-10	40.3	9.50E12	9.50E12	1.1441	0.04958	0.8
Max_Value	36	2.77E10	1.58E10	6.84E-10	62.2	6.06E10	4.67E10	1.2537	0.03534	52.6

4. Conclusion

In this article, the investigation of duty cycle distortion in clock channels with infinisim clock edges was carried out. The simulation and results of infinisim clock edge have also been discussed.

- The infinisim clock edge simulations are done for 28nm technology for a particular clock source.
- The results show that the total pins are valid for the simulation, and it gives the information of any incomplete or missed pin values.
- Also, the results reveal the overall maximum and minimum values of slew, DC, %DC, R2R voltages, frequency, etc.
- In the synopsis prime time tool, the duty cycle has not been varied as in the case of clock edge. It gives only 50% duty cycle results, and the analysis is also not as accurate as clock edge.
- This can also be done for all clock sources in the circuit for the betterment of simulation results without duty-cycle distortion.

References

[1] Te Liang, Zaiming Fu, Hanglin Liu, Ke Liu, and Yindong Xiao, Minimizing the Jitter of Duty Cycle Distortion Correction Technology Based on Cross Point Eye Diagram Correction, IEEE Access, 99 (2019) 1-10.

[2] W.J. Yun, A 0.1 to 1.5 GHz 4.2 mW All-Digital DLL with Dual Duty-Cycle Correction Circuit and Update Gear Circuit for DRAM in 66 Nm CMOS Technology, IEEE International Journal of Solid-State Circuits, (2008) 282-283.

[3] J. S. Wang, C. Y. Cheng, J. C. Liu, Y. C. Liu, and Y. M. Wang, A duty-Cycle-Distortion-Tolerant Half-Delay-Line Low-Power Fast-Lock-In all-Digital Delay-Locked Loop, Journal of Solid-State Circuits, 45(5) (2010) 1036-1047.

[4] Chaithanya Supe, Real-Time Implementation of Circuits, IEEE International Conference on Advances in Vision Computing, 1(4) (2014) 436-442.

[5] V. Ramadesigan, P. W. C. Northrop, S. De, S. Santhanagopalan, R. D. Braatz, and V. R. Subramanian, Modeling and Simulation of Lithium-Ion Batteries from a Systems Engineering Perspective, Journal of the Electrochemical Society, 159(3) (2012) 31-45.

[6] S. Sepasi, R. Ghorbani and B.Y. Liaw, A Novel on Board SOC Estimation Method for Aged Li-Ion Batteries Based on Model Adaptive EKF, Journal of Power Sources, 245 (2014) 337-344.

[7] F. Anceau, A Synchronous Approach for Clocking VLSI Systems, IEEE International Journal of Solid-State Circuits, 17 (2016) 51-56.

[8] Sarfati, B. Frankel, Y. Birk, and S. Wimer, Optimal VLSI Delay Tuning by Space Tapering with Clock-Tree Application, IEEE Transactions on Circuits and Systems-I, 64(8) (2017) 2160-2170. Doi: 10.1109/TCSI.2017.2695100.

[9] Y. Kaplan and S. Wimer, Mixing Drivers in Clock-Tree for Power Supply Noise Reduction, IEEE Transactions on Circuits and Systems, 62(5) (2015) 1382-1392.

[10] Chunchun Sui, Siqi Bai, Ting Zhu, Christopher Cheng, and Daryl G. Beetner, New Methods to Characterize Deterministic Jitter and Crosstalk-Induced Jitter from Measurements, IEEE Transactions on Electromagnetic Compatibility, 57 (2015) 877-884.

[11] Yi Cai, Bernd Laquai and Kent Luehman, Jitter Testing for Gigabit Serial Communication Transceivers, IEEE Design and Test of Computers, 9(1) (2002) 66-74.

[12] Zamek, and Zamek, Definitions of Jitter Measurement Terms and Relationships, Test, 10 (2005) 28-34.

[13] J. Balcarek, P. Fiser, and J. Schmidt, Duty Cycle Distortion in Clock Based Networks in Digital System Design (DSD), 13th Euro micro-Conference on Architectures, Methods and Tools, (2010) 805-808.

[14] M. Ali Altunchu, Taner Guven, Yasar Becerikli, and Suhap Sahin, Analysis of Clock Edges on Digital Circuits, International Journal of Information and Electronics Engineering, 5(6) (2015) 345-349.

[15] M.A.Franklin and D.F.Wann, Asynchronous and Clocked Control Structures for VLSI Based Interconnection Networks, Proceedings-Symposium on Computer Architecture and High-Performance Computing, (2011) 50-59.

[16] V. Adler and E. G. Friedman, Repeater Design to Reduce Delay and Power in Resistive Interconnect, IEEE Transactions on Circuits and Systems-II, 45 (2016) 607-616.

[17] Somasekhar and V. Visvanathan, A 230-MHz Half-Bit Level Pipelined Multiplier using True Single-Phase Clocking, IEEE Transactions on VLSI Systems, 1 (2013) 415-422.

[18] Gijin Park, Jaeduk Han, and Woorham Bae, Design and Analysis of Asynchronous Sampling Duty Cycle Corrector, Electronics, 10 (2021) 2594-2599.

[19] Kao, Design, and Implementation of Fast Locking All-Digital Duty Cycle Corrector Circuit with Wide Range Input Frequency, Electronics, 10 (2021) 71-76.

[20] Hamzaoglu and J. Patel, Reducing Jitter Application Time for Embedded Cores, 29th Annual International Symposium on Jitter Applications, (2009) 260-267.

[21] Surendiran. R, and Alagarsamy. K, Privacy Conserved Access Control Enforcement in MCC Network with Multilayer Encryption". SSRG International Journal of Engineering Trends and Technology (IJETT), 4(5) (2013) 2217-2224.

[22] Gavaskar, S., Surendiran, R. and Ramaraj, D.E., Three counter defense mechanism for TCP SYN flooding attacks. International Journal of Computer Applications, 6(6) (2010) 0975-8887.

[23] Subburaj.V, Srinivasan.M, Surendiran. R , Sundaranarayanan. R. DDoS Defense Mechanism by Applying Stamps using Cryptography. International Journal of Computer Applications. 1(6), ISSN: 0975 – 8887, (2010) 48-52. DOI: 10.5120/143-262.