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Staircase Modulation using GWO Technique for CHB-MLI with Symmetrical and Asymmetrical Mode

Asala. S. AL-Dmour [1], Hussein. D. AL-Majali [2], Ziyad. S. AL-Majali [3]

Department of Electrical Engineering, Faculty of Engineering Mu'tah University, Jordan

[1]asaladmour4@gmail.com, [2]halmajali@mutah.edu.jo, [3]ziyad@mutah.edu.jo

Abstract *- In this research, the Grey Wolf Optimizer GWO algorithm through staircase modulation strategy is utilized to estimate switching angles and bridge DC voltage (input variables) of five-level and seven-level cascade H-Bridge inverters. Estimated values make sure that total harmonics distortion THD of the selected inverters will be minimized as possible. The simulation results using MATLAB/Simulink software and harmonic spectrum using Fast Fourier Transform window for five and seven-level CHB inverter in symmetric (equal DC voltage) and asymmetric (un-equal DC voltage) mode have been presented based on the magnitude of THD in output voltage. The analysis has been done for both R and RC loads.*

Keywords — *Cascaded H-bridge multilevel inverter (CHB-MLI), Grey Wolf Optimizer (GWO) algorithm, Staircase modulation, Total Harmonic Distortion (THD).*

I. INTRODUCTION

Multi-Level Inverters (MLI) have become more appealing in industrial applications requiring high-power and high-voltage due to their ability to attain high power ratings. The distinct configuration of MLI allows them to synthesize higher voltages with less harmonic distortion, less electromagnetic interference, and high efficiency. Due to the efficiency and quality of the output voltage in MLI, researchers have taken an interest in developing and continuously modifying MLI over the past years [1-3].

The Multi-Level Inverter MLI was commonly grouped into three distinct topologies: Diode-Clamped MLI topology DC-MLI [4], Capacitor-Clamped MLI topology CL-MLI [5], and Cascading H-Bridges MLI topology CHB-MLI [6]. As the NPC-MLI inverter uses many diodes clamped so, if the levels number is more than three, the complexity and costs are therefore rising. Also, for FC-MLI Inverter, it uses capacitors clamped that cause voltage sag problems. In addition, it requires a huge number of devices when levels number increases, which is difficult to control. CHB-MLI is used to eliminate the disadvantages of two topologies. In that, CHB-MLI requires fewer components than the other topologies. So, it reduces the cost. This inverter is suitable for high power and HV applications due to its many features and its modular structure, which enables it practical to significantly increase levels number and reach a higher voltage [7,8].

CHB-MLI can be realized as either equal or unequal, based on the magnitude of the DC voltage sources. If the value of DC voltage sources for each bridge is equal, it is said to be symmetrical [9]. While if each bridge is supplied with a non-equal magnitude of DC voltage sources, this arrangement is said to be asymmetrical [10,11]. Since the construction of MLI is mainly concerned with ensuring that it meets power quality standards, total harmonic distortion is an important factor. Using the THD factor, power quality for MLI is tested where the power quality is increased when the THD value is decreased. Therefore, it must be ensured that the output waveform of MLI contains THD within acceptable limits. To minimize THD of the voltage output waveform, it is vital to appropriate the choice of switching angles and input DC voltage sources in such a way that the output waveform is as sinusoidal as feasible. Some papers using a by-pass valve to reduce the THD for inverter mode of HVDC converter [12-16].

There are several modulation strategies in MLI that result in minimum THD and improved power quality, such as Sinusoidal PWM [17,18] and Space Vector PWM [19,20]. A more effective and efficient modulation strategy called a Staircase modulation strategy is also used in the control of MLI. The staircase modulation strategy is one of the low-frequency strategies appropriate for the MLI circuit. This technique involves selecting appropriate angles to eliminate low-order harmonics in the voltage output waveform, thus reducing the THD. Fourier theory is used to analyze output waveform, which results in a set of non-linear transcendental equations. The main problem with this technique is to solve these equations to obtain the appropriate switching angles. To solve these nonlinear equations, numerical iterative methods such as newton raphson's method [21,22] and Resultant Theory [23] can be used. However, these methods lead to numerical difficulty and an arithmetic burden.

These equations can be resolved by using heuristic optimizing algorithms as an alternative to numerical iterative methods for obtaining the appropriate switching angles and values of DC sources that limit the total harmonic distortion. Examples of Heuristic optimization algorithms are genetic

algorithm GA [24,25], particle swarm optimization PSO [26,27], and grey wolf optimizer GWO. Among these, GWO is very efficient and has recently been used in power electronic applications.

In this paper, the staircase modulation technique has been employed through GWO, which finds optimal DC voltage sources and optimal switching angles for SCHB-MLI and ACHB-MLI inverters for five-level and seven-level so as to reduce the. The rest of this paper is organized as follows: Section II introduces the structure of the suggested CHB-MLI. Section III describes the working of the Staircase modulation technique on a 7-level CHB inverter. Section IV introduces the overview of GWO. Applying the GWO algorithm in Staircase modulation to computing optimal switching angles and input dc voltage of 7-level CHB inverter is presented in section V. Section VI presented simulation results and comparison. Finally, the conclusions are presented in Section VII.

II. CASCADED H-BRIDGE MULTILEVEL INVERTER

CHBMLI comprises multiple single-phase H-bridge inverters linked in a sequence to create a staircase waveform for the output voltage. Each isolated DC source in this type of MLI is linked to an H-Bridge inverter. Batteries, wind turbines, fuel cells, or PV can be input DC voltage sources. Via interfacing, the DC source as input to alternating current output using 4 switches, S1, S2, S3, and S4, and four main diodes, each cell will produce 3 different output voltages, Vdc, zero, and -Vdc. The number of DC voltages required is the same as the number of H-Bridges. If n is the number of DC voltage sources, the number of levels of output voltage for CHB-MLI equals m=2n+1. Thus, by adding more cells in series, CHB-MLI levels can be conveniently increased [28,29].

The output voltage of CHBMLI is synthesized by summing output voltages generated from each cell. The magnitude of Vout is given by:

$$v_{out} = v_{o1} + v_{o2} + v_{o3} + \cdots + v_{on}$$

Where:

v_{out}: Represents the output voltage of CHBMLI.

n: The number of H-Bridge cells.

v_{on}: Represents nth H-bridge output voltage.

Fig.1 illustrates the general case of single-phase CHBMLI. As demonstrated, an inverter is made up of n H-bridge cells connected in series. There will be four IGBT switches for each H-Bridge, one separated DC source with equal voltage for all cells. The staircase waveform output voltage for the general n level CHB MLI is illustrated in fig.2. Accordingly, the then-general waveform of CHBMLI is analogous to the ideal sine wave.

There are two types of CHBMLI based on the magnitude of DC voltage input, and they are symmetric CHB inverter and asymmetric CHB inverter. In symmetric mode, the same magnitude of input DC voltage is provided for all cells. The ratio of the DC input voltage is 1:1 [30]. Whereas each cell has a different DC voltage source value in an asymmetric configuration. The input DC voltage sources are fed to cells in different ratios. These ratios can be integer or non-integer. Previous studies have used integer ratios such as ternary (1:3) and binary (1:2) ratios to achieve more output voltage levels without increasing the number of H-bridge cells. Thus, THD reduces as levels number increases. As for a staircase modulation technique, non-integer ratios between the values of DC voltage sources are used to achieve minimum THD [31].

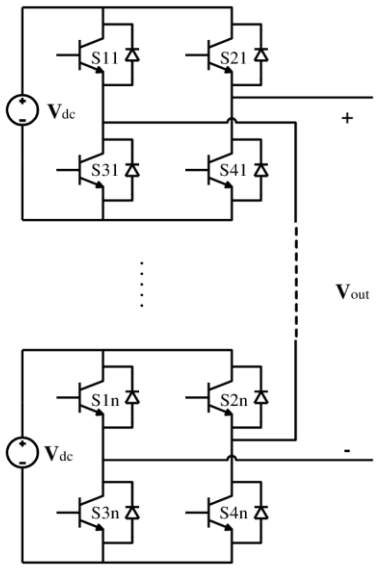

Fig 1Cascaded H-Bridge Multi-Level Inverter CHBMLI Configuration

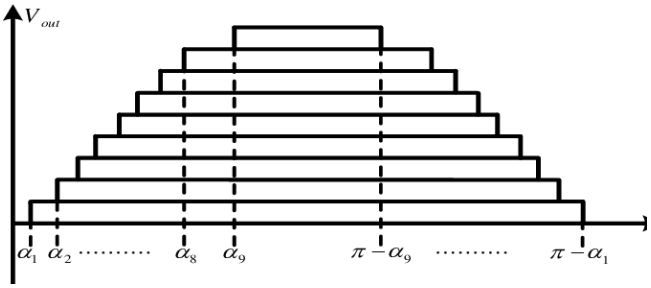

Fig 2 output voltage waveform of CHBMLI

II. STAIRCASE MODULATION

For CHB-MLI, the staircase modulation strategy can conveniently be used to attain high quality. This is due to the unique structure of CHB-MLI. The basic idea of staircase modulation strategy is to find switching angles more simply than conventional methods to ensure that lower order harmonics are eliminated at the output voltage. Because all IGBT switches operate at a basic switching frequency, a staircase modulation strategy has lower switching losses. The suggested method is based on the idea that the phase voltage of the inverter crosses with an original sinusoidal waveform at symmetric points on the Y-axis. Fig.3 illustrates the principle of this approach. As shown in the figure, the

symmetrical points: V_{a1}, $V_{a2}$and V_{a3}, which are output voltages of a 7-level inverter for H-bridge cells [32].

The Fourier series of staircase waveforms can be expressed as:

$$V_{AN} = \frac{4V_{dc}}{\pi} \sum_{k=1,3,5,\dots}^{\infty} \frac{1}{k}\{\cos(k\alpha_1) + \cos(k\alpha_2) + \cos(k\alpha_3)\}\sin(k\omega t) \quad (1)$$

Where:$0 \le \alpha_3 \le \alpha_3 \le \alpha_1 \le \frac{\pi}{2}$

Where: k: is the harmonic order, α_1, α_2, and α_3: are the independent switching angles.

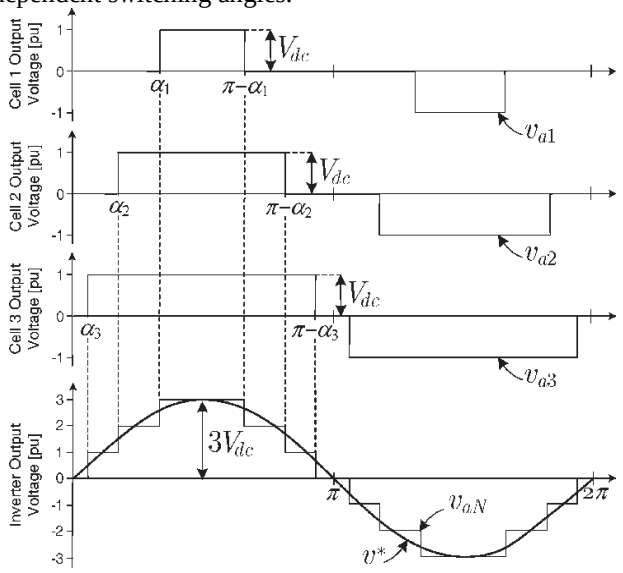

Fig 3 Simple staircase modulation of a 7-level inverter

With the aid of the Fourier series equation can be eliminated the lower order harmonics with selection appropriate switching angle. For 7-level CHBMLI with 5th & 7th harmonic elimination, the equations are as follows [33]:

$$V_f = \frac{4V_{dc}}{\pi}(K_1\cos(\alpha_1) + K_2\cos(\alpha_2) + K_3\cos(\alpha_3)) \quad (2)$$

$$V_5 = \frac{4V_{dc}}{5\pi}(K_1\cos(5\alpha_1) + K_2\cos(5\alpha_2) + K_3\cos(5\alpha_3)) \quad (3)$$

$$V_7 = \frac{4V_{dc}}{7\pi}(K_1\cos(7\alpha_1) + K_2\cos 7(\alpha_2) + K_3\cos(7\alpha_3)) \quad (4)$$

However, this technique contains a huge number of equations with the increasing number of levels in the inverter and thus requires complicated techniques and takes a long time to solve these equations. As a result, the Grey Wolf Optimization GWO algorithm can be used to find the optimum switching angle value for a lesser number of iterations with the least THD.

III. GREY WOLF OPTIMIZER

The GWO is a novel algorithm for meta-heuristic optimization used to solve numeric problems optimally. The GWO algorithm is inspired by the hierarchy of leadership and the predation behavior of the pack of gray wolves. The Grey wolves were split into four categories in this algorithm: alpha α, beta β, delta δ, and omega ω. The hierarchy of gray wolves is seen in Fig.4. The leader and decision-maker is alpha, which may be male or female. The α makes decisions about hunting, sleeping, waking time, etc., and dictates these decisions to the pack. β and δ are the 2nd and 3rd levels of the hierarchy, and their job is to assist Alpha in making a decision. The majority of the total is placed at the bottom of the hierarchy, where it is referred to as Omega [34].

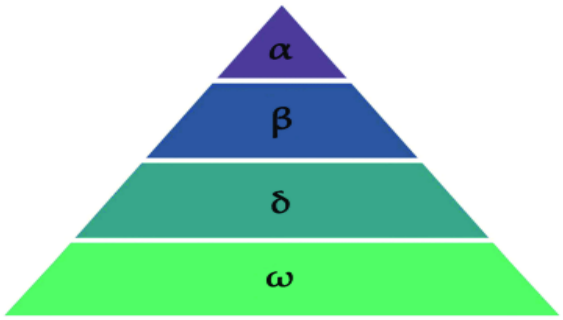

Fig 4 The hierarchy of a grey wolf

A mathematical model is used to simulate the wolf hierarchy. The first element, alpha, is deemed the best solution. And therefore, beta and delta are the 2nd and 3rd best solutions, respectively. Omega is assumed to be the remaining candidate solution. The hunting or optimization in the GWO algorithm is led by Alpha, Beta, and Delta. The omega wolves will follow α, β, and δ. GWO algorithm's mathematical model is divided into three stages: encircling prey, hunting, attacking prey, searching for prey. The procedure is as follows:

A. Encircling prey

During optimization, the positions of wolves around the prey are updated, according to the following equations:

$$\vec{D} = |\vec{C}.\vec{X}_P(t) - \vec{X}(t)| \quad (5)$$

$$\vec{X}(t+1) = \vec{X}_P(t) - \vec{A}.\vec{D} \quad (6)$$

Where t marks present iteration, vector $\vec{D}$ indicates the measured difference between the prey and predator location, $\vec{X}p$ denotes the prey's location vector and vector $\vec{X}$ Refers to the gray wolf's location. The coefficient vectors and are determined using the equations below. The coefficient vector $\vec{A}$ and $\vec{C}$are expressed using the equations below:

$$\vec{A} = 2\vec{a}\vec{r}_1 - \vec{a} \quad (7)$$

$$\vec{C} = 2\vec{r}_2 \quad (8)$$

Where a is reduced linearly from two to zero over the course of iterations, and $\vec{r}_1$&$\vec{r}_2$ denotes the random vectors in the range between zero and 1.

B. Hunting

It is presumed that α, β, and δ have a better knowledge of the location of prey. Consequently, the 3 best solutions that are obtained so far are retained, then oblige omega to update their positions to the best quest agent's location. Where the omega positions are updated via the following equations:

$$\vec{D}_\alpha = |\vec{C}_1\vec{X}_\alpha - \vec{X}|\,,\ \vec{D}_\beta = |\vec{C}_2\vec{X}_\beta - \vec{X}|\ ,\vec{D}_\delta = |\vec{C}_3\vec{X}_\delta - \vec{X}| \quad (9)$$

$$\vec{X}_1 = \vec{X}_\alpha - (\vec{D}_\alpha).\vec{A}_1\,,\ \ \vec{X}_2 = \vec{X}_\beta - (\vec{D}_\beta).\vec{A}_2,\ \ \vec{X}_3 = \vec{X}_\delta - (\vec{D}_\delta).\vec{A}_3 \quad (10)$$

$$\mathrm{X(t+1)} = \frac{(\vec{\mathrm{X}}_1 + \vec{\mathrm{X}}_2 + \vec{\mathrm{X}}_3)}{3} \quad (11)$$

Where: A1, A2, and A3 denotes random vectors

C. Attacking prey

When the prey stops moving, the grey wolves attack it to end the hunt. Gray wolves approach the prey by reducing the value of a, where α decreases from 2 to 0, which makes it nearer to the prey over the iterations. The value of A is also reduced by a, where A is a random value in an interval {-a, a}. When A random values are in [-1 1], a search agent's next position will be somewhere between its current position and the position of prey.

D. Search for prey (exploration)

Based on where alpha, beta, and delta are located, the grey wolves separate to search for prey and unite to attack the prey. |A|>1 or |A|<1 are utilized to indicate the exploration process occurs. If |A|>1, the grey wolves diverge from the prey and converge the prey if |A|<1.

C is a vector containing random values in [0, 2], which is another part of Grey Wolf Optimization that favors exploration. This portion provides random weights for prey in order to stochastically emphasize if C is greater than 1 or deemphasize if C is lesser than 1 on the effect of prey in defining the distance.

The GWO principle is applied to find the optimum switching angle and dc input sources for CHBMLI in symmetrical and asymmetrical mode to minimize overall harmonic distortion and increase output voltage power efficiency.

IV. THD OPTIMIZATION USING GREY WOLF OPTIMIZATION

In this work, the GWO algorithm is utilized to estimate the required switching angles and the DC voltages of multi-level cascaded H-bridge inverters (input variables) that corresponds to minimizing the THD. Where the objective function (fitness) is:

Fitness = minimize (THD value)

The proposed GWO algorithm estimates the input variables of 5 and 7 level CHB inverters by performing Simulink THD calculation. In this work, each GWO searching agent represents the required input variables of the multi-level inverter required to minimize the THD under the conditions of symmetrical, Asymmetrical connection. The suggested algorithm could be outlined in the following steps:

Step 1: Begin by determining the number of wolves in the population, the maximum number of iterations, the lower and upper limits, and the problem dimension.

Step 2: utilize the objective function script to calculate the fitness value.

Step 3: After collecting the fitness value, save the first-best value as the alpha score, the second-best value as the beta score, and the third-best value as the delta score in their respective places. It is important to understand that the stored fitness and is the same for the first iteration.

Step 4: update the parameters a, A, C

Step 5: update the wolves' positions based on α, β, and δ positions. Check the wolves' positions with the boundaries and return them to the specified range in case they deviate from it.

Step 6: Repeat steps two to five until the maximum iteration is reached and return the best score and position of that run number and store it.

Step 7: return the minimum best score with its corresponding position for the specified condition.

Fig.5 presents a flowchart of the proposed GWO algorithm. GWO algorithm takes the specified boundaries into consideration by putting constraints on the range of switching angles and DC voltages. Also, it illustrates the detailed steps of GWO implementation.

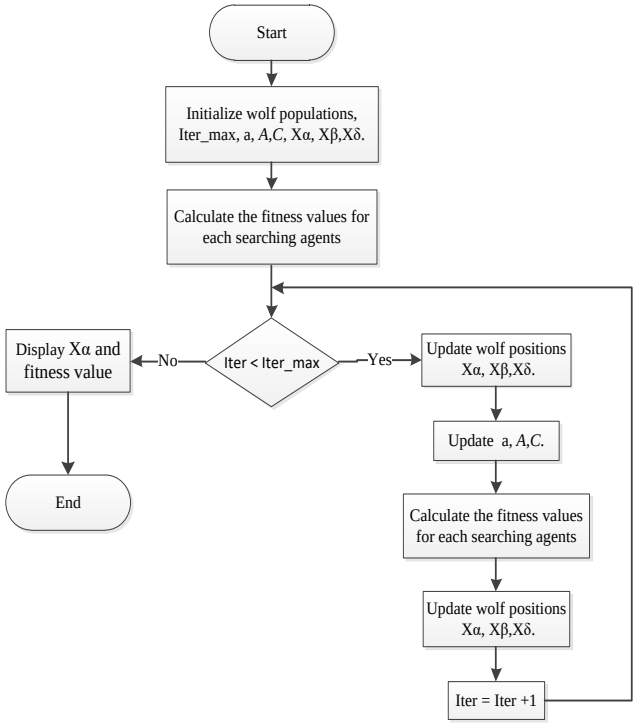

Fig 5 Flow chart of GWO algorithm

V. SIMULATION RESULT

Matlab/Simulink has been carried out for 5 and 7 levels CHB-MLI for both symmetrical and asymmetrical modes. Was presented and discussed the achieved results from the

GWO algorithm that calculated the required input variables in order to minimize the THD of CHBMLI (5 and 7 levels).

Symmetrical and asymmetrical 7-level CHBMLI consists of three H-bridges connected in series, each with four switching devices. Six different pulses were generated based on a1, a2, and a3 switching angles to perform the pulsing staircase technique. For the symmetrical mode, the Simulink model deals only with the base three switching angles and shows the effect of angles shifting on the THD of MLI. In the case of asymmetrical mode, the DC voltages of the series bridges will be manipulated along with the switching angles to provide better harmonic distortion of the conducted system.

The results obtained from Table (1) showed that for resistive load, the Asymmetrical operation mode of the 7-level inverter provided the better THD values. Moreover, connecting the inverter to the grid reduces THD as well. Table (2) illustrates that we can conclude the same results from a 7-level inverter for a resistive–capacitive load.

Table 1: 7-Level inverter results with R-load under different conditions

Searching Agents = 50, maximum iteration = 500				
Optimized Values	**Stand alone (Sym)**	**Grid-connected (Sym)**	**Stand alone (Asym)**	**Grid-connected (Asym)**
α_1 (deg)	26.370	13.556	26.616	20.320
α_2 (deg)	51.540	30.000	51.498	46.087
α_3 (deg)	77.155	90.000	77.143	71.973
V_{dc1} (V)	100	100	100	100
V_{dc2} (V)	100	100	85	85
V_{dc3} (V)	100	100	100	100
THD (%)	31.7264	31.0704	31.2197	30.9373

Table 2: 7-Level inverter results with RC load under different conditions

Searching Agents = 10, maximum iteration = 100				
Optimized Values	**Stand alone (Sym)**	**Grid-connected (Sym)**	**Stand alone (Asym)**	**Grid-connected (Asym)**
α_1 (deg)	29.309	29.773	0.185	0.870
α_2 (deg)	59.366	58.212	30.451	30.000
α_3 (deg)	86.787	87.057	55.510	55.228
V_{dc1} (V)	100	100	100	100
V_{dc2} (V)	100	100	99.625	99.584
V_{dc3} (V)	100	100	85.881	87.918
THD (%)	15.1094	14.5552	14.5891	14.1204

Symmetrical and asymmetrical 5-level CHBMLI consists of two H-bridges connected in series, each with four switching devices. Four different pulses were generated based on α1and α2 switching angles to perform the pulsing staircase technique. For the symmetrical mode, the Simulink model deals only with the base two switching angles and shows the effect of angles shifting on THD of MLI. In the case of asymmetrical mode, the DC voltages of the series bridges will be manipulated along with the switching angles to provide better harmonic distortion of the conducted system.

It can be seen from Table (3) that the symmetrical operation mode of the 5-level inverter with resistive provided the best THD values compared to Asymmetrical. On the other hand, still, the grid-connected system scoring better THD for the same inverter level. Table (4) showed the effect of resistive–capacitive load on the 5-level inverter, and it can be seen that the Asymmetrical mode recorded the minimum THD compared to the other operating conditions.

It's notable that the Asymmetrical grid-connected achieved the lowest value of THD for 7-level CHB inverter with the conducted loads and for 5-level CHB inverter with resistive – capacitive load only.

Table 3: 5-Level inverter results with Resistive load under different conditions

Searching Agents = 10, maximum iteration = 100				
Optimized Values	**Stand alone (Sym)**	**Grid-connected (Sym)**	**Stand alone (Asym)**	**Grid-connected (Asym)**
α_1 (deg)	25.562	13.692	4.328	14.327
α_2 (deg)	60.000	48.796	38.760	49.393
V_{dc1} (V)	100	100	100	100
V_{dc2} (V)	100	100	89.298	98.935
THD (%)	44.2870	43.1647	44.6255	43.1623

Table 4: 5-Level inverter results with RC load under different conditions.

Searching Agents = 10, maximum iteration = 100				
Optimized Values	**Stand alone (Sym)**	**Grid-connected (Sym)**	**Stand alone (Asym)**	**Grid-connected (Asym)**
α_1 (deg)	19.447	6.874	17.011	11.141
α_2 (deg)	56.447	45.661	54.029	50.444
V_{dc1} (V)	100	100	100	100
V_{dc2} (V)	100	100	99.267	97.950
THD (%)	28.3114	27.7052	27.8650	27.2222

Figures (6 to 9) showed the FFT analysis of 7-level output voltages under various operation modes with resistive load.

Figures (10 to 13) illustrated the FFT analysis of 7-level output voltages under various operation modes with the resistive-capacitive load.

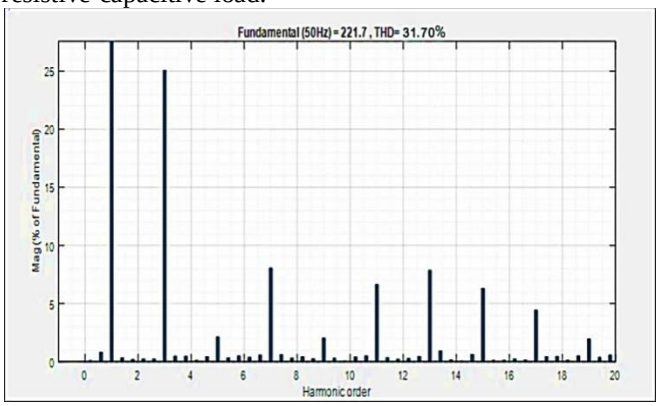

Fig 6 FFT analysis of Symmetric standalone 7-level inverter with R-load

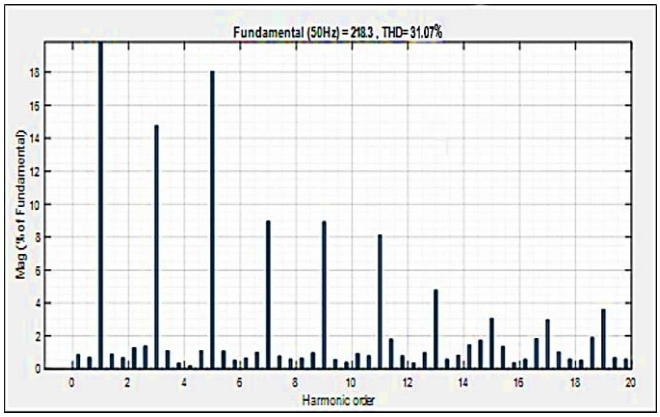

Fig 7 FFT analysis of Symmetric grid-connected 7-level inverter with R-load

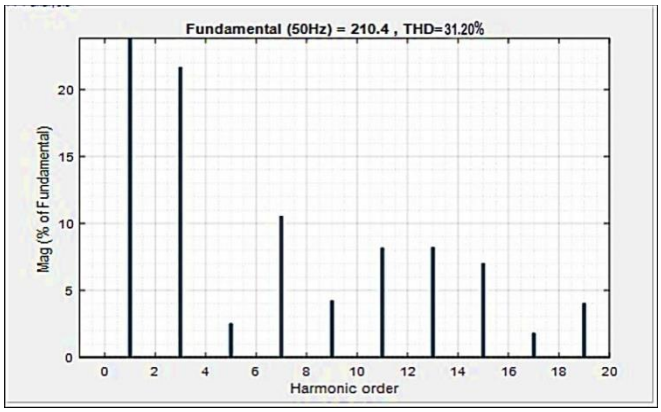

Fig 8 FFT analysis of Asymmetric standalone 7-level inverter with R-load

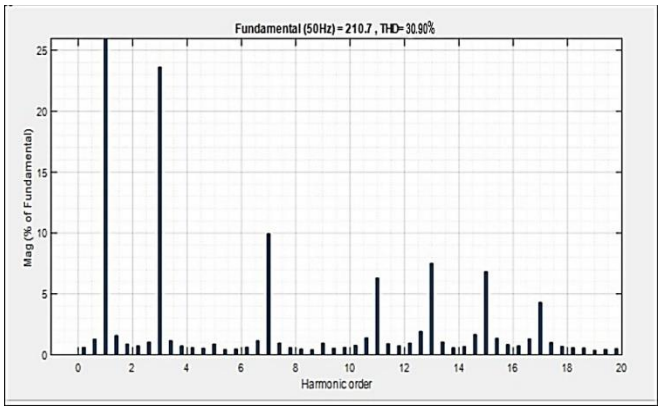

Fig 9 FFT analysis of Asymmetric grid-connected 7-level inverter with R-load

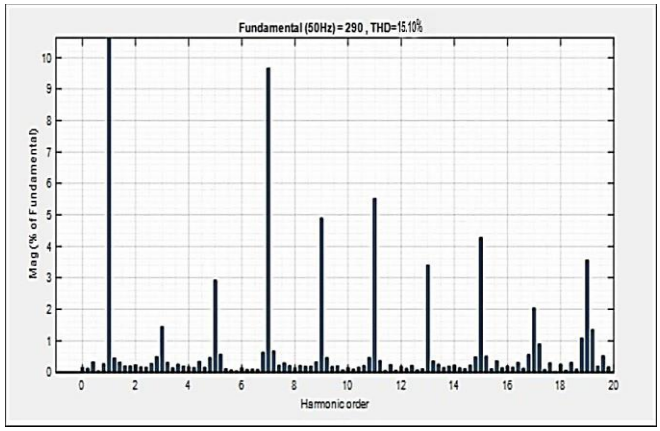

Fig 10 FFT analysis of Symmetric standalone 7-level inverter with RC-load.

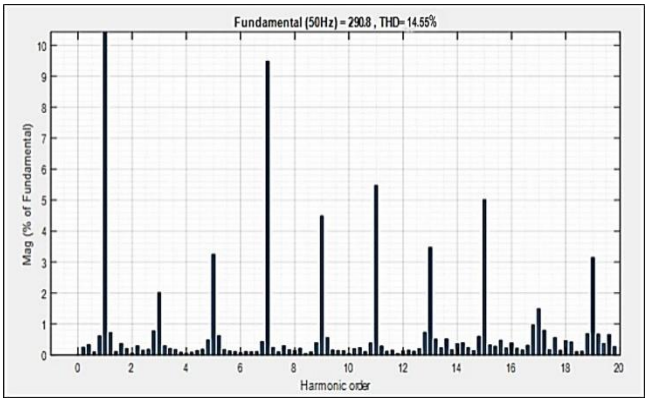

Fig 11 FFT analysis of Symmetric grid-connected 7-level inverter with RC-load.

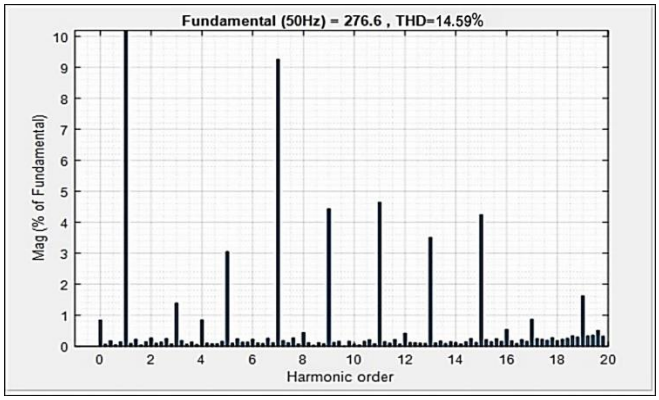

Fig 12 FFT analysis of Asymmetric standalone 7-level inverter with RC-load.

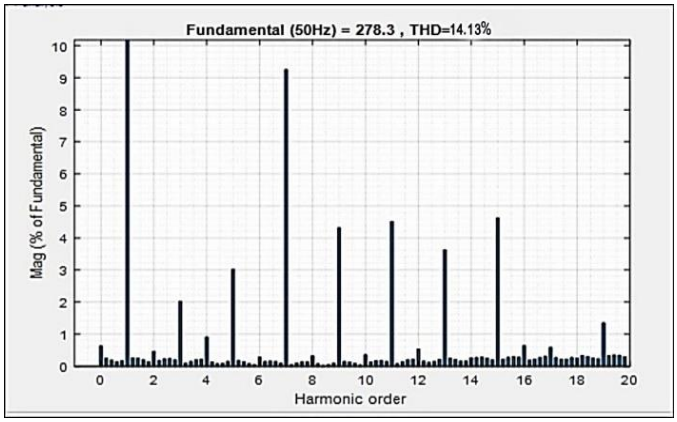

Fig 13 FFT analysis of Asymmetric grid-connected 7-level inverter with RC-load

Figures (14 to 17) showed the FFT analysis of 5-level output voltages under various operation modes with resistive load.

Figures (18 to 21) illustrated the FFT analysis of 5-level output voltages under various operation modes with resistive - capacitive load.

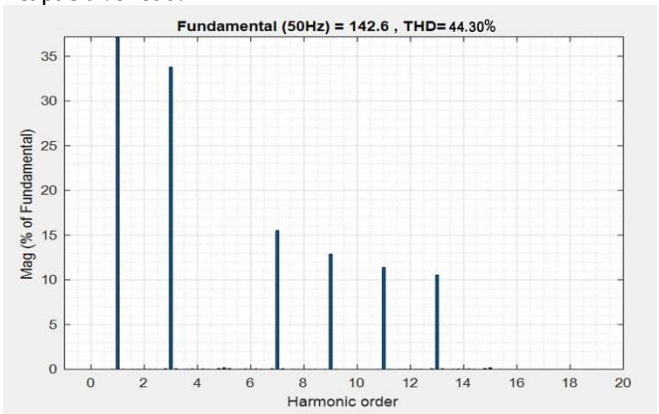

Fig 14 FFT analysis of Symmetric standalone 5-level inverter with R-load.

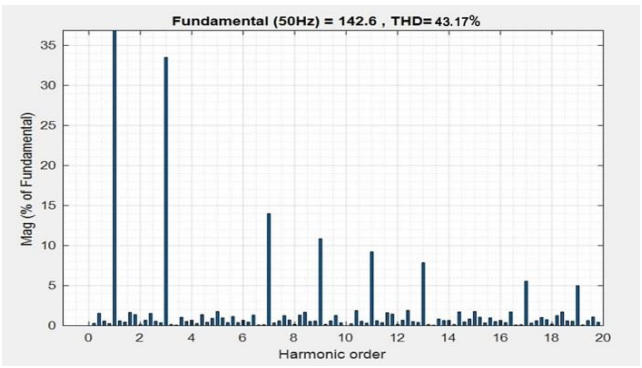

Fig 15 FFT analysis of Symmetric grid-connected 5-level inverter with R-load.

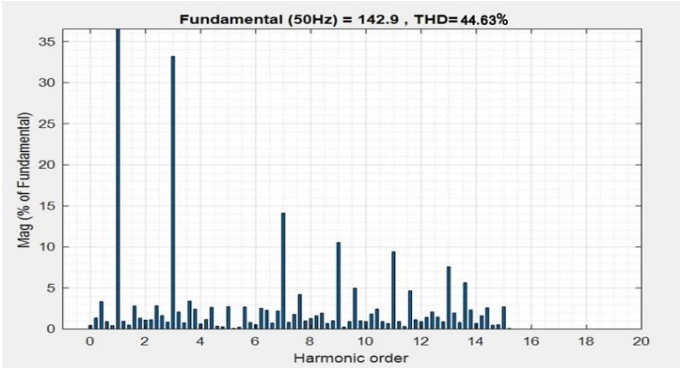

Fig 16 FFT analysis of Asymmetric standalone 5-level inverter with R-load.

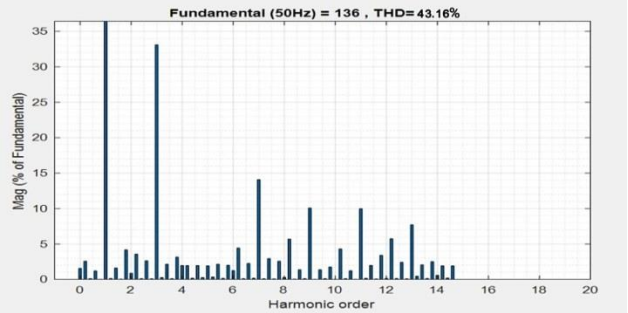

Fig 17 FFT analysis of Asymmetric grid-connected 5-level inverter with R-load.

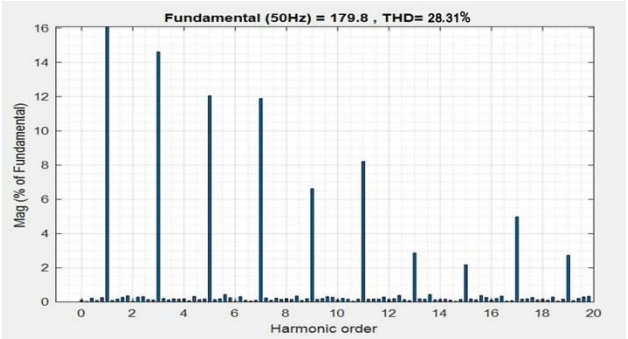

Fig 18 FFT analysis of Symmetric standalone 5-level inverter with RC-load

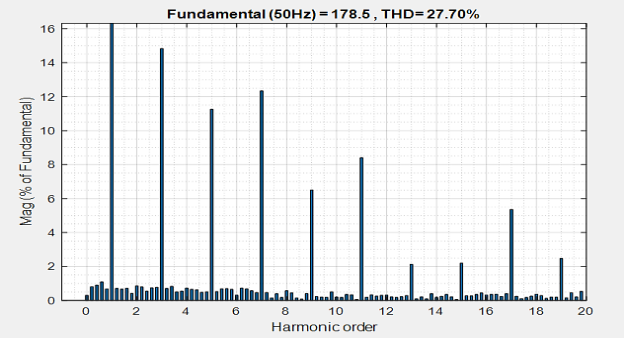

Fig 19 FFT analysis of Symmetric grid-connected 5-level inverter with RC-load.

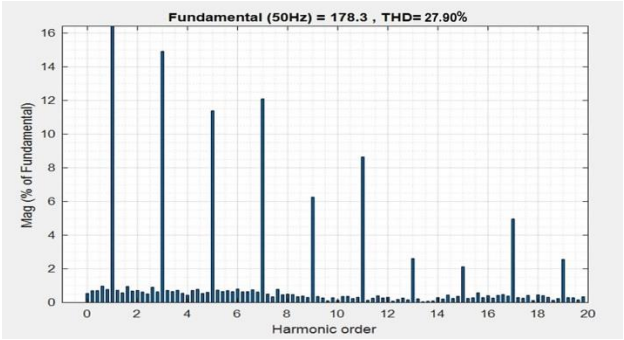

Fig 20 FFT analysis of Asymmetric standalone 5-level inverter with RC-load.

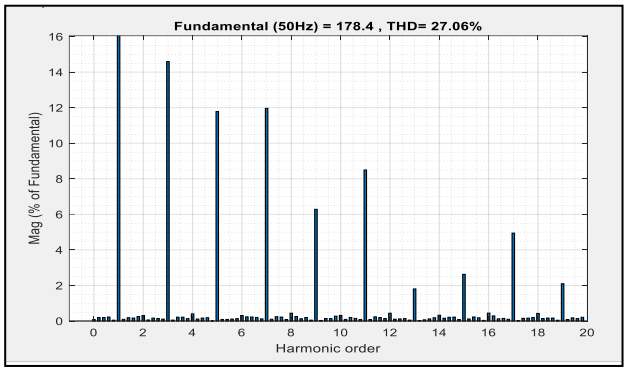

Fig 21 FFT analysis of Asymmetric grid-connected 5-level inverter with RC-load

Table 5: Comparison of result with other methodologies

Comparison of existing topologies with optimization techniques			
Reference paper	**Techniques**	**Level**	**THD (%)**
Lee, S. S., Chu, B., Idris, (2015)	GA	7-level	16.96
Chabni, F., Taleb, (2018)	PSO	7-level	18.68
	HGA	7-level	18.266
Manai, L., Armi, F., &Besbes, M. (2020)	GA	9-level	14.22
	NR	9-level	10.20
	ECSR	9-level	18.21
Mishra, P., & Mahesh, A. (2019, June)	PSO	7-level	13.68
	SCR	7-level	13.45
In this Thesis	GWO	7-level	14.5891
		5-level	27.8650

The results are also compared with four references for asymmetrical mode. These references are (Lee, S. S., Chu, B., Idris, (2015), Chabni, F., Taleb, (2018), Manai, L., Armi, F., &Besbes, M. (2020), and Mishra, P., & Mahesh, A. (2019, June)), as shown in the table (5). The reference (Lee, S. S., Chu, B., Idris, 2015) presented a seven-level asymmetrical CHB inverter. GA is used for SHE-PWM to calculate switching angles only to eliminate the 3rd & 5th harmonics of the output voltage.

The reference (Chabni, F, Taleb, 2018) presented a 7 and 5-levels CHB multilevel inverter with non-equal dc sources. Lower order harmonics for the output of voltage can be eliminated by the optimal determination of switching angles by using SHEPWM along with optimization techniques to reduce and optimize THD. The switching angles are drawn by solving a non-linear equations system using the Hybrid Genetic Algorithm HGA and compared to the PSO method.

The reference (Manai, L., Armi, F., &Besbes, M. 2020) presented a 7-level asymmetricCHBMLI. SHE based on the newton-raphson N-R algorithm is used to calculate switching angles only to eliminate lower harmonics of the output voltage. This paper mainly focused on a comparative study on performances between NR, GA, and ECSA in order to choose the most accurate one to obtain the smallest output voltage THD rate.

The reference (Mishra, P., & Mahesh, A. (2019, June)) presented a 7-levels CHBMLI with non-equal dc sources. Lower order harmonics for the output of voltage can be eliminated by the optimal determination of switching angles by using a sine cosine algorithm SCR and compared with the particle swarm optimization PSO method.

Therefore, a comparison is made with these references. Table (5) shows the comparison between the proposed algorithm, the reference ((Lee, S. S., Chu, B., Idris, (2015), Chabni, F., Taleb, (2018), Manai, L., Armi, F., &Besbes, M. (2020), and Mishra, P., & Mahesh, A. (2019, June)). From Table (5), in the first and second references, which used GA, PSO, and HGA method, the THD value for 7-level inverters was higher than the proposed GWO algorithm. In the third reference, three methods were used: GA, NR, and ECSR for a nine-level inverter, where the THD was higher in the GA method and ECSR than the proposed GWO algorithm. While the THD was lower in the NR method but this is due to the different levels; in addition to that, this method requires an appropriate initial estimation that is close to the optimum value and requires a longer calculation time. In the fourth reference, which used the PSO and SCR method, the THD value for the 7-level inverters was lower than the proposed

algorithm. However, the practical limitation associated with PSO is that it cannot modify its velocity step size to obtain fine-tuning in the local search space, which in turn results in early convergence and stagnation of local optima

VI. CONCLUSION

This research work addressed the problem of determining the minimum THD for the output waveform of CHBMLI and the effect of symmetric and asymmetric DC sources on the THD value. The GWO algorithm has been proposed to solve the problem of staircase modification techniques. The proposed algorithm can find the optimum values of the DC sources and the optimum switching angles in a simple way. They also reduce the computational burden and ensure accuracy. In MATLAB software, 7 and 5 levels of the asymmetrical and symmetrical Cascaded H-Bridge inverters are realized. On the basis of total harmonic distortion, a comparison is made between these two levels.

The simulation results showed that a 7-level CHB inverter provides the better THD value in the asymmetrical mode, whether for a resistive load or a resistive-capacitive load. Also, connecting it to the grid reduces THD. As for a 5-levels CHB inverter with resistive, it gives the THD value in the symmetrical mode better compared to the asymmetrical mode. But for a 5-level CHB inverter with a resistive–capacitive load, it gives the THD value in the asymmetrical mode better compared to the asymmetrical mode. Also, connecting it to the grid reduces THD.

From the simulation results and comparison with other techniques, the proposed algorithm has proven effective in finding the optimum switching angles and DC input sources that minimize total harmonic distortion. It is also observed from harmonic content analysis that as the number of levels increases, the THD reduces, and the output waveform becomes closer to the sinusoidal waveform.

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