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An Ultra Low Current Mismatch Charge Pump and Loop Filter in 0.18um CMOS Process for Low Spur PLL Applications

Dr. Pradeep B. Mane[#1],Ms. Shobha N. Pawar[#2]

[#1]*Principal, AISSMS's Institute of Information Technology,Savitribai Phule Pune University, Pune, India.*

https://orcid.org/0000-0002-3252-9983

[#]*2Assistant Professor, Dept. of E&TC Engineering, AISSMS's Institute of Information Technology, Savitribai Phule Pune University, Pune, India. https://orcid.org/0000-0001-8086-0761*

[1]pbmane6829@gmail.com, , [2]shobha.n.pawar@gmail.com

Abstract *- Miniaturization is the need of advanced satellite, broadcasting and telecommunication networks. Phase locked loops (PLL) are used in satellite transceivers for carrier generation. It is of great significance to design PLL on single chip with less switching time, large bandwidth and specifically minimal phase noise/reference spur. Charge pump (CP) based PLL is low cost solution for frequency synthesis it also exhibits a wide capture range without offset but the downside is it generates high reference spur owing to current mismatch. This paper discusses non-ideal effects of the charge pump including current mismatch, charge injection and charge sharing and suggests mitigation techniques for them. Paper also compares conventional charge pump architectures and suggests best suitable architecture for integrated PLL. Paper later gives design and implementation of CP and loop filter(LF) using 0.18um CMOS process with 1.8V supply voltage. DC analysis of the CP circuit gives I_{UP} and I_{DOWN} current values of 469.9 μA and 410.9 μA respectively which gives negligible current mismatch ratio of 0.13%. LF is designed with loop bandwidth of 5MHz and achieves 0.8us settling time.*

Keywords — *Charge Pump (CP), Phase Locked Loops (PLL), Current Mismatch, Charge Sharing, Clock Feedthrough*

I. INTRODUCTION

Phase Locked Loop (PLL) is widely used as frequency synthesizers in modern communication systems. PLLs are used to generate high frequency carrier signals from low frequency signals for stable, high-precision and low phase noise applications. PLL frequency synthesizer works as a local oscillator (LO) and it is used as a source of frequency reference for up conversion and down conversion in transceivers. High frequency, wide band synthesizers are greatly advantageous. PLL can be undoubtedly identified as a feedback control system which has low noise phase frequency detector (PFD), a precision charge pump (CP), a programmable divider, loop filter and voltage controlled oscillator (VCO). Control logic is used for coarse and fine tuning of VCO frequencies [1]. Figure1 explains operation of PLL, tri-state PFD compares phase and frequency difference between reference frequency signal (F_{REF}) and feedback signal (F_{BK}), when F_{REF} leads(Higher than) F_{BK}, UP signal generates which ultimately increases output current of charge pump and hence tune voltage and thus increases oscillator output frequency similarly when F_{REF} lags(Lower than) F_{BK} DOWN signal generates which ultimately decreases output current of charge pump and hence tune voltage and thus oscillator output frequency decreases.

Charge pump (CP) acts as a bipolar switched current source in PLL; ideally charge pump converts phase difference (error signal) in to current [3]. It means CP produces positive (source) and negative (sink) current pulses proportional to the frequency/phase difference between reference frequency signal and feedback signal. These current pulses then drive the loop filter, which produces variable control voltage and hence PLL output frequency varies [4].

PLL in-band phase noise can be greatly deteriorated by the charge pump noise and spurs can be generated which ultimately degrades PLL performance and transceiver sensitivity [2]. One of the major issues in integer-N PLL synthesizer design is reference spur generated by charge pump circuit which is modulated by VCO at output and will get added in to the needed signal.

It has been noticed from the literature that the sources of spur in charge pump PLL are approximately given by:

$$P_{spur} = 20\log\left[\sqrt{2}(Req * \Delta T * \Delta Icp * K_{VCO} * f_{pl}/2f_{ref}\right] \text{dBc} \quad (1)$$

Req is filter resistor, ΔT is turn-on time,ΔIcp is mismatch current in charge pump, $K_{VCO}$is the gain of VCO, f_{pl} is frequency of loop filter pole and $f_{ref}$is the PLL input reference frequency.

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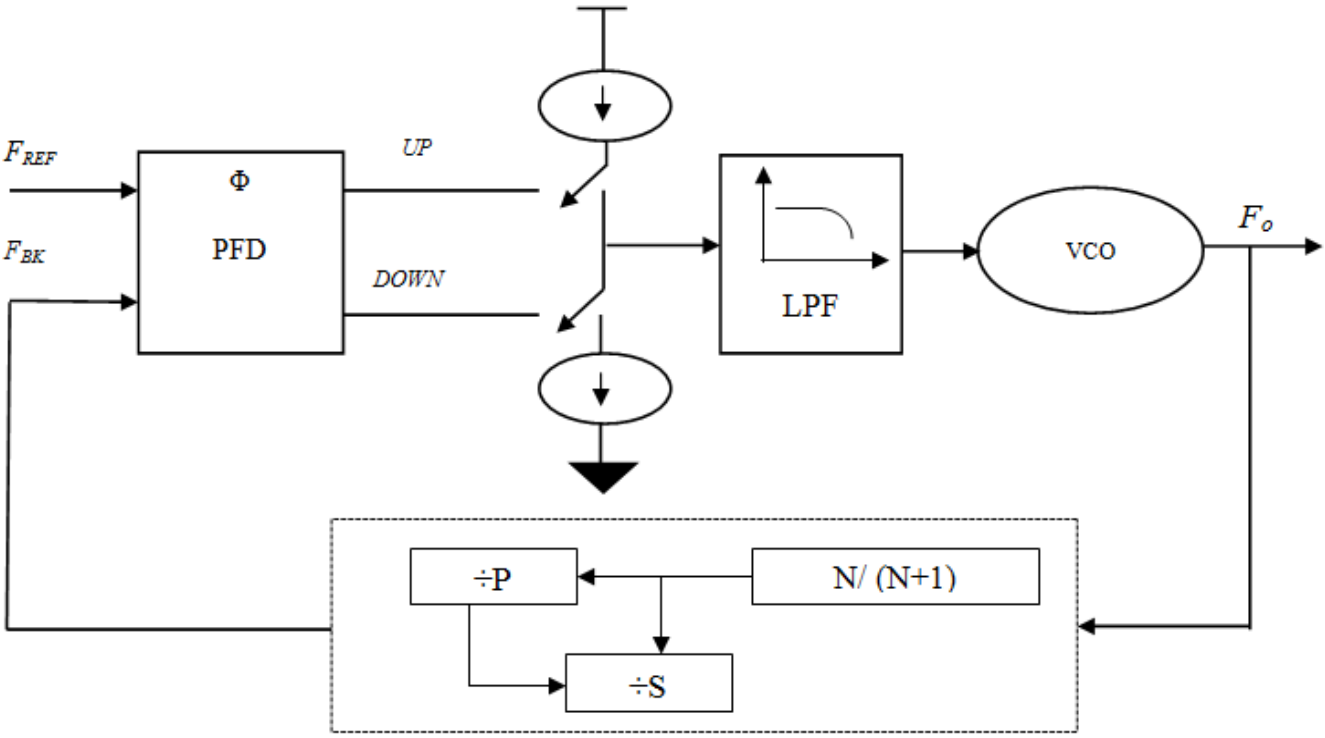

Figure1. Architecture of PLL

Req and f_{pl} affects the settling time of the loop.K_{VCO} has to be large to maintain tuning range requirement.ΔT should be passable to eliminate the dead zone. Hence to minimize P_{spur}, ΔIcp has to be small.

Co et.al [5] has proposed track and hold charge pump for improvement of reference spurs and jitter performance. In THCP single switch is used for generation of up and down current pulses which minimizes current mismatch and results in better spur performance, Ali et. al [6] proposed voltage switched charge pump over current switched charge pump because of design simplicity but downside is it generates variable pump current to mitigate this effect event driven technique has been proposed, Song et al[7] presented design and simulation of mismatch free charge pump for spur reduction using multi stage current mirror circuits, Boon et.al [8] presented design of quadrature PLL for IEEE 802.15.4 applications. He proposed charge pump design with gain boosted technique for reduction of reference spurs. In this paper charging and discharging currents are matched by adding multiple gain boosting stages in up and down sub circuits.

This paper presents mathematical modelling of the CP considering spur reduction, to design CP with an ultra low spur current matching is desirable. This paper proposes use of unity gain amplifier along with symmetrical switch design for current matching and for matching of turn ON/OFF time of the switches which in turn reduces current mismatch ratio. CP-PLL works in acquisition and tracking regions. In acquisition region PLL is locked and in tracking PLL tries to achieve the lock. Charge pump nonidealities affects PLL performance in tracking region and even though reference and feedback frequencies are same PLL fails to achieve lock. Hence it is of prime importance to study non-ideal effects of charge pump and reduction techniques for each, hence paper gives brief about non ideal effects along with mitigation techniques.

This paper is organized as follows section-I introduces PLL architecture and previous work done related to CP circuit; Selection of charge pump topologies along with associated non-ideal effects and their solutions are discussed in section-2, implementation of CP and LF is presented in section-3, Measurement results using cadence virtuoso 0.18um CMOS process are discussed in section-4 and finally the paper is concluded in section-5.

II. SELECTION OF CHARGE PUMP TOPOLOGIES

The linear, time-invariant(LTI) model of PLL shown in figure 1 supposes that the PFD and charge pump continuously generates error signal (subtraction of reference input and feedback input) and applies to VCO as a control input . But practically it only generate current pulses at rising edges of the reference signal. Conventional charge pump works in three states as given in table 1; Up, down and hold.

Table 1. Charge pump operation

State	S_1	S_2	V_{tune}
Up	ON	OFF	Increases
Hold	OFF	OFF	Lock
Down	OFF	ON	Decreases

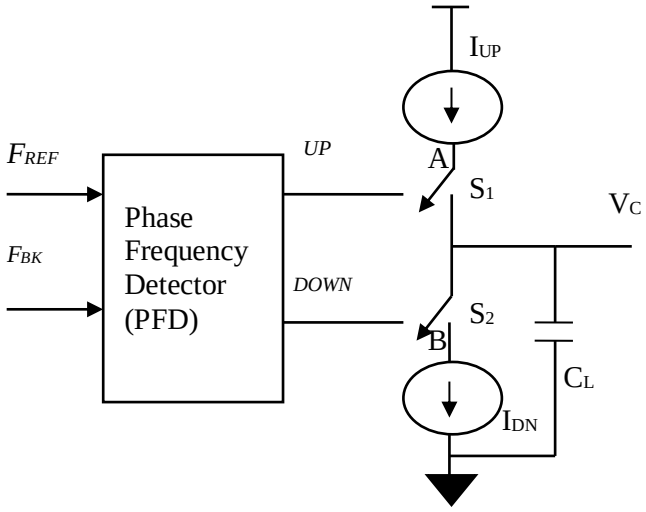

Figure 2: Conventional charge pump configuration

As shown in figure 2 when UP signal is high switch S_1 turns ON and S_2 turns OFF, I_{UP} charges load capacitor C_L and hence control voltage (V_C) increases which in turn increases PLL output frequency. Contrary when down signal is high S_2 turns ON allowing C_L to discharge through I_{DN} hence control voltage (V_C) decreases and PLL output frequency also decreases. In locked state both switches S_1 and S_2 remains OFF and hence control voltage (V_C) remains constant [9]. S_1 and S_2 are implemented using PMOS and NMOS transistors respectively.

Charge pump noise considerably decreases with increase in charge pump gain. Conventional CP with only two switches doesn't provide sufficient gain for noise removal hence it is important to explore various CP topologies. Two commonly available topologies are single ended charge pumps and differential charge pumps.

A. SINGLE ENDED CHARGE PUMP

Also known as tri-state charge pumps are popular because of low power consumption, flexibility, minimization of pads, external components and chip area. Maximum current carried by these pumps is only 4.5 mA [16,20]. As given in [26] single ended charge pumps are further classified as switch at drain, switch at gate and switch at source based on position of switch as shown in figure 3, 4 and 5.Among these three topologies switch at source topology is more attractive because of simple architecture, comparable switching time and most important is low power consumption [14, 15]. Although it provides many advantages including less chip area they have downside; These CP circuits generate high spurs, noise because of switch mismatches between NMOS and PMOS transistors hence single ended charge pumps are not preferred in communication applications.

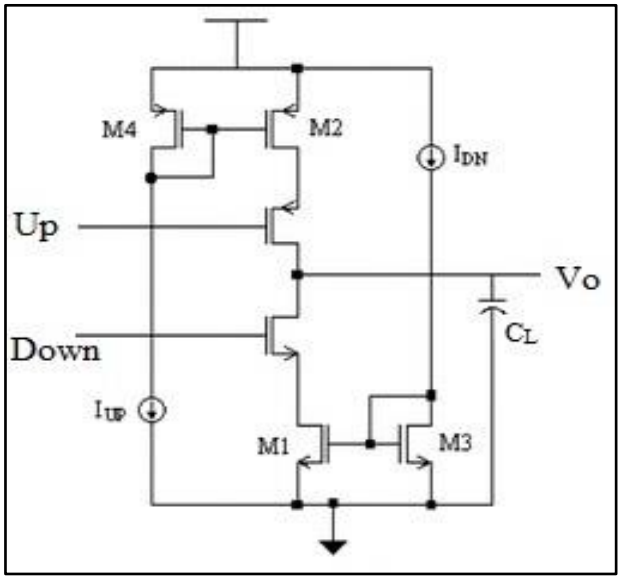

Figure 3.Switch-at–drain

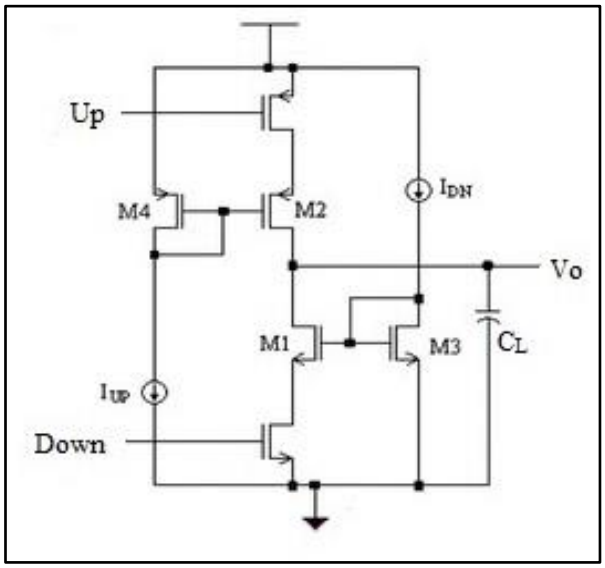

Figure 4. Switch-at-source

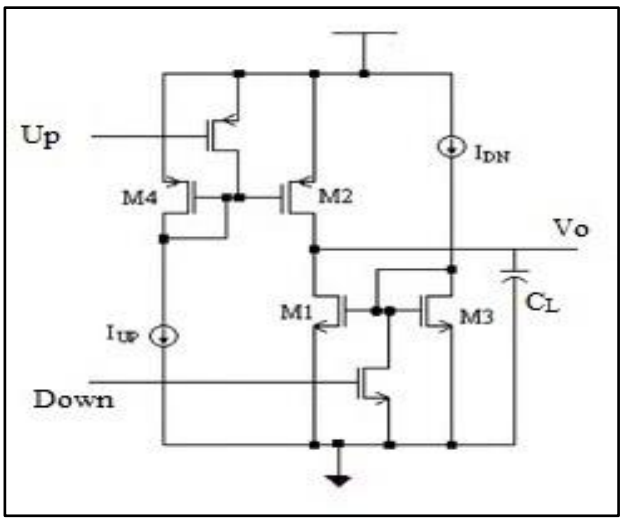

Figure 5. Switch-at-gate

B. DIFFERENTIAL CHARGE PUMP

Differentia charge pumps are often preferred over single ended charge pumps because of switch mismatches between NMOS and PMOS transistors is unaffected. Differential charge pump provides fully symmetrical operation by using switches for inverted inputs up and down. This topology doubles the range of output voltage and avoids high voltage controlled oscillators (VCO) gain. In this topology leakage current act as a common mode offset hence this architecture is less sensitive to leakage current variations. Hence differential charge pump is chosen over single ended charge pump [17, 19].In [21, 22, 23] for reduction of built in phase noise of CP stabilizing OP-AMP is suggested.

This architecture is proposed because it delivers ideally constant pump currents$\{I_{UP}, 0, I_{DN}\}$ during each transition cycle of the PFD. Moreover, this design is free from up/down current mismatch. As a result, it lowers the in band noise and reference spur. The circuit is designed with NMOS and PMOS switches with same channel length and W/L ratio of 18 . To make switches to remain in saturation under all process corners (PVT, Process, voltage and temperature) Von is set to 150mV.

It has been noticed from [16] that the implementation of CP with constant current is tremendously challenging due to non-ideal effects like current mismatch, charge sharing and clock feedthrough. Hence to design single chip PLL synthesizers it is of extreme importance to understand and remove non-ideal effects associated with CP.

C. CHARGE PUMP NON-IDEAL EFFECTS

Current Mismatch occurs because of asymmetrical operation of the MOS switches. The delay between controlled signals Up and down causes variations in charging and discharging current pulses. As given in [12] current mismatch causes variation in control voltage (V_C) and hence PLL output frequency even in locked state which is undesirable.

The commonly used techniques for removal of current mismatch in CP are to increase length of transistors or to increase output impedance. The charge pump designed in [8] has suggested use of only NMOS switches to make charging and discharging paths symmetrical. Other CP given in [17] has proposed multi stage current mirror circuit for generating source and sink currents. This paper has identified and compared various mitigation techniques considering low on chip area, speed and high frequency operation.

This work proposes use of unity gain operational amplifier for achieving same up and down currents. As shown in figure 8 this unity gain amplifier helps to keep V_A and V_B at same voltage level as that of control voltage even when both S_1 and S_2 will turn ON. OP-AMP tracks pump currents and allows compensation in current mismatch.

Charge sharing is the commonly observed effect in CP circuits. As given in figure 2 in hold state of CP when both switches are OFF voltage at node A is V_{DD} and voltage at node B is zero, and it can be observed that the V_C is floating. Due to non-ideal narrow pulses at Up signal for short time period both transistors are simultaneously ON which will cause V_A to decrease and V_B to increase because of charge sharing between load capacitor C_L, PMOS capacitor and NMOS capacitor; this will deviate control voltage as shown in figure 6 and hence control voltage varies compared to ideal output shown in figure 7.

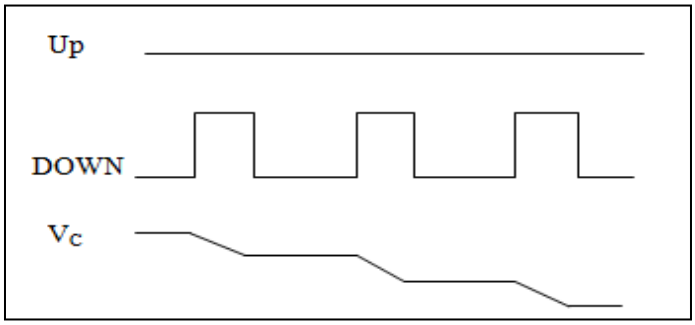

Figure 6. Charge pump ideal output

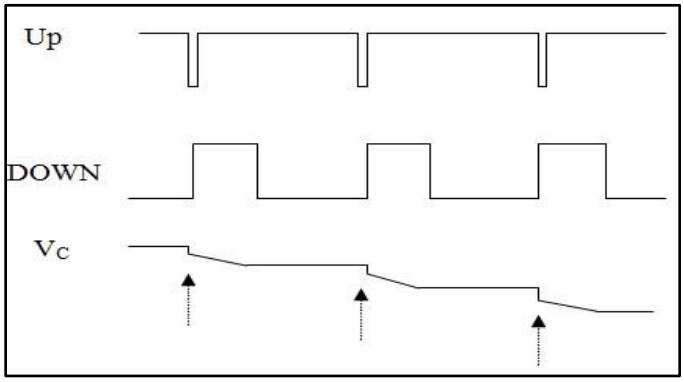

Figure 7. Effect of charge sharing on CP output

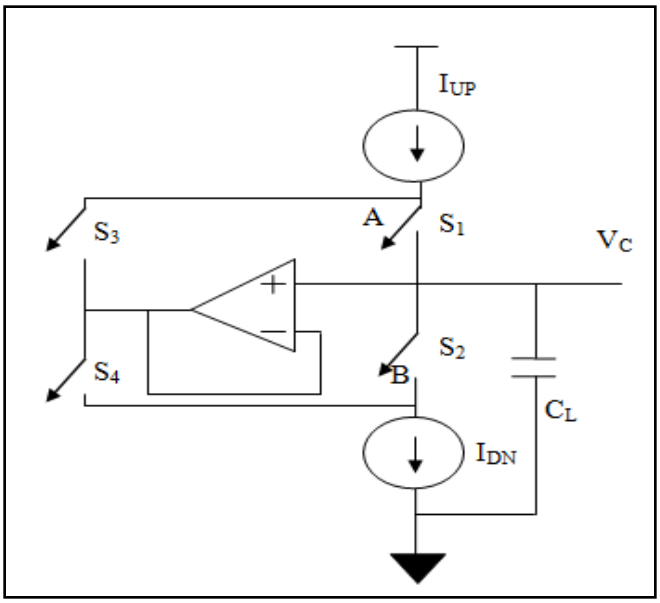

Figure 8. Proposed charge pump with unity gain amplifier

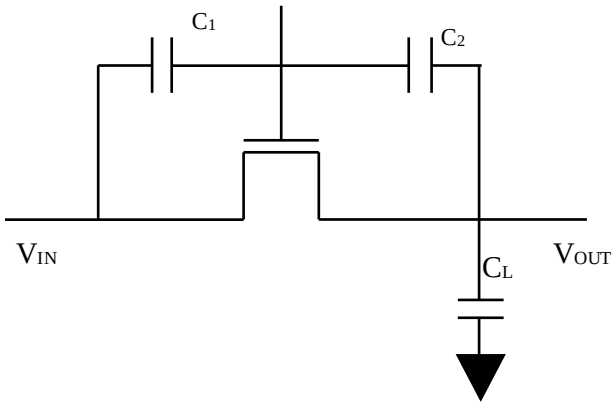

Figure 9. Charge injection in MOSFET

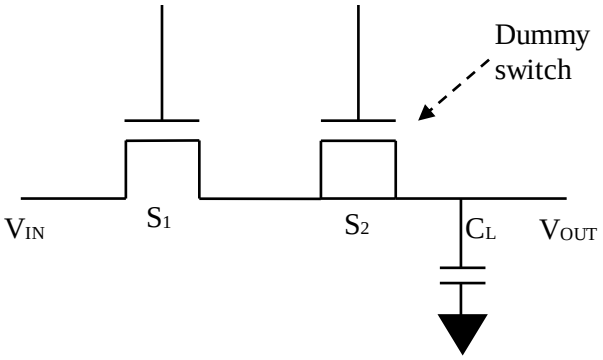

Figure 10. Elimination of charge injection in by using dummy switch

Another effect observed in CP is injection of charges. It is noticed from [4] that this effect occurs because of coupling capacitance from gate of MOSFET to drain and source of MOSFET. In CP circuit MOS transistors are used as switches as shown in figure 9. When switches are ON gate terminal of MOSFET holds charges. Once switch turns OFF charges under gate terminal injected to drain / source terminal of MOSFET. When switch is connected to output terminal like S_1/S_2 as given in figure 8, it causes ripples in output because of stored charge.

Classical mitigation approaches include placement of switch away from output node, placement of dummy transistor having size half as compared to actual switch transistor as shown in figure 10 in series with MOS switch with inverting control voltage and drain and source terminals are shorted. When first switch S1 turns OFF half of its charge is injected in to S2 but this charge is matched with the charge injected by S2 and hence total charge injection is cancelled out. When S2 turns OFF it also injects charge but as drain and source terminals are shorted and S1 is ON total charge will be injected on to low impedance voltage source which is charging C_L and hence charge at C_L will remain unchanged. Design proposed in [4] suggests replacement of NMOS/PMOS switches with transmission gates. This paper suggests placement of switch near source (Near V_{DD} or Ground) for removal of charge injection.

III. IMPLEMENTATION OF CHARGE PUMP

The proposed design for the charge pump is shown in figure 8. An Op-amp with negative feedback is proposed to maintain constant gate voltage of the MOSFET to achieve constant current flow which is independent of drain to source voltage. The pulse width of output current (I_{CP}) generated by CP is directly proportional to the phase error (θ_e) generated by PFD. In ideal CP circuit up (charge) and down (discharge) currents are same, that is $I_{CP} = I_{UP} = I_{DOWN}$. So ideally in locked state VCO control voltage (V_C) varies because of noise only, practically non-ideal effects of CP cause periodic ripples on V_C. As variations on V_C are minimal in locked state, VCO Output is expressed in [24] as:

$$V_{out}(t) = V_0 \cos\left[\omega_0 t + K_{VCO}\int_0^t V_c(\tau)d\tau + \theta_0\right] \quad (2)$$

In case of narrow band system the maximum phase deviation ($\Delta\Phi$) is less than $\pi/2$.

$$\Delta\emptyset = \left|K_{VCO}\int_0^t V_c(\tau)d\tau\right|_{max} \quad (3)$$

Initially when phase θ_0 is zero (2) becomes:

$$V_{out}(t) = V_0 \cos\left[\omega_0 t + K_{VCO}\int_0^t V_c(\tau)d\tau\right]$$

$$V_{out}(t) = V_0 \cos(\omega_0 t)cos\left[K_{VCO}\int_0^t V_c(\tau)d\tau\right] -$$
$$V_0 \sin(\omega_0 t)\sin\left[K_{VCO}\int_0^t V_c(\tau)d\tau\right] \quad (4)$$

$$V_{out}(t) \approx V_0 \cos(\omega_0 t) - V_0 K_{VCO} \int_0^t V_c(\tau) d\tau . \sin(\omega_0 t)$$

Let, $V_c(t)$ be a sinusoidal signal with reference input:
$V_c(t) = A_m \cos \omega_{ref} t$
Equation (3) reduces to the following:

$$\Delta\emptyset = \left| K_{VCO} \int_0^t A_m \cos(\omega_{ref}\tau)\, d\tau \right|_{max} = \frac{K_{VCO} A_m}{\omega_{ref}} \quad (5)$$

Equation (4) reduces to the following:

$$V_{out}(t) = V_0 \left[\cos \omega_0 t - \frac{\Delta\emptyset}{2} \cos(\omega_0 - \omega_{ref}) t + \frac{\Delta\emptyset}{2} \cos(\omega_0 + \omega_{ref}) t \right] \quad (6)$$

Equation (6) indicates reference spurs are present at $\omega_0 + \omega_{ref}$ and $\omega_0 - \omega_{ref}$ with associated power are given as:

$$P_r = 20 \log \left(\frac{K_{VCO} A_m}{2\omega_{ref}} \right) dBc \quad (7)$$

In a PLL, the output up/down of PFD is a narrow pulses in each phase comparison period (T_{ref}). *R*andom part of CP output (I_{out}) get generated because of noises in the PLL, the mismatches in the charge pump generate deterministic and periodic part of I_{out}. As PFD and CP gives discrete time behavior the spectrum folding because of sampling effect exists. The spectrum of discrete time phase error (θ_{e_dt}) with reference frequency ω_{ref} is written as:

$$\theta_{e\_dt}(\omega) = \sum_{n=-\infty}^{\infty} \theta_e (\omega + n\omega_{ref}) \quad (8)$$

This effect produces phase noise at offset frequencies of $n\omega_{ref}$, $n = \pm 1, \pm 2, ...$, this phase noise at offset frequencies produces reference spur. Based on (8) open loop noise transfer function becomes:

$$H_{ol}\lfloor j(\omega + \omega\_ref) \rfloor \approx H_{ol}(j\omega_{ref}) \quad (9)$$

The upper bond of the reference spur because of numerous noise sources considering PLL output *rms* phase error in *rad* as $\Delta\emptyset_{rms}$ must be composed as:

$$P_r < 20 \log(\Delta\emptyset_{rms}) + 20 log\left(|H_{ol}(j\omega_{ref})|\right) \quad (10)$$

Reference spur touches this upper bond only when noise from VCO and loop filter is dominating the $\Delta\emptyset_{rms}$. It is observed that when $\Delta\emptyset_{rms} = \pi/180 = 1°$, equation (10) becomes nearly *-35dB*. Ideally $\omega_Z << \omega_{ref}$, where ω_Z the zero in loop filter for stability open loop transfer function is can be written as:

$$\left|Z_{If}(j\omega_{ref})\right| \approx R_1 . \frac{C_1}{C_1 + C_2 + C_3} \frac{1}{\sqrt{1 + (\omega_{ref}/\omega_{p2})^2}} \frac{1}{\sqrt{1 + (\omega_{ref}/\omega_{p3})^2}} \quad (11)$$

$$\left|H_{ol}(j\omega_{ref})\right| \approx \frac{\omega_c}{\omega_{ref}} \frac{1}{\sqrt{1 + (\omega_{ref}/\omega_{p2})^2}} \frac{1}{\sqrt{1 + (\omega_{ref}/\omega_{p3})^2}} \quad (12)$$

ω_{p2}, ω_{p3} are second and third poles respectively. Periodic and deterministic ripples in VCO control voltage get produced because of charge pump nonidealities. The CP output current I_{out} is a periodic signal with period T_{ref} can be disintegrated into discrete Fourier series as [25]:

$$I_{out}(t) = \sum_{k=1}^{\infty} c_k e^{jk\omega_{ref} t} \quad (13)$$

The VCO control voltage is

$$V_c(s) = I_{out}(s) . Z_{lf}(s) \quad (14)$$

Hence the reference spur level in dBc becomes:

$$P_r = 20 \log \frac{K_{vco} |c_1| \cdot |Z_{lf}(j\omega_{ref})|}{2\omega_{ref}}$$

$$= 20 \log \left[N\pi \cdot \frac{|c_1|}{I_{cp}} \right] + 20 log\left(|H_{ol}(j\omega_{ref})|\right) \quad (15)$$

The pulse width of current I_{cp} to compensate the leakage current I_{leak} can be written as:

$$\tau = \frac{I_{leak}}{I_{cp}} T_{ref} \quad (16)$$

The coefficients of Fourier series in (13) are:

$$C_k = \frac{1}{T_{ref}} \left[\int_0^c I_{cp}\, e^{-jk\omega_{ref} t} dt - \int_0^{T_{ref}} I_{leak} e^{-jk\omega_{ref} t}\, dt \right]$$

$$= I_{leak} \frac{\sin(k\omega_{ref}\tau/2)}{k\omega_{ref}\tau/2} e^{-jk\omega_{ref}\tau/2} \quad (17)$$

From (16) it can be stated that $\tau << T_{ref}$ when $I_{leak} << I_{cp}$. The coefficient corresponding to the reference spur becomes:

$$|c_1| \approx I_{leak} \quad (18)$$

The mismatch current between up/down current can be calculated as:

$$\Delta I_{cp} = I_{up} - I_{dn} \quad (19)$$

Pulse width of CP current to compensate this current mismatch is obtained as:

$$\tau = \frac{\Delta I_{cp}}{I_{cp}} t_{on} \quad (20)$$

Generally $\Delta I_{cp} << I_{cp}$ and $t_{on} << T_{ref}$ hence $\tau << T_{on}$. The Fourier of CP current as given by (13) are:

$$C_k = \frac{1}{T_{ref}} \left[\int_0^{I_{on}} \Delta I_{cp}\, e^{-jk\omega_{ref} t} dt - \int_0^{I_{on}+\tau} I_{cp} e^{-jk\omega_{ref} t}\, dt \right]$$

$$= \Delta I_{cp} \frac{t_{on}}{T_{ref}} \frac{\sin(k\omega_{ref} t_{on}/2)}{k\omega_{ref} t_{on}/2} e^{-jk\omega_{ref} t_{on}/2} -$$

$$I_{cp} \frac{\tau}{T_{ref}} \frac{\sin(k\omega_{ref}\tau/2)}{k\omega_{ref}\tau/2} e^{-jk\omega_{ref}(\tau/2 + t_{on})} \quad (21)$$

The coefficient of reference spur due to current mismatch is:

$$|c_1| \approx \pi \Delta I_{cp} \left(\frac{t_{on}}{T_{ref}} \right)^2 \quad (22)$$

Mismatch current is due to delay mismatch between falling edges of up and down pulses or turn-off time mismatch between two switches[32]. This generates both positive and negative current pulse I_{cp} of equal width with pulse width τ, and the Fourier coefficients are:

$$C_k = \frac{1}{T_{ref}}\left[\int_0^{\tau} I_{cp}\, e^{-jk\omega_{ref}t}\, dt - \int_{t_{on}}^{t_{on}+\tau} I_{cp} e^{-jk\omega_{ref}t}\, dt\right]$$
$$= j \cdot 2I_{cp}\frac{\tau}{T_{ref}}\frac{\sin(k\omega_{ref}\tau/2)}{k\omega_{ref}\tau/2}\sin\left(\frac{k\omega_{ref}t_{on}}{2}\right)e^{-jk\omega_{ref}(\tau+t_{on})/2} \quad (23)$$

Thus the coefficient for the reference spur due to the timing mismatch is

$$|c_1| \approx 2\pi I_{cp}\frac{\tau}{T_{ref}} \cdot \frac{t_{on}}{T_{ref}} \quad (24)$$

In the CP circuit designed in this paper T_{ref} is chosen as 10ns, $t_{on} = 1ns$, $\tau = 0.1ns$ and N=100 then as per (15) spur level is -34dB.

Besides the three types of mismatches discussed in section II, periodic operation of the PFD, CP and loop filter in a PLL with on chip loop filter and VCO periodic supply noise and substrate noise also partially contribute to the reference spur as given in [24].

A Ku band (12GHz to 18GHz) satellite transponder application is considered in this work which need to be designed with minimal reference spur. As given in [5] reference spur is directly proportional to current mismatch.

$$Reference\ spur \propto \Delta I_{cp}\left(\frac{F_{BW}}{F_{ref}}\right)^2 \quad (25)$$

Where ΔI_{cp} is the mismatch current of the CP, F_{BW} is the PLL bandwidth and F_{ref} is the input reference frequency. Based on the above considerations, a second order RC loop filter is proposed for the spur reduction. Locking time or switching time of the synthesizer circuit is decided by the bandwidth of the LF. As per mathematical analysis given in [24] for stability concerns loop bandwidth is suggested to be less than 1/10th of the reference frequency. Noise transfer characteristics of PLL get affected because of loop bandwidth. In [25] equation for loop bandwidth is derived and suggested as the optimal loop bandwidth is where the high-pass VCO noise contribution is same as low pass noise contribution from reference signal, PFD and charge pump. The PLL settling time depends on loop filter's cutoff frequency which is given as:

$$t_s = \frac{4}{f_c} \quad (26)$$

t_s: Settling time

f_c=LPF cutoff frequency.

In this work 2nd order LPF is proposed as shown in figure 16. It was decided to use cutoff frequency of 5MHz to suppress low frequency noise with reference frequency of 100MHz for achieving 100MHz resolution in PLL output.

IV. MEASUREMENT RESULTS

Implementation of double ended charge pump with operational amplifier (Schematic given in figure 15) using 0.18um, 1.8V CMOS process is shown in figure 11. Up and down outputs of PFD along with their inverted versions are used for removal of charge sharing and current mismatch by matching switch ON/OFF times. Schematic for testing of designed CP is given in figure 12. Figure 13 and 14 shows simulation results obtained using spectre simulator, output of charge pump for up state is presented in figure 13; which shows increase in control voltage with increase in phase/ frequency difference between reference and feedback signal.

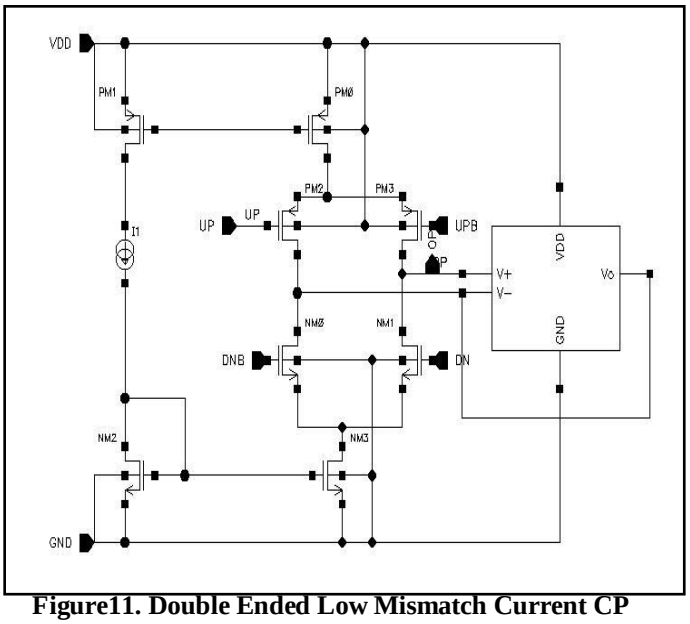

Figure11. Double Ended Low Mismatch Current CP Schematic

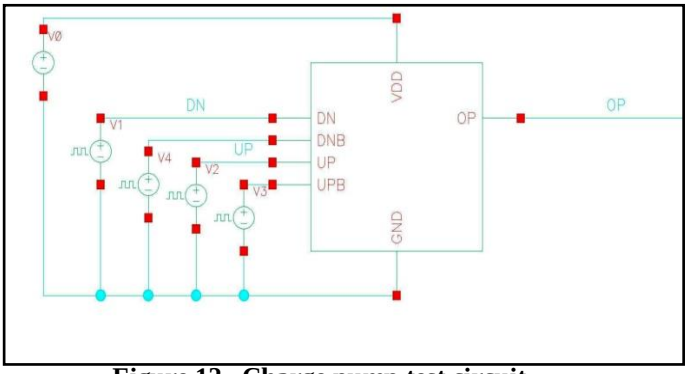

Figure 12. Charge pump test circuit

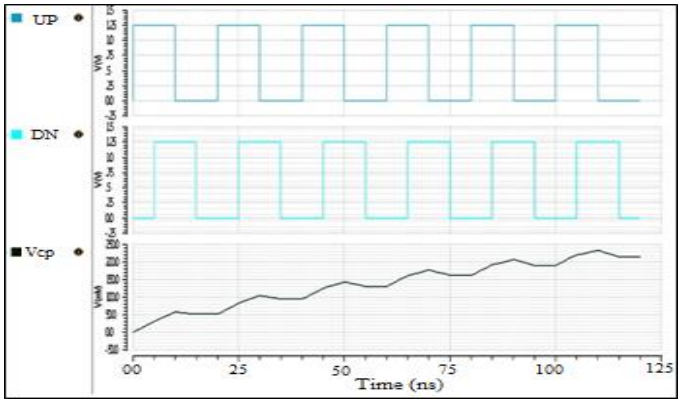

Figure 13. CP output waveform(Tracking mode)

Locked state is shown in figure 14 where reference and feedback signals are in phase and hence control voltage remains constant.

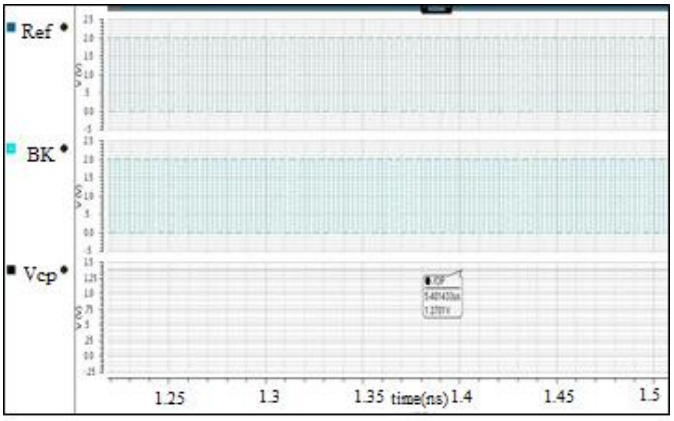

Figure 14. CP output waveform (Locked state)

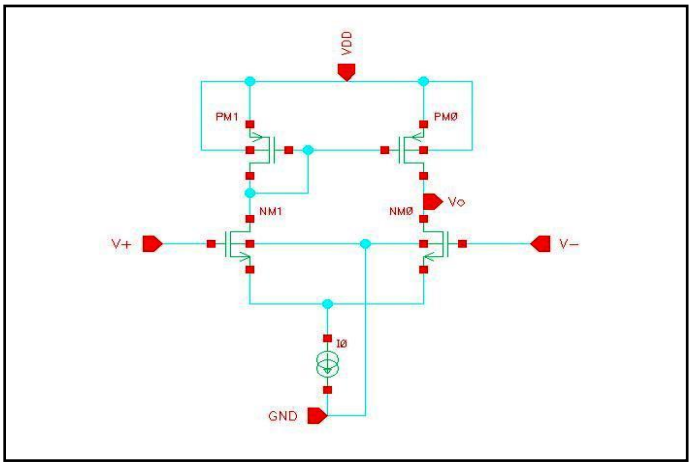

Figure 15. Op-Amp for current mismatch removal

$$I_{mismatch} = 2 * \frac{(I_{UP} - I_{DOWN})}{(I_{UP} + I_{DOWN})} \quad (26)$$

Eq. (26) defines current mismatch ratio. DC analysis of the circuit gives I_{UP} and I_{DOWN} current values of 469.9 µA and 410.9 µA respectively. From DC analysis and eq. (26) current mismatch ratio is measured to be less than 0.13%.

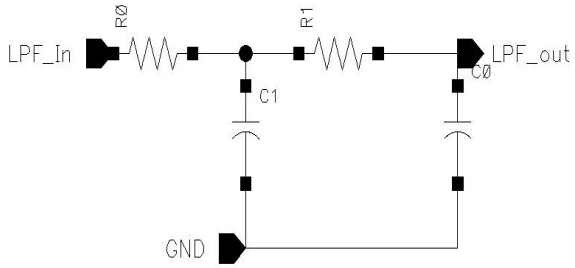

Figure 16. Schematic of the 2nd order RC LPF

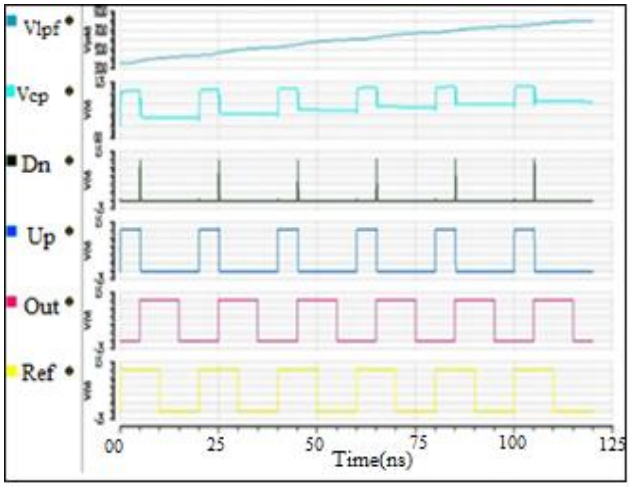

Figure 17. LPF transient analysis

Comparisons with conventional charge pump circuits:
DC analysis proves that this implementation is free from up/down current mismatch and as a result it lessens in band noise and spur level. The reason is use of op-amp for removal of charge sharing and current mismatch. Another reason is careful selection of W/L ratios of CMOS transistors to match ON/OFF time of switches so as to get same up and down current.

Table 2: CP performance comparison

Parameter	[4]	[27]	[28]	[29]	This work
Process/ Technology	0.18um	90nm	0.13um	0.18um	0.18um
Supply voltage	1.8V	1.8V	1.3V	1V	1.8V
Output Frequency	4 GHz	2.5GHz	2.4 GHz	2.44 GHz	12GHz-18GHz
CP type	Differential	Cascode	Differential	Open loop	Differential
No. of transistors used	12	20	11	14	12
CP output current	10uA	40uA	50uA	100uA	469uA

CP Performance comparison is shown in table 2 and table 3. Compared with other state-of-the-art CP designs this work uses only 12 transistors for PLL implementation which occupies very small chip area and hence this CP can be used in integrated single chip PLL. Current mismatch ratio is comparable with the existing work with the implemented circuit achieves better dynamic range of 0.3-0.9V. Hence the

measurement results shows that the proposed CP circuit along with loop filter can be used in wideband, high frequency PLL frequency synthesizer with reduced mismatch current for spur reduction.

Table 3: CP performance comparison for dynamic range and mismatch current

Parameter	[4]	[30]	[31]	This work
Process/ Technology	0.18um	0.18um	0.18um	0.18um
Current Mismatch	0.01%	0.03%	0.44%	0.13%
Dynamic range	0.15-1.6V	0.4-1.1V	0.06-0.85V	0.3-0.9V
Output current	10uA	34.7uA	40uA	469uA

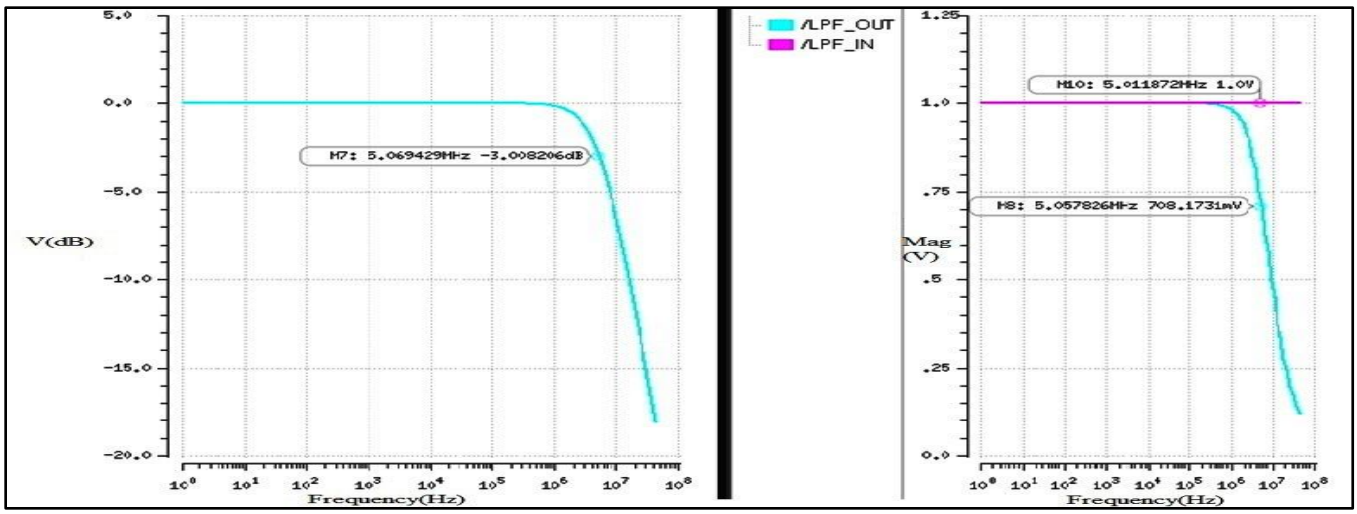

Figure 18:AC analysis of the LPF

V. CONCLUSIONS

This paper presents implementation of charge pump and loop filter for wideband, fully integrated Ku band (12GHz to 18GHz) PLL frequency synthesizer. Implementation of charge pump and second order loop filter using 0.18um CMOS process with 1.8V power supply is presented. Paper also examines non-ideal effects present in charge pump which includes current mismatch, charge sharing and clock feedthrough and suggests mitigation techniques for them. Paper then presents mathematical modeling of charge pump for reference spur reduction by current matching. Measurement results shows up and down currents of 469.9 µA and 410.9 µA respectively with current mismatch ratio of 0.13%. Loop filter is designed with cutoff frequency of 5 MHz which gives PLL settling time of 0.8µs only which helps PLL to achieve lock faster. Measurement results shows the implemented circuit uses only 12 transistors hence occupies minimal chip area and it is suitable for single chip PLL design.

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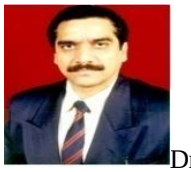

Dr. Pradeep B. Mane received his BE (E&TC) and ME (E&TC) degree from Government College of Engineering Pune,India and P.hD from Bharati Vidyapeeth University,Pune. He worked in Philips India ltd. for 3 years, 15 years in Bharati Vidyapeeth COE Pune and currently working as a Principal in AISSMS's Institute of Information Technology, Pune affiliated to Savitribai Phule Pune University. He was a member of the BOS for Electronics faculty in Bharati Vidyapith University and Savitribai Phule Pune University. He has co-authored 6 books for engineering courses with Wiley and Technova publications in the field of Radio and TV engineering and Computer networks. He has published 50 papers in national, international conferences and seminars. He has 47 publications in international journal. He is a regular reviewer for Springer Wireless Personal Communication journal. His area of interest is wired, wireless communication and computer networks. He was CO-PI for ISRO-UOP research grant. He is a fellow of IEI, IETE and member of IEEE, ISA, IJERIA and ISTE. He has received national awards for Best Engineering College Principal for year 2017 from Bharatiya Vidya Bhavan(ISTE) and Computer Society of India (CSI). He is recognized as a Ph.D Guide of Savitribai Phule Pune University and Bharati Vidyapeeth deemed university in Electronics engineering. Four students have completed Ph.D. under his guidance and eight students are currently working under his guidance.

Ms. Shobha N. Pawar received her BE (E&TC) degree from University of Pune, Maharashtra, India in 2007 and ME (E&TC - Microwaves) from Savitribai Phule Pune University, Pune in 2012. Currently pursuing Ph.D from AISSMS's Institute of Information Technology affiliated to Savitribai Phule Pune University, Pune. She has teaching experience of 12 years and research experience of 1.5 years; currently she is associated with AISSMS Institute of Information Technology, Pune as an Assistant Professor in Electronics and Telecommunication Engineering. She has published papers in 18 international journals and presented papers in 6 international conferences. She was principal investigator of ISRO-UOP sponsored research project. She is a life member of ISTE, IETE and member of IEEE.