Green and Sustainable FPGA Based Counter For IOT Based Processor

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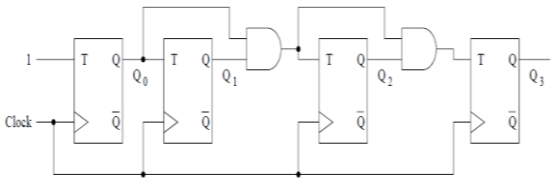
Abstract *--- In the era of Industry 4.0, where billions of devices are connected together with the help of Artificial Intelligence, Internet of Things (IOT), Internet of Everything(IOE) and many more technologies which processes lots of data for getting the user equipped with information as these technologies are great advantage of the human beings but for the efficient use of energy for our digital devices that would be harmless for our environment and hence we opt for green computing. Therefore, in our work we have design green FPGA based counter which proves to be the heart of digital devices and hence tried to reduce the energy consumption of digital devices. So, design 64-bit FPGA based counter we have worked with Virtex-7 series family in combination with Verilog, HDL and Xilinx ISE Simulator. here, we have worked with 15 series IO Standards that are LVCMOS15, SSTL15, and LVDCI_15. we have calculated the total power consumption at constant voltage 0.970. In our work, we have found significant power reduction FPGA based 64-bit counter to 54.79%by applying LVCMOS15 IO Standard at volt 0.970.*

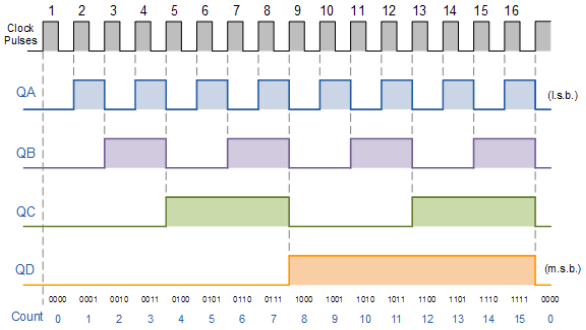
Keywords — *AI , FPGA, IOT, Industry 4.0,counter , HDL, Verilog, Xilinx ISE Simulator*.

I. INTRODUCTION

This As we know that IoT is transforming the world today having the fastest growing workloads for data centers, this IoT workload is accelerated by FPGA. FPGA (Field Programmable Gate Array) is an Integrated Circuit that can be reprogrammed in the field after manufacturing. In our experiment, for designing FPGA based counter we have used Verilog language which is the hardware Description Language. The fabrication of different types of gates forming Sequential logic device is counter. It can be made using T Flip-flop or D Flip-flop connected in cascade. We can store the occurrences of particular events in counter. Here we have used 5G frequency range (30 GHz to 70 GHz) for making our device more technically sound and more user friendly.

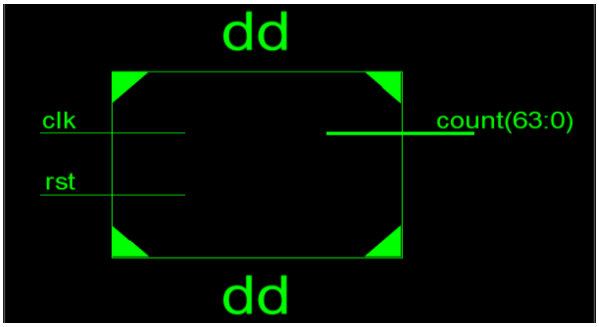


In figure 1 we have shown the 4-bit synchronous up counter.



In figure 2 we have shown the waveform of 4-bit synchronous up counter.

In this paper, we have design FPGA based 64-bit asynchronous up counter.



Top Level of schematic of 64-bit Counter is shown in figure

II. METHODOLOGY

A. FPGA METHODOLOGY:

The Xilinx FPGA device methodology in figure 4 allows to achieve the optimality of device and design characteristics, such as:

- ✓ Routing Utilization
- ✓ Design Performance
- ✓ Power Consumption

This methodology also allows to achieve efficiencies in:

- ✓ Software runtime
- ✓ Debugging capability
- ✓ Portability

During the design of the component first we used specification that has Verilog RTL coding . In second step, functional simulation contains technology logic synthesis, mapping, placement. At last we have done Timing Simulation through routing, Bitstream generation and finally downloading to FPGA.

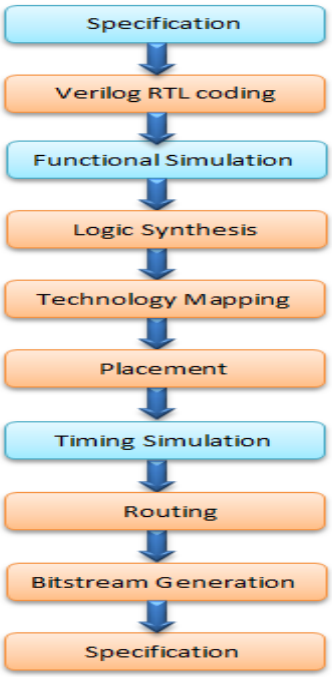


FIGURE 4- FPGA METHODOLOGY

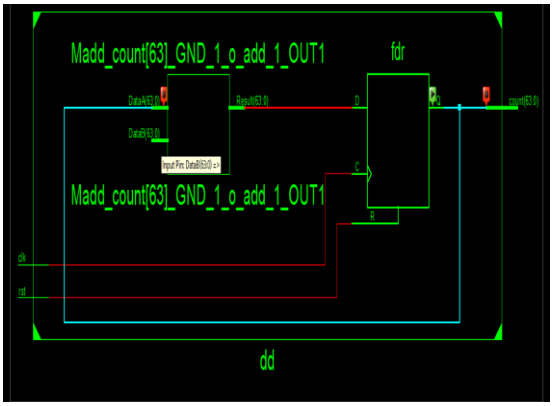


Figure 5- RTL schematic of 64-bit Counter

Figure 5 shows the Behavioural simulation process which takes place accompanied by post-Synthesis simulation and post implementation Simulation. After that in last design can go for the fabrication in to the manufacturer company.

III. RESULTS AND DISCUSSION

Table 1: Calculating power by applying LVCMOS 15 at voltage 0.970 Volt.

Frequency	Clock	Signal	IO	Leakage	Total
30 GHz	0.373	0.037	1.254	0.177	1.845
40 GHz	0.497	0.049	1.672	0.181	2.404
50 GHz	0.621	0.061	2.090	0.184	2.963
60 GHz	0.746	0.074	2.509	0.187	3.522
70 GHz	0.870	0.086	2.927	0.191	4.081

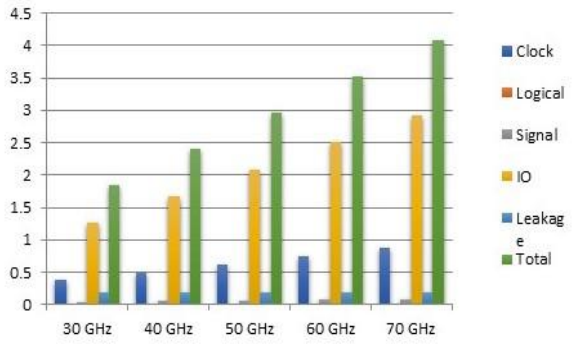


Figure 6- shows the chart of calculating power at voltage 0.970 by applying LVCMOS 15

In the table 1 and figure 6 calculating total power consumption by Appling IO standard LVCMOS 15 at voltage 0.970 Volt. In this experiment we have taken the frequency from 30GHz to 70GHz. During the work we have found that total power consumption is directly proportional to frequency. Therefore, at 30 GHz we found 1.845-watt minimum power consumption of device. The reduction of the frequency from 70 GHz to 30GHz then total power consumption is reduced by 54.79%.

Table 2 Calculating power by Appling SSTL15 at voltage 0.970 Volt

Frequency	Clock	Signal	IO	Leakage	Total
30 GHz	0.341	0.063	0.424	0.173	1.004
40 GHz	0.455	0.084	0.522	0.174	1.240
50 GHz	0.568	0.106	0.621	0.174	1.475
60 GHz	0.682	0.127	0.719	0.177	1.711
70 GHz	0.795	0.148	0.817	0.178	1.946

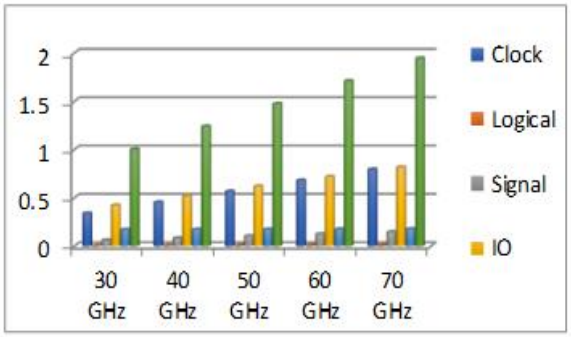


Figure 7 Chart of calculating power at voltage 0.970 by applying SSTL 15

In table 2 and figure 7 During the experiment calculated total power consumption is dominant by IO power by applying SSTL15. At the 70 GHz. Then, total power -consumption is 3.537. In SSTL 15 when we fluctuate the frequency from 70GHz to

30 GHz we reduced the total power consumption by 48.41%.

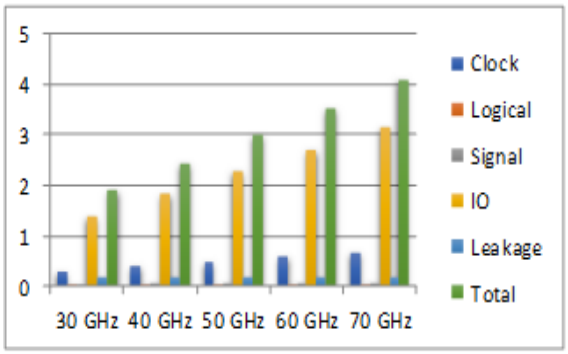


Figure 8- shows the chart of calculating power by applying LVDCI_15 at voltage 0.970

We have calculated total power In table 3 and figure 8 by applying LVDCI 15 IO standard at the same voltage. At 30 GHz we calculate total power consumption 1.891 Watt but the power reduction from 70GHz to 30GHz is 53.76 %.

Table 3 Calculating power by Appling LVDCI_15 at voltage 0.970 Volt

Frequency	Clock	Signal	IO	Leakage	Total
30 GHz	0.287	0.004	0.032	0.178	1.891
40 GHz	0.382	0.005	0.042	0.181	2.441
50 GHz	0.478	0.006	0.053	0.184	2.990
60 GHz	0.574	0.007	0.064	0.188	3.540
70 GHz	0.669	0.008	0.074	0.191	4.090

RELATED WORK

Energy Efficient ALU Design Based On Voltage Scaling [1]. Reprogrammable hardware for educational purposes [2]. HSTL IO Standards Based Processor Specific Green Counter [3].Capacitance Scaling Based Low Power Comparator Design on 28nm FPGA [4]. SSTL Based Energy Efficient FIFO Design for High Performance Processor of Portable Devices [5].Energy Efficient CRC Design for Processor of Workstation, and Server using LVCMOS [6]. Test of RAM-Based FPGA: Methodology and Application to the Interconnect [7]. Block RAM-based architecture for real-time reconfiguration using Xilinx R FPGAs [8].Techniques and Algorithms for Fault Grading of FPGA Interconnect Test Configuration[9] Techniques and Algorithms for Fault Grading of FPGA Interconnect Test Configuration [10]. 8-bit AES FPGA Implementation using Block RAM [11].High Performance FIFO Design for Processor through Voltage Scaling Technique[12].A new phase-shifted full bridge converter with voltage-doubler-type rectifier for high-efficiency PDP sustaining power modules[13].Industrial Artificial Intelligence for Industry 4.0-based Manufacturing Systems Towards In-Transit Analytics for Industry 4.0[14].

IV. CONCLUSIONS

In our experiment we have designed AI efficient and sustainable FPGA based counter and calculated the total power consumption of the device. We have Calculated total power by considering clock, signal, IO and Leakage power as our parameter. Here, our component is efficient for 5G Frequency range by applying the constant voltage of 0.970 on the IO Standards of 15 series. Working with SSTL15,we reduce the power consumption by 48.41% , by using LVDCI_15 we get 53.76% power reduction and the most significant and efficient result is 54.79% by using LVCMOS 15 IO Standard.

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