Impact of Channel Length Variation on Short Channel Effect Parameters of Two Different GAA Nanowire Transistor Structure

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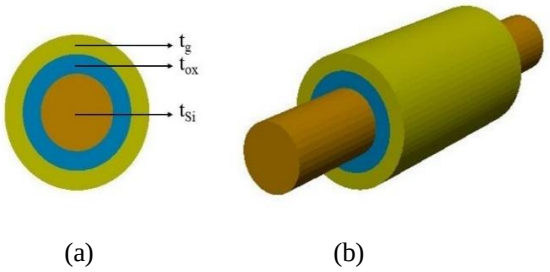
Abstract *- Two different structures of junctionless nanowire transistor have been introduced in this work and their performance has been analyzed. Previously proposed two structures: rectangular GAA junctionless nanowire transistor, cylindrical GAA nanowire transistor are analyzed using the CVT model approach by TCAD Silvaco Atlas. Short channel effect parameters like Drain induced barrier lowering (DIBL), Threshold Voltage Roll off (TVRO), Subthreshold Swing (SS), on state and off state current ratio (I_{on}/I_{off}) for the mentioned structures of n-channel JLNW transistor are analyzed. Simulation has been executed by varying channel length (L_g) and oxide thickness (T_{ox}) to observe the electrical transport characteristics. In quintessence, JLRG is better in the threshold voltage roll off parameter over channel length alteration. Although JLCG is better candidate in other SCE parameters like I_{on}/I_{off} ratio, SS and DIBL than JLRG.*

Keywords *- Cylindrical gate structure, rectangular gate structure, CVT, short channel effects, DIBL, I_{on}/I_{off} Ratio, threshold voltage, Silvaco TCAD*

I. INTRODUCTION

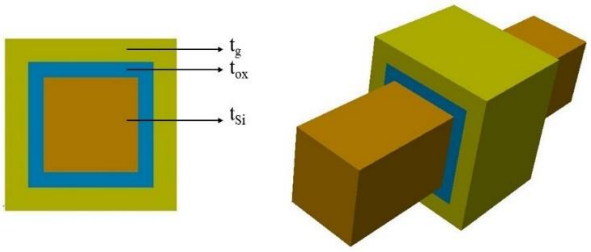
Over the past decades, conventional MOSFET has been scaled down in size. The smaller size of MOSFET is desirable for various reasons. The primary reason is to make transistors smaller in size to integrate the more and more transistor in a given chip area to increase the device functionality.MOSFETs channel lengths were once several micro-meters, but modern integrated circuits are incorporating MOSFETs withchannel lengths of nanometers.Due to the downscaling of MOSFETs, short channel effects (SCEs) have become a huge problem for nanometer technology.In conventional MOSFETs, the channel potential is controlled by gate electrode only but the MOSFET with short channel length, the drain potential alsoinfluencesthe channel potential and degrade the control of the gate over the channel potential. This degradation includes the drain induced barrier lowering (DIBL), increased off state leakage current (I_{off}),subthresholdswing (SS) and threshold voltage roll-off(TVRO).These effects are known as short channel effects(SCEs) and these effects degrade the performance of the device. All the existing transistor are based on the use of semiconductor junctions. As the device length is reduced in size, the formation of junction between source and body or drain and body has become a problem in an ideal MOSFET and junctions are difficult to fabricate. To surpass these effects, a new technology device has been introduced known as **"Junctionless Nanowire Transistor(JLNT)"**. Junctionless nanowire transistor(JLNT) developed at Tyndall National Institute in Ireland, is transistor with no PN junction and uniformly doped throughout the device and typically range from 10^{19} to 10^{20} [1].Junctionlesstransistor are either N+/N+/N+ or P+/P+/P+ devices. In a junctionless gated resistor, the doping concentration in the channel is identical to the source and drain. Because the gradient of the doping concentration between source and channel or drain and channel is zero, no diffusion can take place, which eliminates the need for costly ultrafast annealing techniques and allows one to fabricate devices with shorter channels [2]. Junctionless transistor is highly resistive to short channel effects (SCEs) as there is no pn junction. The Junctionless Nanowire Transistor (JLNT) is a multigatedevice which operates in the similar principle to a conventional MOSFET [3]. During ON state when the gate voltage is greater than the threshold voltage, larger body current flows due to heavy doping concentration in the channel region. During OFF state when the gate voltage is less than threshold voltage, the channel is fully depleted due to work function difference between gate material and semiconductor device layer [4]. In our work, we have compared two different structures of JLNT, junctionless rectangular gate (JLRG) and junctionless cylindrical gate (JLCG). These two structures have already been proposed at a recent past but never compared between them on the base of short channel effects.In these particular device structures, SCE parameters have been observed with the increase of channel length. According to our observation, we can conclude that JLCG is better between them because Subthreshold Swing is almost 60mV/decade which is near to ideal and DIBL is low.

II. DEVICE MODELING AND SIMULATION SETUP



(a) (b)

Fig 1. (a) Cross Sectional and (b) 3D view of the Cylindrical Gate Junction Less Nanowire Transistor. The gate length for the simulated device is taken as 15 nm while the diameter of channel is 4 nm. The SiO_2thickness is 1 nm.



(a) (b)

Fig. 2.(a) Cross Sectional and (b) 3D view of the Rectangular Gate Junction Less Nanowire Transistor. The gate length for the simulated device is taken as 10 nm while the thickness of channel is 6 nm. The SiO_2 thickness is 1 nm.

Fig. 1 and 2 describe the structure of two devices. 3-D simulator TCAD Silvaco Atlas is used to characterize the electrical transport characteristic.Different parameters such as I_{on}/I_{off} ratio,DIBL, Subthreshold Swing (SS), Threshold voltage roll off are all investigated by varying channel length and oxide thickness of our nanoscale structures.

In our simulation, constant voltage and temperature (CVT) or Lombardi model for carriers is used to capture field dependent mobility, phonon scattering limited mobility, impurity scattering limited mobility and also surface roughness induced mobility [5]. The Shockley–Read–Hall (SRH) model is used to analyze the recombination effect of devices. This model is based on a quasi-stationary approximation tosimulate the interface trap charges[6].

Further, we have used NEWTON GUMMEL Method which causes the solver to start with Gummel (decoupled) iterations to generate a better guess and then switch to Newton, if convergence is not achieved [7].

III. RESULT & DISCUSSION

A. Simulation parameters

TABLE-I

SIMULATONPARAMETERS

Structure	Channel Length L_g (nm)	Channel Doping (cm^{-3})	Oxide Thickness T_{ox} (nm)	Channel Thickness T_{si} (nm)
JLRG	10	10^{19}	1	6
	12	10^{19}	1	6
	15	10^{19}	1	6
	16	10^{19}	1	6
	18	10^{19}	1	6
JLCG	10	10^{19}	1	4
	12	10^{19}	1	4
	15	10^{19}	1	4
	16	10^{19}	1	4
	18	10^{19}	1	4

B. I-V characteristics

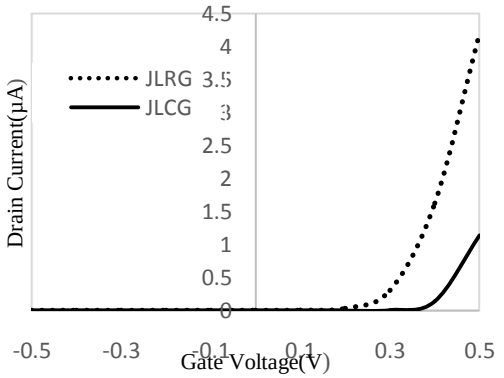


Fig3.I_dVsV_{gs} comparison curve of JLCG and JLRG for T_{ox}= 1nm and V_{ds}= 0.3V

In Fig. 3, the electrical transportcharacteristic ofJLRG and JLCG transistor has been shown.

C. Threshold Voltage Roll Off (TVRO)

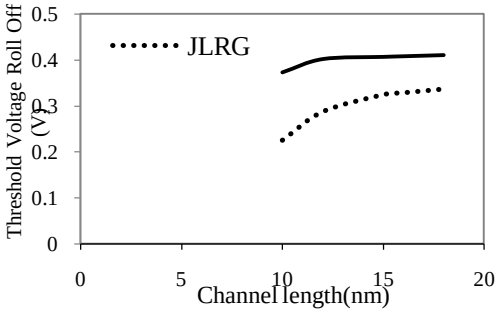


Fig. 4. Threshold voltage Roll off Vs L_g comparison curve of JLCG and JLRG for T_{ox}= 1nm and V_{ds}= 0.3V

The threshold voltage of the JLNTs is the gate voltage, which converts the fully depleted channel into a partially depleted one to start the bulk current conduction between the source and drain of the device [8].Threshold voltage is measured by using constant current method. The comparison study of the JLRG and JLCG has shown in Fig 7 in terms of threshold voltage by varying channel length. From the figure, we can observe that V_{th}increasesas the channel length increases. Because increased channel length increases inversion charge carriers at the channel region.

D. I_{on}/I_{off}Ratio

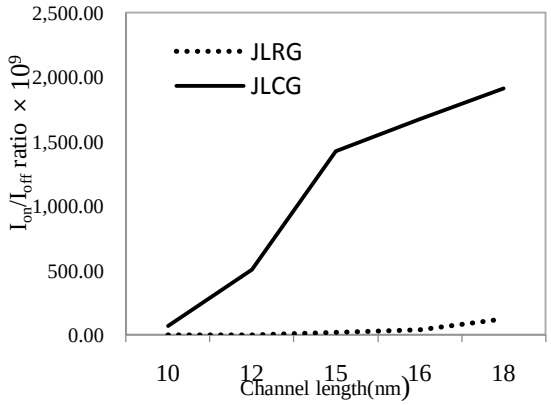


Fig 5. I_{on}/I_{off}VsL$_g$ comparison curve of JLCG and JLRG for T_{ox} = 1nm and V_{ds} = 0.3V

The I_{on}/I_{off}ratio as a function of channel length is illustrated in Fig. 5. It observed that as the length of the channel increased from 10nm to 18nm,the I_{on}/I_{off} current ratio also increased in both JLCG and JLRG. From the Fig 5, it is shown that the value of On/Off current ratio at L=18nm is high in JLCG because the leakage current at L=18nm is less compared to other length. So I_{on}/I_{off} ratio is high in JLCG as compared to JLRG.

E. Subthreshold Swing (SS)

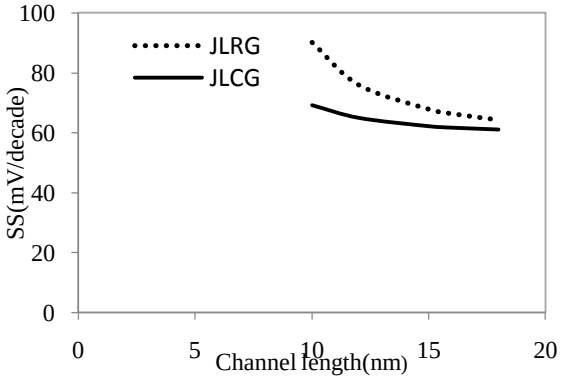


Fig 6. SS Vs L$_g$ comparison curve of JLCG and JLRG for T_{ox}= 1nm and V_{ds}= 0.3V

In Fig.6, the variation of subthreshold swing as a function of channel length is shown. The value of subthreshold swing (SS) was calculated by following equation,

$$SS = \frac{\partial Vgs}{\partial log\ 10 Ids} (1)$$

Subthreshold swing is the reciprocal of subthreshold slope. Subthreshold slope is the switching parameter of the device going from off state to on state and vice versa. From the Figure it observed that JLCG has subthreshold swing near to 60mV/decade which is the theoretical limit of subthreshold swing [9]. It is also observed that SS decreases with the increment of channel length. The approximated reason may be that the drain current increases with channel length. JLCG shows smaller SS than JLRG means that better gate control and improved I_{on}/I_{off} ratio in JLCG.

F. DIBL

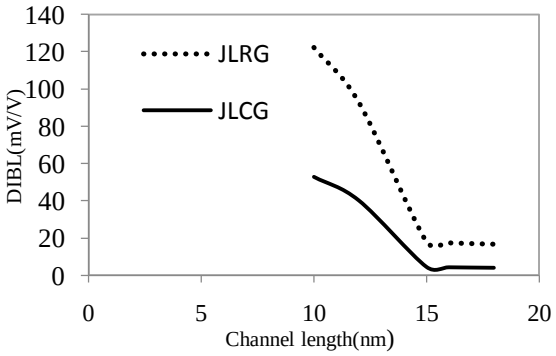


Fig 7. DIBL Vs L$_g$ comparison curve of JLCG and JLRG for T_{ox}= 1nm

In Fig. 7, DIBL is shown as a function of channel length. DIBL is an important parameter in short channel devices. DIBL measures the decreasing of the threshold voltage due to the reduction of the potential barrier at source region at high drain voltage. DIBL was calculated by following Equation,

$$DIBL = -\frac{\Delta Vth}{\Delta Vds} (2)$$

Once the drain depletion region is more significant in shorter devices, they present higher DIBL values, which indicates higher variances of the threshold voltage [10]. So, there is a higher increase of DIBL for decreasing channel length, due to the influence of the electric field near the drain. Fig 7 illustrated that as the channel length increases,I_{off}decreases,V_{th}increases so DIBL increases. It also observed that JLCG at L=15nm shows 4.48mV/V DIBL where JLRG shows 18.13mV/V DIBL. In that parallelism, JLCG shows better performance.

IV. CONCLUSION

In this work, short channel effects (SCEs) of JLRG GAA and JLCG GAA observed by changing channel length and oxide thickness of these structures. Various simulation results discussed along with the graphs. From the observation, we can conclude that JLCG shows significant improvement in SCEs than JLRG. JLRG shows better result in terms of threshold voltage roll off than JLCG but in the consideration of better stability over channel length alteration, JLCG is a better candidate.In case of SS, JLCG shows almost ideal value of SS and it gives better I_{on}/I_{off}ratio due to less leakage and better gate control over channel. On the other hand, JLCG shows better performance in case of DIBL whereas JLRG shows comparatively poor performance because of small change of threshold voltage with the change of drain voltage.Based upon the above discussion, JLCG is better device than JLRG in downscaling challenge and SCEs issues.

Finally, the arguments of this section above are summarized in the table below:

Table-II

SUMMARY of JLRG and JLCG

Criteria	Performance of JLRG	Performance of JLCG
TVRO	Better	Good
SS	Good	Better
I_{on}/I_{off}Ratio	Good	Better
DIBL	Good	Better

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